APPLICATION OF THE CASCADED MULTILEVEL INVERTER AS A SHUNT ACTIVE POWER FILTER

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Abstract

The thesis addresses the application of the cascaded multilevel inverter as a shunt active power filter. The series connection of semiconductor devices and multilevel inverters are compared in terms of conduction and switching losses, total harmonic distortion and distortion factor of the phase and line voltages, and common mode voltage. A generalized approach is proposed for conduction loss calculation when using carrier based pulse width modulation techniques. Different techniques for controlling multilevel inverters are presented and evaluated. A generalized algorithm for multilevel space vector modulation is proposed that gives a fixed, fast execution time independent of the number of levels. Four novel techniques for multilevel inverter space vector modulation generation are assessed, viz., phase shifted, mapped phase shifted, hybrid, and mapped hybrid space vector modulation. Innovative predictive current control for the two-level shunt active power filter is proposed. The capacitor voltage control harmonic current extraction technique used for the two-level shunt active power filter is extended to the three-level shunt active power filter, which utilizes conventional multilevel space vector modulation and phase shifted space vector modulation. A novel capacitor voltage balancing technique is extended to the five-level shunt active power filter, which employs phase shifted and hybrid space vector modulation techniques. Simulation and experimental results validate the proposed modulation techniques.

Dedication

To my best friend 'Akram' who passed away during my Ph.D.

Acknowledgement

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List of Symbols

C	Capacitance	F
E	Voltage per unit cell of phase x	V
e_x	Voltage of point of common coupling	V
f	Supply frequency	Hz
f_s	Sampling frequency	Hz
f_{sw}	Switching frequency	Hz
i_d	Active current	A
$\bar{i}_d$	Fundamental active current	A
$\tilde{i}_d$	Harmonics active current	A
i_{fx}	Active filter current of phase x	A
i_{Lx}	Load current of phase x	A
i_q	Reactive current	A
$\bar{i}_q$	Fundamental reactive current	A
$\tilde{i}_q$	Harmonics reactive current	A
i_{sx}	Supply current of phase x	A
L	Inductance	H
m	Number of levels per phase voltage	
m_a	Modulation index	
m_h	The highest harmonic order to be reduced	
p	Active power	W
$\bar{p}$	Fundamental active power	W
$\tilde{p}$	Harmonics active power	W
q	Reactive power	VAR
$\bar{q}$	Fundamental reactive power	VAR
$\tilde{q}$	Harmonics reactive power	VAR
T_{sw}	Switching cycle	s
T_s	Sampling time	s

Abbreviations

ADC	Analogue to digital converter
APF	Active power filter
APOD	Anti-phase opposition disposition
CSI	Current source inverter
DB-PWM	Dead band pulse width modulation
DF	Distortion factor
DMA	Direct memory access
DSP	Digital Signal processor
EVM	Evaluation module
FFT	Fast Fourier transform
FPGA	Field programmable gate array
GTO	Gate turn-off thyristor
H-SVM	Hybrid space vector modulation
HVDC	High voltage direct current transmission
IGBT	Insulated gate bipolar transistor
MH-SVM	Mapped hybrid space vector modulation
MPS-SVM	Mapped phase shifted space vector modulation
NPC	Neutral point clamped
PCC	Point of common coupling
PD	Phase disposition
PF	Passive filter
POD	Phase opposition disposition
PS-SVM	Phase shifted space vector modulation
PWM	Pulse width modulation
SDM	Sigma delta modulation
SIC	Supper imposed carrier
S-PWM	Sinusoidal pulse width modulation
TCR	Thyristor controlled reactor
THD	Total harmonic distortion
THI-PWM	Third harmonic injection pulse width modulation
UPFC	Unified power flow controller
UPS	Uninterruptible power supply
VSI	Voltage source inverter

Preface

The thesis addresses the application of the multilevel inverter to shunt active power filtering.

Chapter one introduces different multilevel inverter configurations. Chapter two introduces different modulation control techniques applicable to multilevel inverters. The multilevel inverter and the series connection of semiconductor devices are compared in high-voltage, high-power applications. The comparison includes conduction and switching losses, total harmonic distortion and distortion factor for the phase and line voltages, and the common mode voltage. The hardware and software systems are described in chapter four. Chapter five proposes a generalized algorithm for multilevel space vector modulation with a fast, fixed digital signal processor execution time, independent of the number of levels. The algorithm is a systematic numerical-based algorithm. Chapter six proposes new multilevel space vector modulation techniques, viz; phase shifted, mapped phase shifted, hybrid, and mapped hybrid space vector modulation. The active filter and harmonic current extraction techniques are reviewed in chapter seven. Chapter eight proposes innovative predictive current control for the two-level shunt active power filter. Chapter nine extends the capacitor voltage harmonic current extraction technique to the three-level inverter for two different multilevel space vector modulation techniques. Chapter ten presents a novel capacitor voltage balance technique which minimized the number of sensors, using two multilevel space vector modulation techniques. The general conclusions, the author's contribution, and future research are presented in chapter eleven.

Chapter 1

Introduction

Multilevel inverters belong to the inverter circuit family, where the output voltage is comprised of intermediate discrete voltage levels [1.1]. The purpose of these circuits is to generate a high-voltage waveform using lower voltage switching devices. Typically, series connected devices are switched sequentially, producing an output pattern which contains discrete predefined steps. Each switch blocks its normal operating voltage, but the total output voltage can be much higher. Apart from the increased voltage capability, another advantage of the circuit is a reduced output harmonic content for a particular switching frequency, when compared to a conventional two-level inverter [1.2]. The multilevel inverter is capable of pulse width and pulse amplitude modulation.

The multilevel inverter concept [1.3] appeared in the early eighties [1.4] as an almost theoretical approach to overcome the limitations in voltage, power, and switching frequency imposed by power semiconductor devices. The neutral point clamped (NPC) inverter structure [1.5] was used in rail traction applications [1.6],[1.7]. In such applications, the reduction of the harmonic content in the voltage and current outputs produced by inverters with 4.5 kV / 3 kA GTO thyristor (gate turn-off thyristor), switched at relatively low frequency (200 to 300 Hz maximum), is of paramount importance. In addition, the multilevel structure reduces voltage stresses on semiconductor devices, permitting the direct connection of the inverter to the contact line in the case of a 3 kV DC supply [1.8].

The multilevel concept has been used in other applications. In [1.9] a non-conventional power inverter for plasma stabilization was presented, where the series connection of the H-bridge inverter was proposed as a way to build voltage waveforms characterized by any number of levels. This modular approach to inverter design was further studied [1.10], [1.11] and generalized for three-phase applications [1.12]. The extension of the NPC structure to the generation of any number of voltage levels first appeared in [1.13]. As with the two-level inverter, there are models for multilevel inverters [1.14], [1.15] and the performance of the multilevel inverter is discussed in [1.16].

As the IGBT (insulated gate bipolar transistor) developed and became capable of managing considerable power levels at a relatively high switching frequency [1.17],[1.18], the multilevel concept was rediscovered. Multilevel inverters are now being considered for applications such as active filtering, power system reactive

power compensation [1.19], and large induction motor drives [1.20]. Multilevel inverters can be classified into different types as shown in figure (1.1)

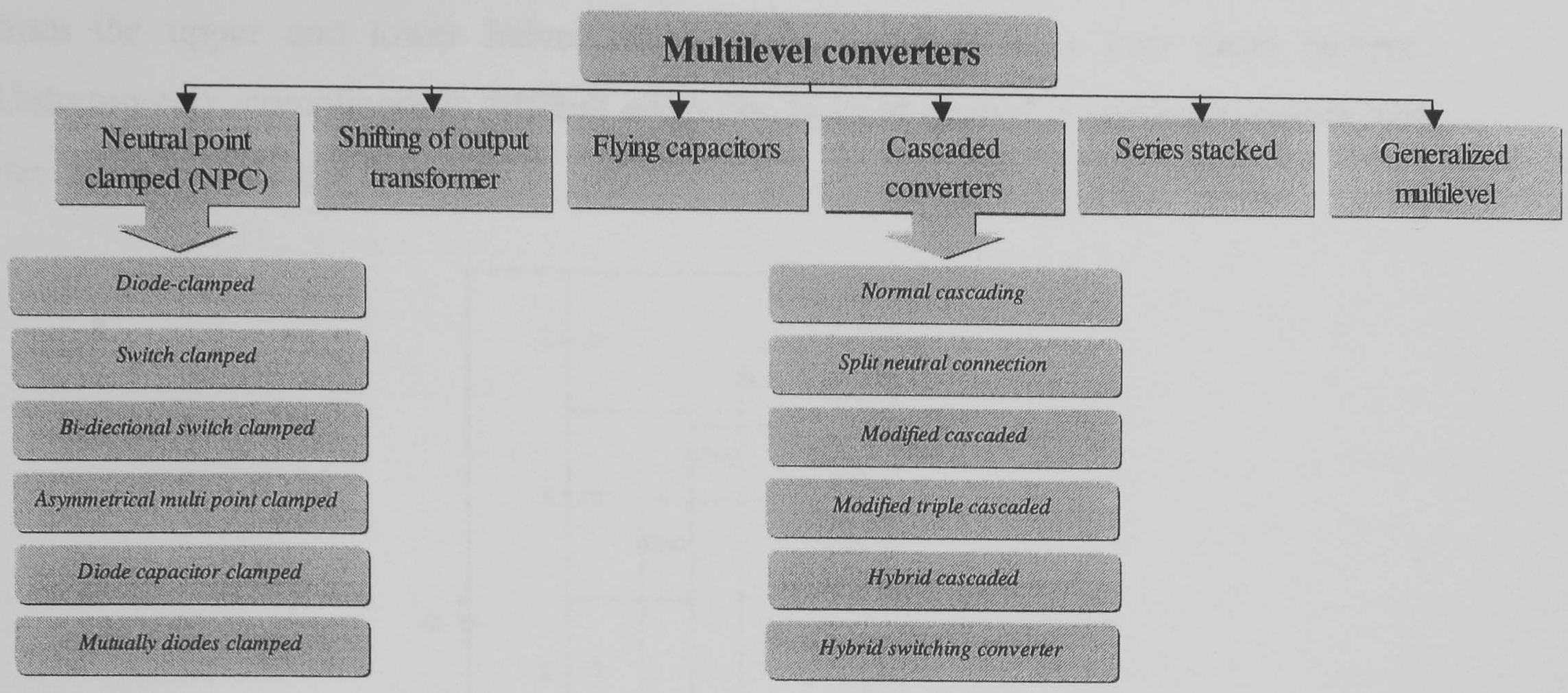


Figure 1.1. Classification of multilevel inverters

1.1 Neutral point clamped multilevel inverter

The neutral point clamped (NPC) inverter was introduced by Nabea et al. [1.5], and had a multilevel structure. The half-bridge version of the three-level NPC inverter provides three output voltage levels ($\pm$E and 0) where E is the constant voltage per level, whilst the full-bridge configuration can generate five output voltage levels ($\pm$2E, $\pm$E, and 0). The generalized multilevel structure, which can be arbitrary extended to any number of output voltage levels, as proposed by Choi et al. [1.21], can be considered as an extension of the three-level NPC inverter. This inverter has an inherent voltage-balancing problem which makes real power flow control difficult. An excessive number of clamping diodes is required when the number of levels is high. Also a high voltage rating is required for some of the blocking diodes [1.22]. Neutral point clamped [1.23]-[1.28] multilevel inverters can be classified into the following six categories, according to the inverter voltage clamping method.

1 Diode-clamped inverter

In the diode-clamped inverter, a single DC link series capacitor bank is used which is divided into sublevels as shown in figure (1.2). The switching devices are arranged in series. Diodes provide connection to the capacitor sublevels. The three-level diode clamped circuit or NPC circuit was the first multilevel circuit proposed [1.5]. The switching sequence connects the output to either the neutral point (midpoint of the capacitors), positive DC link, or negative DC link, as shown in figure (1.3). The two

capacitors share equally the total DC link, provided that no mean current is drawn from the neutral point. Under normal operating conditions, equal power should be drawn from the upper and lower halves of the link, resulting in a zero mean current. Unfortunately, compliance is difficult and some form of control is needed to ensure that the capacitor voltages balance.

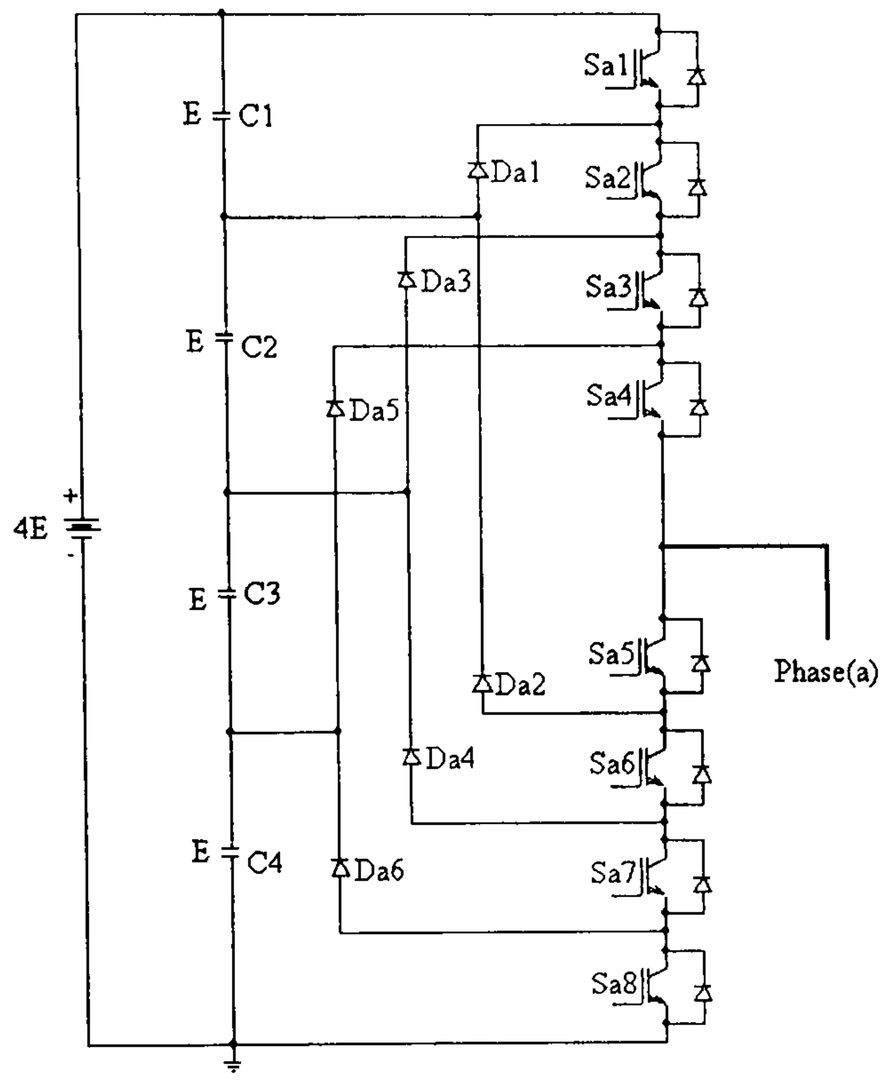


Figure 1.2. Diode clamped 5-level inverter circuit diagram

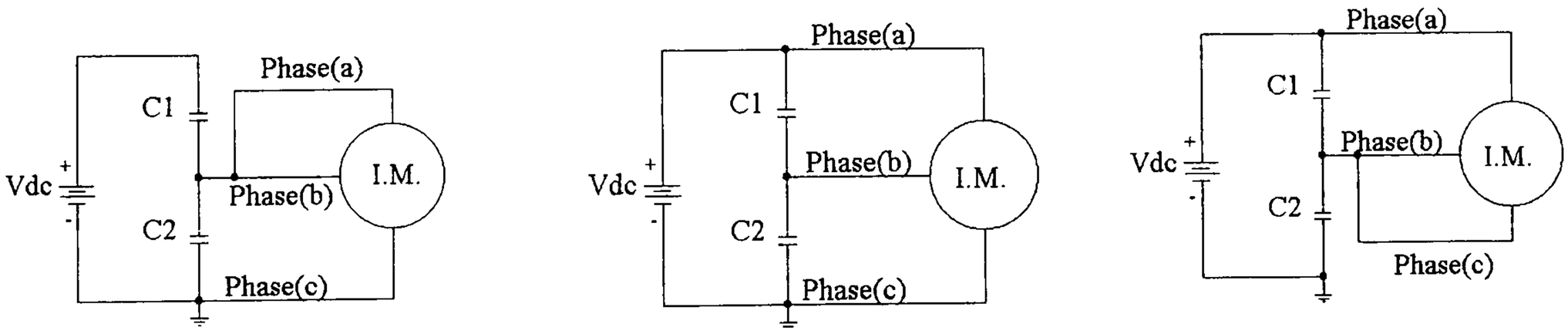


Figure 1.3. Three level inverter feeding an induction motor

The *first* simplest and the most used balancing method, uses n controllable switches each with a series resistance, in parallel to the capacitors. By chopping, the higher voltage is discharged and balance is obtained, however losses are increased.

The *second* balancing method is to transfer the energy among the asymmetrical charged capacitors. Voltage control can be achieved by using non-dissipative circuitry, such as the buck-boost inverter proposed in [1.21].

The *third* balancing solution is to vary the firing sequence by exploiting inverter sequence redundancies [1.29]. This approach minimizes the additional balance requirements but may increase the switching frequency of the power devices, which increases system losses.

Since the control requirements are relatively simple, this circuit is of considerable interest for industrial drives (medium voltage GTO drives [1.30]) and traction (IGBT drives [1.31]).

The diode clamped circuit is theoretically expandable to m-levels as discussed in [1.21]. The next main configuration is the five-level inverter, as shown in figure (1.2). Switching of the devices will connect the output to any of the levels in the DC link. However analysing the power flow through the circuit shows that, whilst the neutral point should remain balanced, the upper and lower capacitor pairs cannot remain balanced whilst power is being drawn at the output. In order for the circuit to function in real applications, some form of active balancing must be employed to ensure that the capacitors remain correctly charged. Another difficulty is that although the IGBTs only need to block their normal operating voltage (E), the clamping diodes connecting each leg to the capacitor bank, may have to block voltages up to (3E). Series connection of diodes in order to meet this is possible, particularly if the devices can be matched correctly thereby avoiding the need for snubbers (i.e. use diodes from the same wafer). Increasing the number of levels beyond five becomes problematic, both in terms of capacitor balancing and clamping diode requirements. Furthermore, the isolation voltage of individual switches becomes important as the output voltage increases. It is therefore unlikely that practical drives will expand much beyond five levels using this structure.

With increased use, still larger capacity inverters are expected. However since the capacities of switching devices are insufficient, certain techniques and controlling methods have been proposed for the parallel connection of NPC inverters as discussed in [1.32]-[1.35].

2 Switch-clamped inverter

Clamping is achieved using switches as shown in figure (1.4a) instead of diodes as in the first inverter type.

3 Bi-directional switch-clamped inverter

The clamping is achieved using a bi-directional switch, as shown in figure (1.4b)

4 Asymmetrical multipoint clamped inverter

Consider the multi-point clamped (MPC) structure proposed in [1.1] and [1.13], represented in figure (1.5) for the case of a single-phase application, in a configuration with three DC link capacitors.

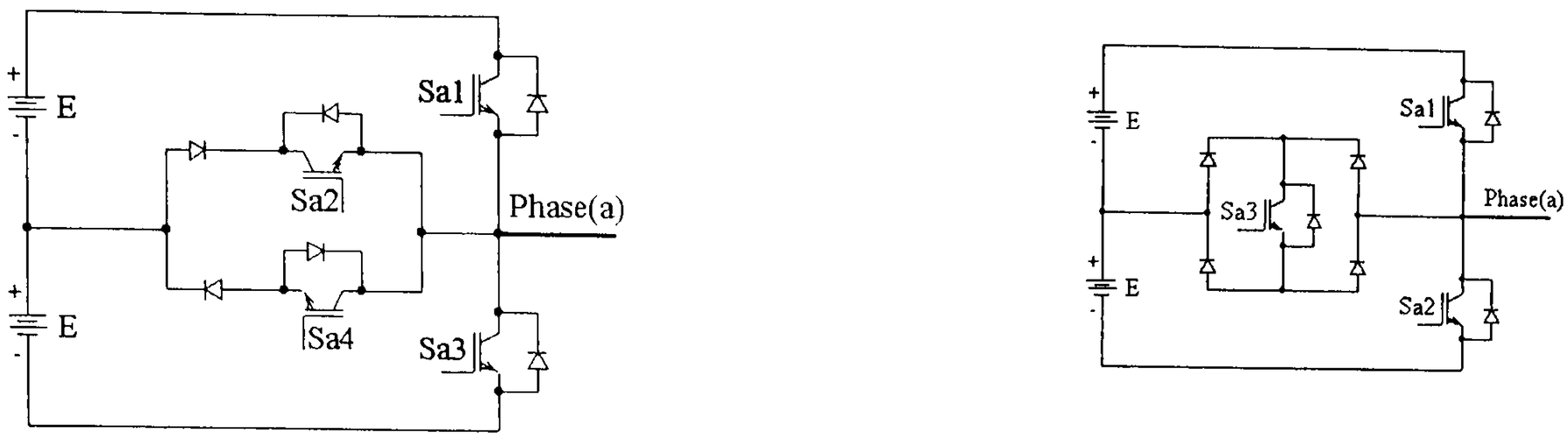


Figure 1.4. (a) Switch-clamped inverter and (b) Bi-directional switch-clamped

This single-phase MPC inverter could be used on the AC side of electronic rail locomotives [1.36]. If the central capacitance is half the outer capacitances, the DC link voltage is not equally shared among the three capacitors. That is

$$C_1 = C_3 = 2C_2 \tag{1.1}$$

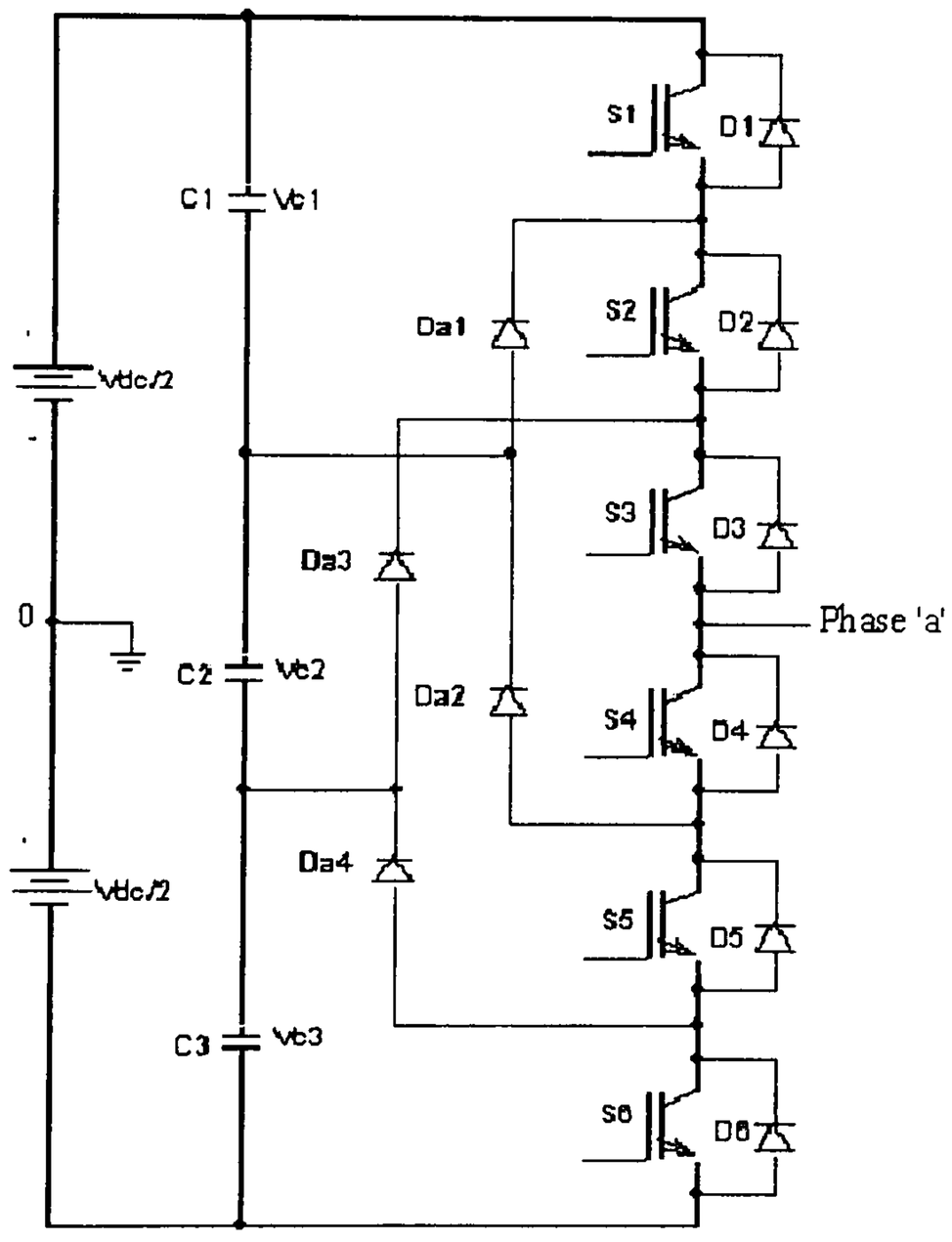


Figure 1.5. Single-phase multi-point clamped inverter with three DC link capacitors

The voltages across the capacitors are

$$V_{c1} = V_{c3} = \tfrac{1}{4} V_{DC}, \quad V_{c2} = \tfrac{1}{2} V_{DC} \tag{1.2}$$

This is an initial condition that must be satisfied during inverter operation by using control circuitry and/or extra passive/active components. The central capacitors in MPC structures are subjected to charging and discharging phenomena that result in undesired voltage imbalance among the DC capacitors [1.29]. The output terminals A and B can be connected to four DC levels ($\pm \frac{1}{2} V_{DC}$, $\pm \frac{1}{4} V_{DC}$) with respect to ground, shown as 0 in

figure (1.5), which means sixteen different switching sequences (some redundant) as shown in Table 1.1. Redundancy in switching sequences is a property of multilevel inverters that can be exploited to achieve some additional goals, such as switching optimisation [1.10] or voltage sharing among the DC link capacitors [1.29].

In this scheme, the switching sequence is exploited to achieve a greater number of levels in the AC voltage output waveforms. Table 1.1 shows nine line-to-line voltage levels ($\pm V_{DC}$, $\pm \frac{3}{4} V_{DC}$, $\pm \frac{1}{2} V_{DC}$, $\pm \frac{1}{4} V_{DC}$, *and 0*.)

Table 1.1. Relationship between line-to-line voltage, phase voltage, and switching sequences

V_{AB} $\times V_{DC}$	V_{AO} $\times V_{DC}$	V_{BO} $\times V_{DC}$	S_{a1} and $\overline{S_{a4}}$	S_{a2} and $\overline{S_{a5}}$	S_{a3} and $\overline{S_{a6}}$	S_{b1} and $\overline{S_{b4}}$	S_{b2} and $\overline{S_{b5}}$	S_{b3} and $\overline{S_{b6}}$
-1	$-\frac{1}{2}$	$\frac{1}{2}$	0	0	0	1	1	1
$-\frac{3}{4}$	$-\frac{1}{2}$	$\frac{1}{4}$	0	0	0	0	1	1
	$-\frac{1}{4}$	$\frac{1}{2}$	0	0	1	1	1	1
$-\frac{1}{2}$	$-\frac{1}{4}$	$\frac{1}{4}$	0	0	1	0	1	1
$-\frac{1}{4}$	$-\frac{1}{2}$	$-\frac{1}{4}$	0	0	0	0	0	1
	$\frac{1}{4}$	$\frac{1}{2}$	0	1	1	1	1	1
0	$-\frac{1}{2}$	$-\frac{1}{2}$	0	0	0	0	0	0
	$-\frac{1}{4}$	$-\frac{1}{4}$	0	0	1	0	0	1
	$\frac{1}{4}$	$\frac{1}{4}$	0	1	1	0	1	1
	$\frac{1}{2}$	$\frac{1}{2}$	1	1	1	1	1	1
$\frac{1}{4}$	$-\frac{1}{4}$	$-\frac{1}{2}$	0	0	1	0	0	0
	$\frac{1}{2}$	$\frac{1}{4}$	1	1	1	0	1	1
$\frac{1}{2}$	$-\frac{1}{4}$	$-\frac{1}{4}$	0	1	1	0	0	1
$\frac{3}{4}$	$\frac{1}{4}$	$-\frac{1}{2}$	0	1	1	0	0	0
	$\frac{1}{2}$	$-\frac{1}{4}$	1	1	1	0	0	1
1	$\frac{1}{2}$	$-\frac{1}{2}$	1	1	1	0	0	0

5 Mutually diode clamped inverter

A five-level diode clamping inverter [1.37] is shown in figure (1.6). A total of eight switches and twelve diodes of equal voltage rating are used; the same as with the conventional diode clamping inverter with diodes in series [1.37]. Theoretically, this pyramid architecture can be extended to any level number. An *m*-level inverter leg requires *(m-1)* storage capacitors, *2(m-1)* switches, and *(m-1)(m-2)* clamping diodes. The following rules govern switching operation.

i. At any instant, there must be M-1 neighbouring switches ON.

ii. For each neighbouring switch, an outer switch can only be turned on when the inner switch is ON.

iii. For each neighbouring switch, an inner switch can only be turned off when the outer switch is OFF.

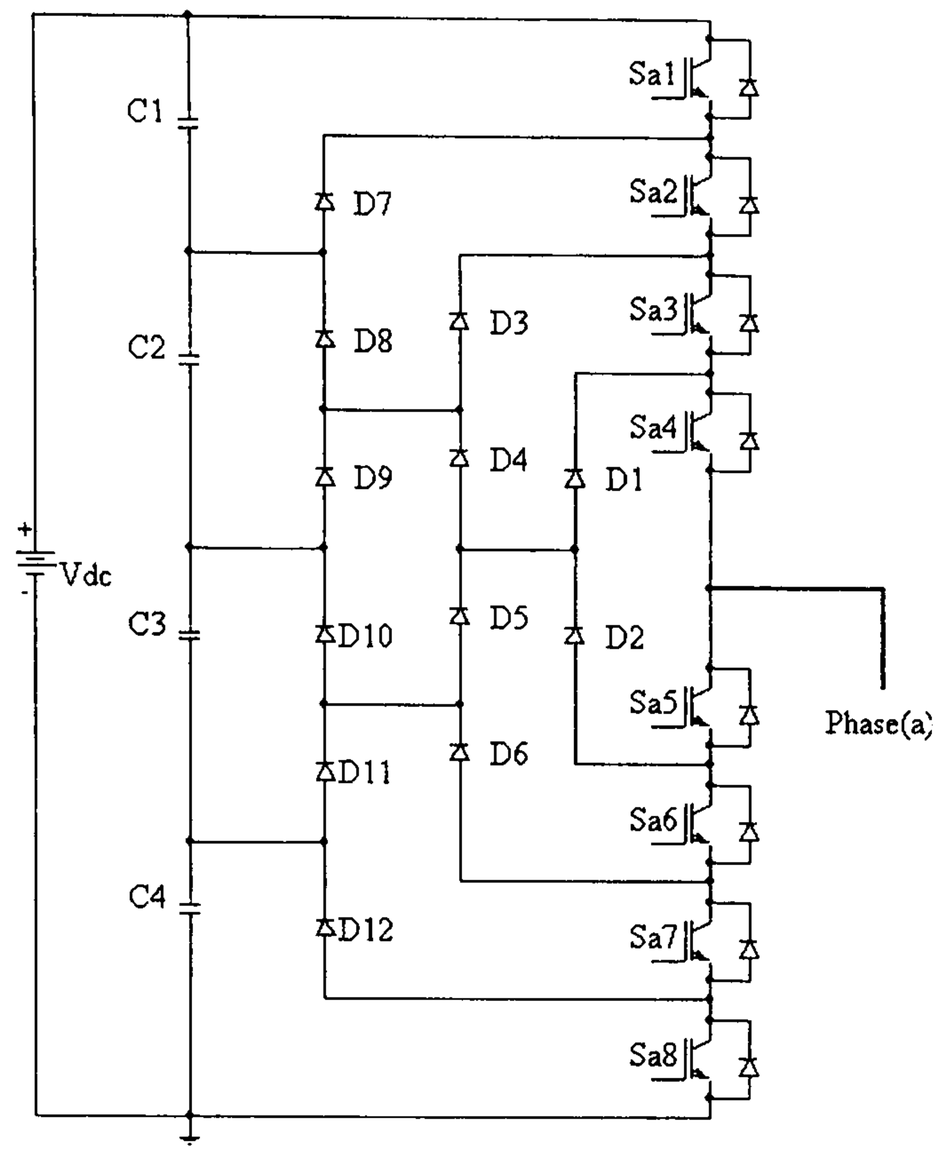


Figure 1.6. Structure of the diode clamping inverter (five-level)

Since stray capacitance of an outer switch experiences one more discharge than the inner switch, among the blocking devices, the outer switch blocks the lowest voltage. The center device experiences the highest voltage stress. This same unequal blocking voltage distribution problem, arising from indirect clamping, also occurs with the conventional diode clamping inverter. The severity of the problem depends on the stray inductances of the structure. With proper bus-bar design, and in particular, appropriate positioning of an auxiliary clamp, the problem is minimized. Figure (1.7) shows a resistive auxiliary clamping network for the diode clamping inverter.

From the analysis and experimentation presented in [1.37], the following conclusions are drawn regarding this inverter.

i. The diode clamping inverter avoids the diodes series connection problem of the conventional diode clamping inverter. Not only are the main switches clamped by the clamping diodes, the clamping diodes are also mutually clamped. No large RC network is needed to deal with the voltage sharing problem among series connected diodes.

ii. The unbalanced blocking voltage distribution problem resulting from indirect clamping, is expected to be reduced by adding an auxiliary clamping network.

The turn-on snubbering problem and the dc link imbalance problem are not resolved. This diode clamping inverter represents an improvement over the conventional structure and is expected to facilitate the practical application of this multilevel inverter to high power conversion.

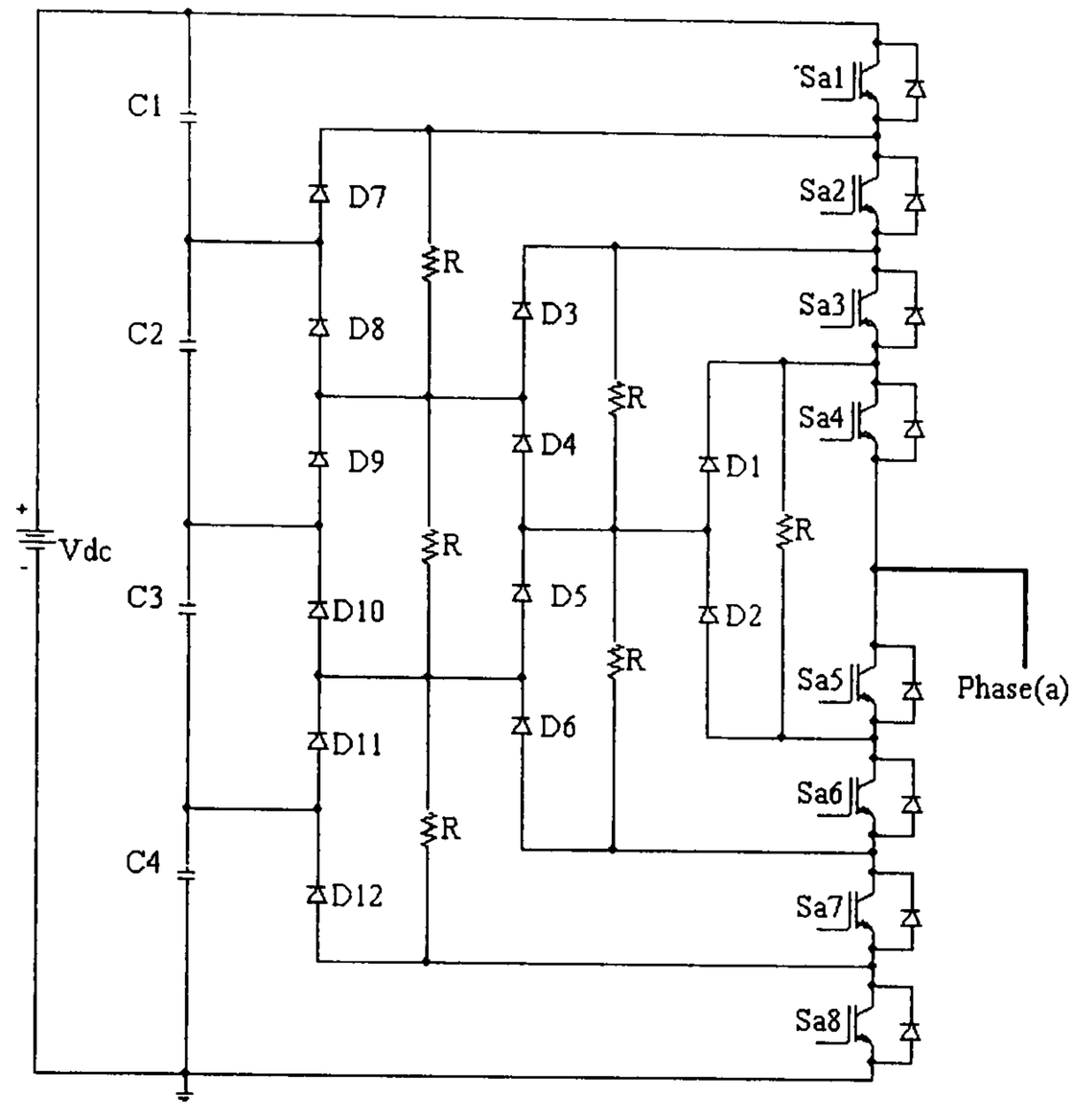


Figure 1.7. An auxiliary clamping network configuration for a diode clamping inverter

6 Diode-capacitor clamped inverter

Figure (1.8) shows one leg of the diode-capacitor clamped multilevel inverter structure [1.38]. It has the advantage of reducing the capacitor voltage imbalance and the over voltage across the inner switching devices. All the switching devices are independently connected to the divided capacitor voltages. The DC link voltage sources C_1 to C_4, supply power to the load.

1.2 Shifting output transformer multilevel inverter

This technique for obtaining output voltage multilevel operation (from the load side point of view) involves summing the output of different inverters by means of a suitable phase shifting transformer [1.91]. A structure made of 30-degree phase shifted inverters and an output transformer is shown in figure (1.9). A five level output results when two inverters and a common supply E, (subsequently 'level' refers to a phase output voltage) are used in conjunction with a delta/star and delta/zig-zag summing transformer.

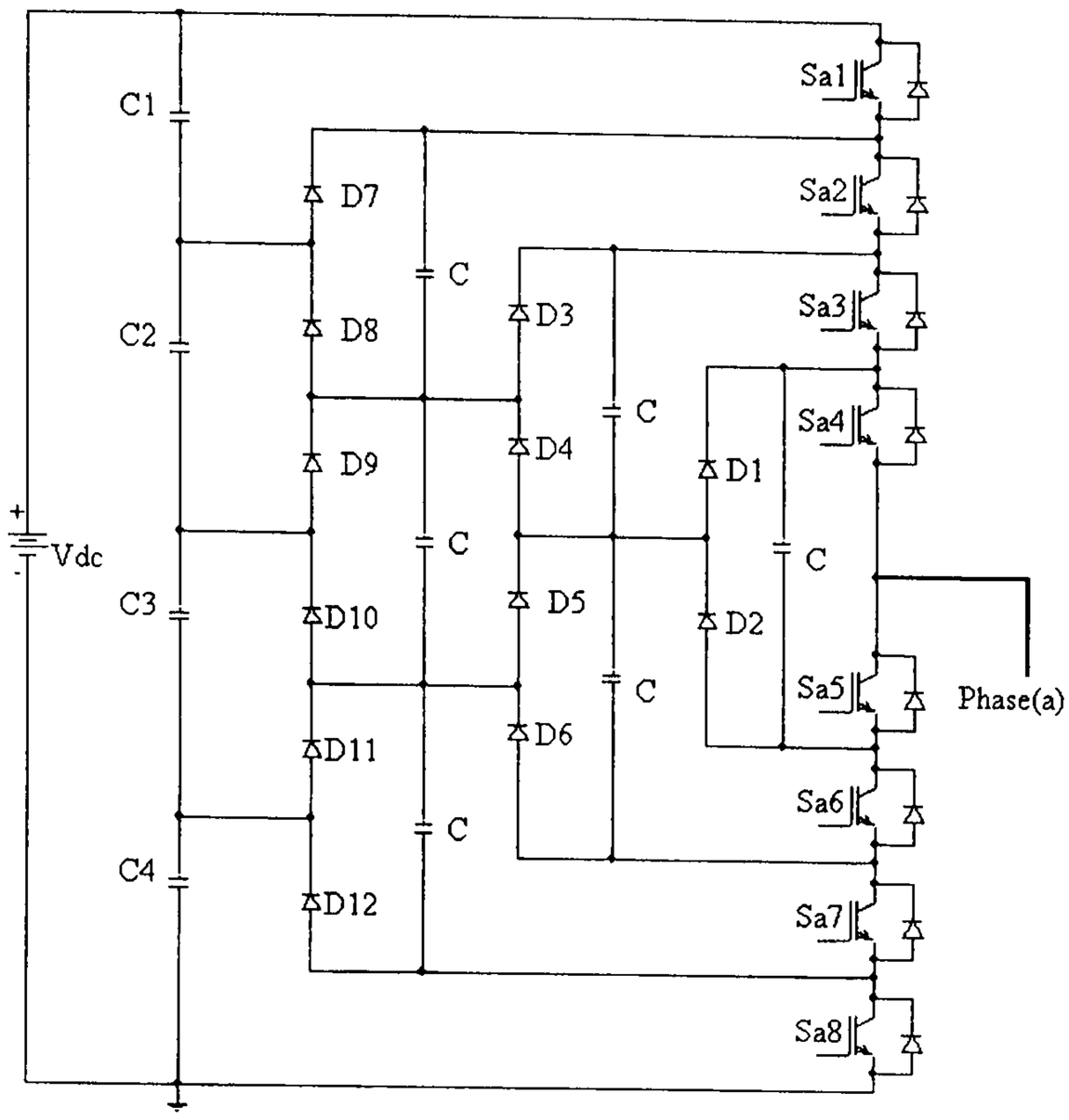


Figure 1.8. Diode-capacitor clamped multilevel inverter

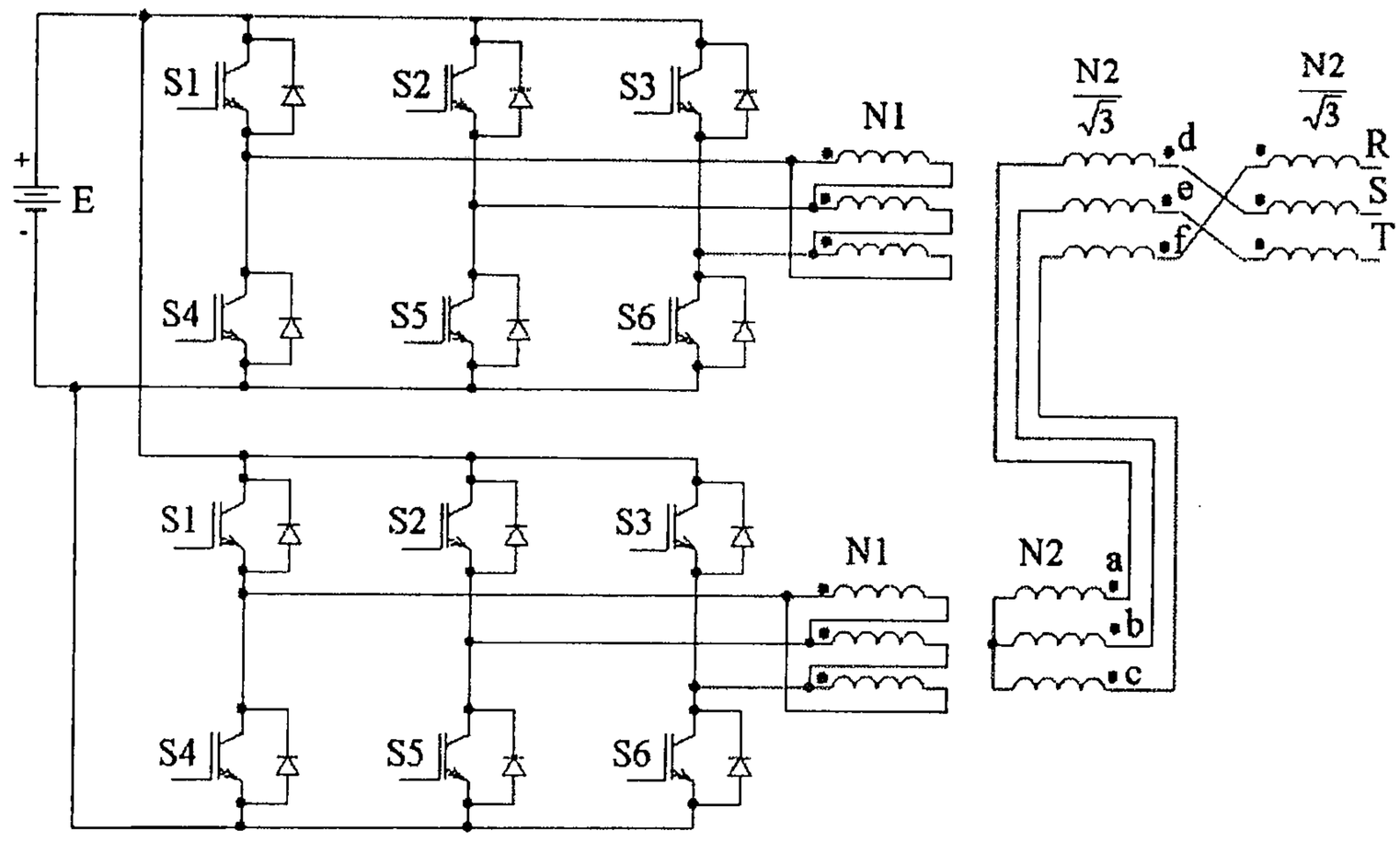


Figure 1.9. Output phase shifting transformer

In this way, inherent harmonic elimination is obtained, i.e., the third, fifth, and seventh harmonics are neutralized by the transformer connection, while higher order harmonics are reduced by means of PWM switching techniques. The principle illustrated can be extended to incorporate multilevel inverters, by increasing the number of bridges and transformers.

One recent major realization has been a 10 MW power conditioning system for battery energy storage applications. In this plant, multilevel operation is obtained by the series connection of (equivalent) single-phase inverters and transformers. The system is described as two equivalent leading and lagging 18 pulse stepped wave three-phase

inverters [1.41]. An additional advantage of the structure is that the transformer permits voltage matching and electrical isolation between the inverter and the load.

However, the main problem of the phase shifting technique is the transformer. The transformer is a bulky element that has to be added, and even though it does not saturate, it is difficult to avoid saturation at low frequency operation when voltage boosting is required in AC drives applications. For these reasons, the main application of this kind of structure is for fixed frequency output (high power UPS, power conditioning systems for energy conversions, etc.). High-power adjustable speed induction motor drives based on parallel-connected voltage source GTO thyristor inverters have been published. Instead of an output transformer, an interphase reactor is used to sum inverter output voltages [1.42].

1.3 Flying capacitor multilevel inverter

Another type of multilevel inverter is the flying capacitor inverter [1.43]-[1.46], as shown in figure (1.10). This multilevel circuit employs capacitors pre-charged to 4E, 3E, 2E, and E (for a five-level inverter). The capacitors float with respect to earth (hence the term 'flying'), and are connected to the output using series connected semiconductor devices as illustrated in figure (1.10). The principle for single-phase operation is that the switches can be used to connect the capacitors directly to the output. Capacitor voltages must be carefully controlled, otherwise the quality of the output voltage will deteriorate, and more importantly the blocking voltage imposed on certain devices may increase beyond their rating. Assuming a sinusoidal output current with a zero mean, if the capacitance is sufficiently large, there will be only small capacitor voltages variations [1.47]. However, in a practical motor drive application, where low frequencies are generated, and transient operation is common, some form of additional voltage control will be required. It is possible to create an output voltage by series connection of the capacitors, allowing current to flow in the direction required for recharging. For example, the output voltage 3E can be created by, as shown in Table 1.2.

i. Turning on switches 1, 2, 4, and 6 (4E-2E+E), figure (1.11a)
ii. Turning on switches 1, 3, 4, and 7 (4E-3E+2E), figure (1.11b)
iii. Turning on switches 2, 3, 4, and 8 (3E), figure (1.11c)
iv. Turning on switches 1, 2, 3, and 5 (4E-E), figure (1.11d)

Table 1.2. Inverter states

P.U. 4E	Sa1 (Sa8')	Sa2 (Sa7')	Sa3 (Sa6')	Sa4 (Sa5')
0	0	0	0	0
¼	0	0	0	1
¼	0	0	1	0
½	0	0	1	1
¼	0	1	0	0
½	0	1	0	1
½	0	1	1	0
¾	0	1	1	1
¼	1	0	0	0
½	1	0	0	1
½	1	0	1	0
¾	1	0	1	1
½	1	1	0	0
¾	1	1	0	1
¾	1	1	1	0
1	1	1	1	1

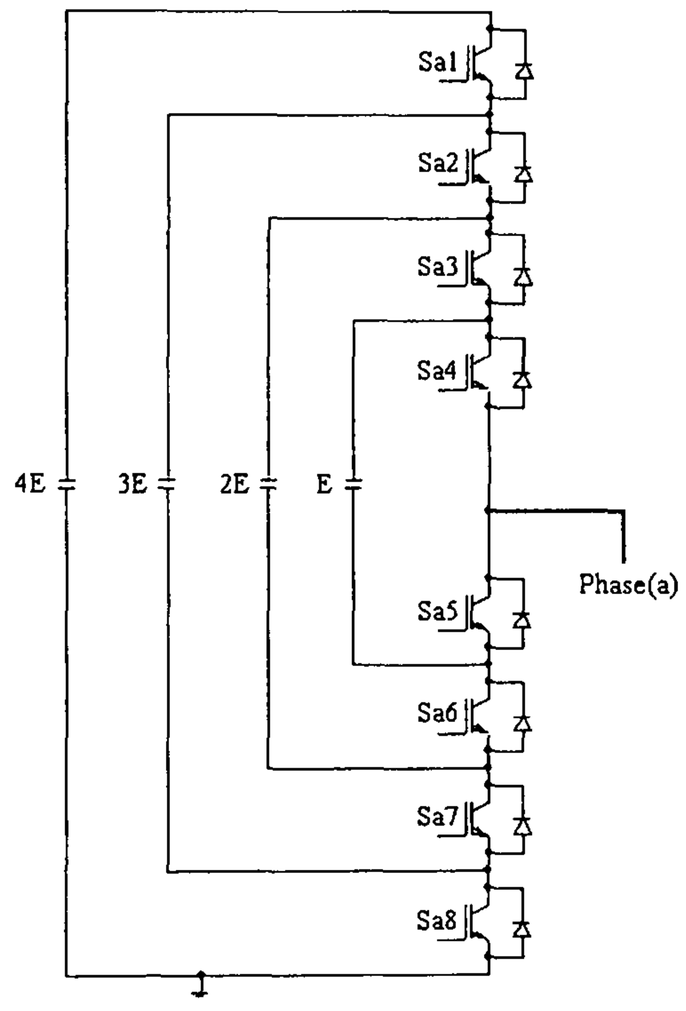
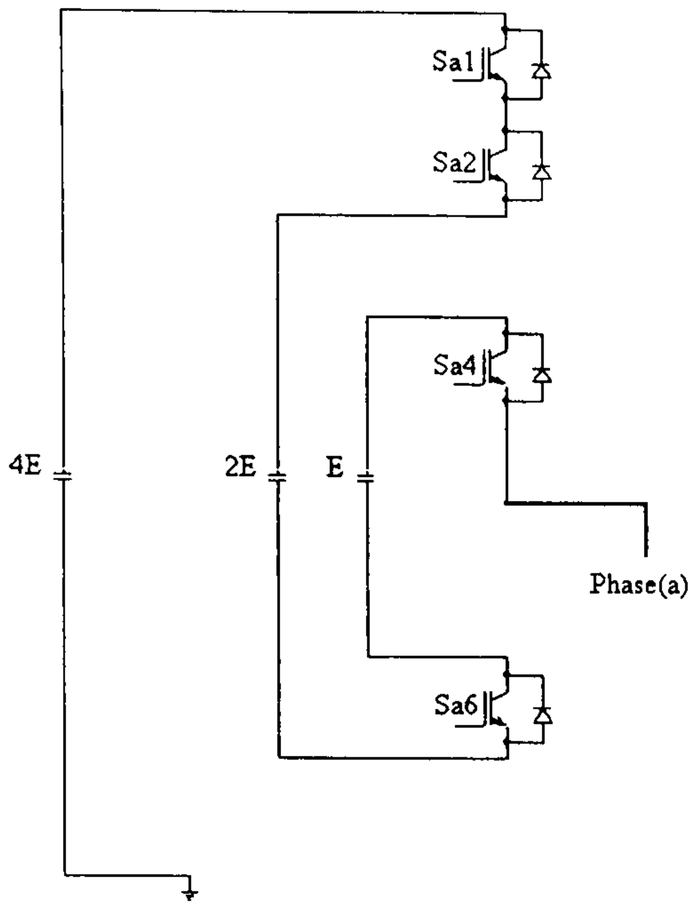


Figure 1.10. Flying capacitor multilevel inverter

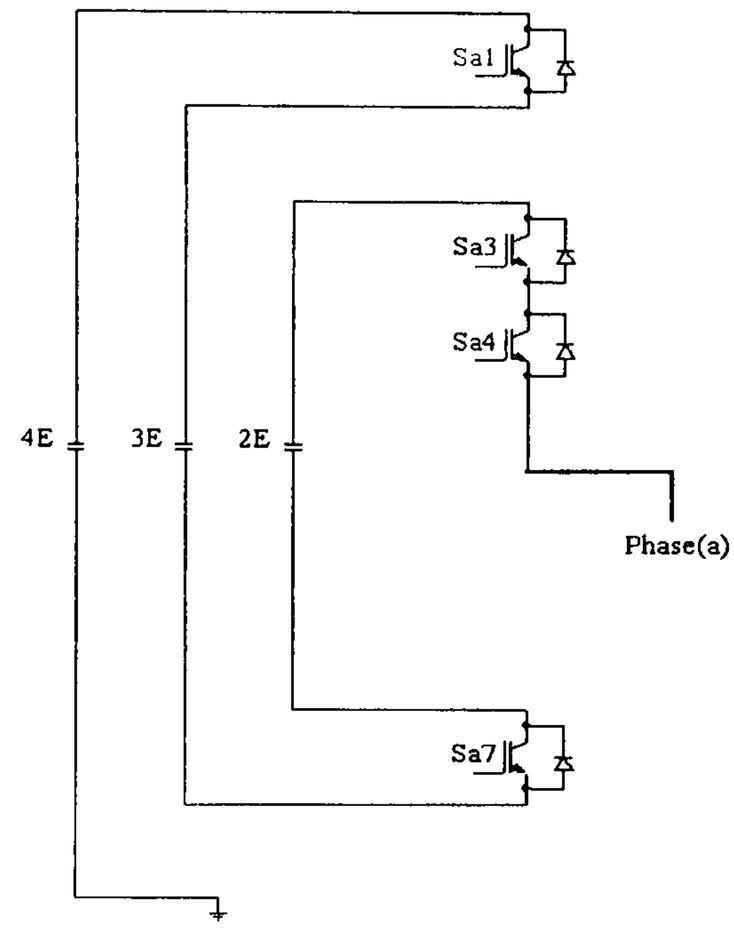
It can be appreciated that capacitor voltage control through switching pattern control becomes complex when the output is extended to three phases, and the real time processing requirement makes the system impractical. In addition, the capacitors need to be chargeed initially, a function that the basic circuit cannot inherently achieve. Additional circuitry is required.

The advantages [1.22] of this inverter are: large amount of storage capacitance provides extra ride through capabilities during power outage, it offers switch combination redundancy for balancing the different voltage levels, and both real and reactive power flow can be controlled, making it a possible voltage source inverter candidate for high-

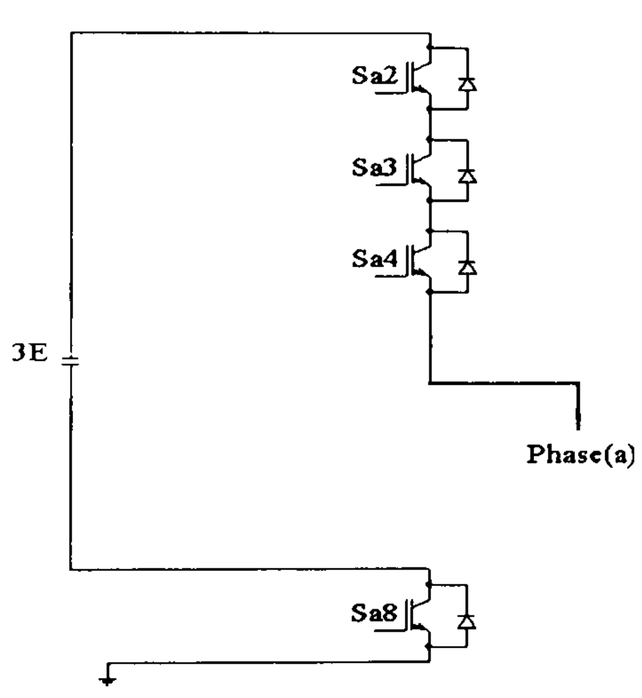
voltage DC transmission. The disadvantages are: an excessive number of storage capacitors are required when the level number is high, high-level systems are more difficult to package, and they are more expensive because of the required bulky capacitors. Inverter control is complicated and the switching frequency and switching losses are high for real power transmission [1.39], [1.40].



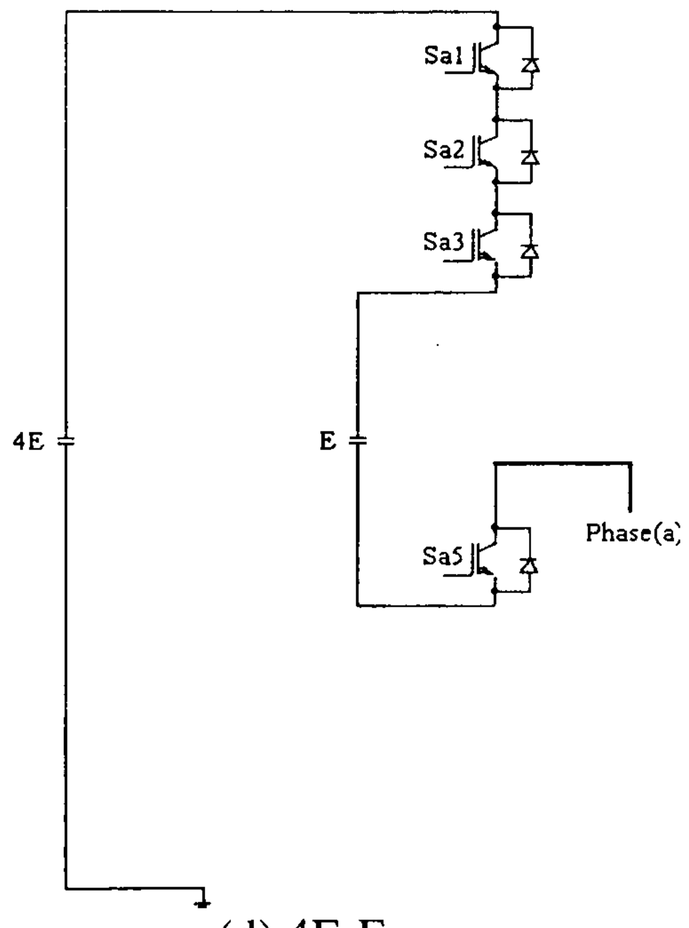
(a) 4E-2E+E



(b) 4E-3E+2E



(c) 3E



(d) 4E-E

Figure 1.11. Example of conduction paths to achieve a 3E output voltage

1.4 Cascaded multilevel inverters

The cascaded full-bridge inverter proposed by Marchesoni et al. [1.9] can be extended to an *m*-level output. However such a structure utilizes more isolated DC sources than the NPC inverter [1.48]-[1.51]. The cascaded multilevel inverter can be classified into the following six categories.

1 Normal cascaded multilevel inverter

The cascaded multilevel inverter or (the isolated H bridge circuit (IHC)) is the simplest multilevel inverter [1.2],[1.22]. As the name suggests, it uses familiar H-bridges connected in a series chain to generate the output pattern. A typical circuit is shown in figure (1.12). Each cell is capable of independently producing an output voltage of $\pm E$ or 0 in a chain of n cells, and the output voltage can vary between +nE to –nE, i.e., 2n+1 levels. Each individual cell requires an isolated supply, which is the main limitation. The method used to generate the isolated supplies often depends on the application. For use on satellites [1.52], isolated DC supplies were available from solar cells. Advantages [1.22] are: it requires the least number of components among all multilevel inverters to achieve the same number of voltage levels, modularised circuit layout and packaging is possible because each level has the same structure, there are no extra clamping diodes or voltage balancing capacitors, and soft switching can be used in this structure to avoid bulky and lossy R-C-D snubbers. The disadvantage is the need for separate DC sources for real power conversion.

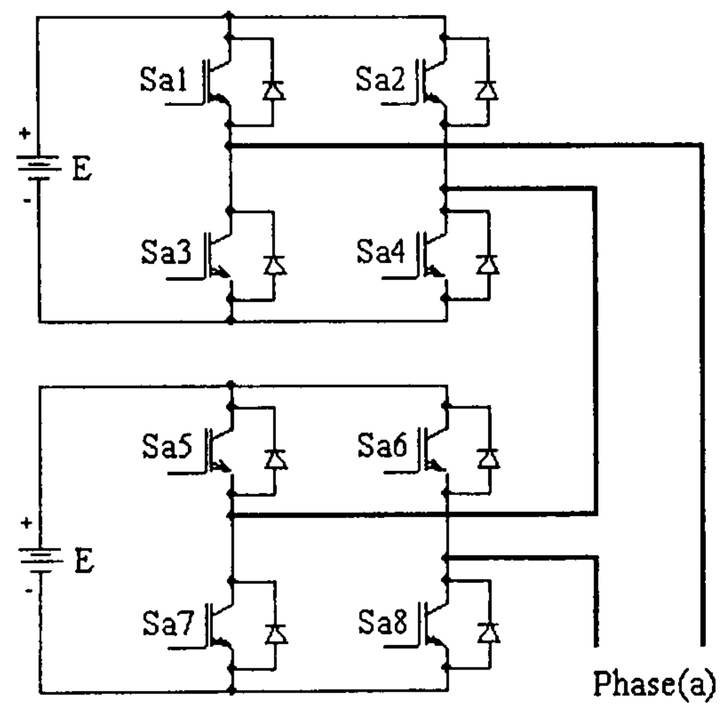


Figure 1.12. Normal cascaded five-level inverter

2 Split neutral

The split neutral cascaded inverter is shown in figure (1.13). It is constructed by separating the machine windings and connecting the ends of each coil between two inverters [1.53]. The inverters are supplied by separate isolated DC sources. Referring to figure (1.13), using Kirchhoff's voltage law the machine voltage equations can be written as

$$v_{as} = v_{a1g1} + v_{g1g2} - v_{a2g2} \tag{1.3}$$

$$v_{bs} = v_{b1g1} + v_{g1g2} - v_{b2g2} \tag{1.4}$$

$$v_{cs} = v_{c1g1} + v_{g1g2} - v_{c2g2} \tag{1.5}$$

Since both inverters are supplied from separate DC voltage sources, they can be thought of as independent nodes in a network and thus Kirchhoff's current law yields

$$i_{as} + i_{bs} + i_{cs} = 0 \tag{1.6}$$

It can be shown from the machine equations that the phase voltages sum to zero if the currents sum to zero. Given this fact, equations (1.3) to (1.5) can be added and the result can be solved for v_{g1g2}, to yield

$$v_{g1g2} = \frac{1}{3}(v_{a2g2} + v_{b2g2} + v_{c2g2} - v_{a1g1} - v_{b1g1} - v_{c1g1}) \tag{1.7}$$

Substituting equation (1.7) into equations (1.3) to (1.5), the machine voltages may be related to the phase to ground voltages as

$$v_{as} = \frac{2}{3}(v_{a1g1} - v_{a2g2}) - \frac{1}{3}(v_{b1g1} - v_{b2g2}) - \frac{1}{3}(v_{c1g1} - v_{c2g2}) \tag{1.8}$$

$$v_{as} = \frac{2}{3}(v_{b1g1} - v_{b2g2}) - \frac{1}{3}(v_{a1g1} - v_{a2g2}) - \frac{1}{3}(v_{c1g1} - v_{c2g2}) \tag{1.9}$$

$$v_{as} = \frac{2}{3}(v_{c1g1} - v_{c2g2}) - \frac{1}{3}(v_{a1g1} - v_{a2g2}) - \frac{1}{3}(v_{b1g1} - v_{b2g2}) \tag{1.10}$$

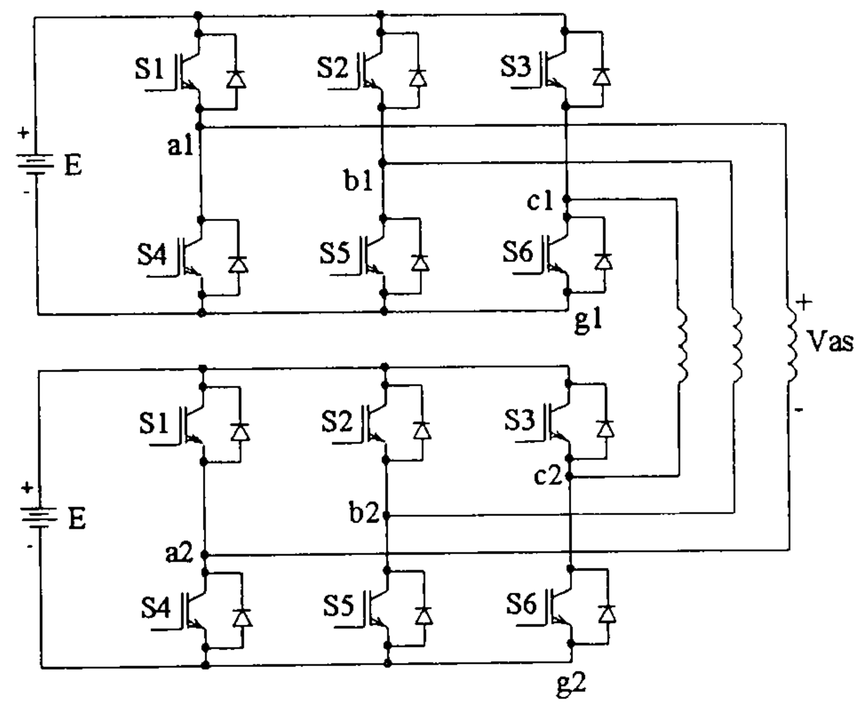


Figure 1.13. Cascaded inverter

3 Modified cascaded multilevel voltage source inverter

The basic structure of this inverter [1.54] is shown in figure (1.14), where every phase has n-full bridges and the voltage sources E_k and E_{k-1} progressively decrease in value by a factor of three. Thus the level number is $2(3^0+3^1+\text{----}+3^{n-1})+1 = 3^n$ for an n full-bridge inverter.

Figure (1.14) is an example of a 9 level (n = 2) inverter. It is possible to obtain 0, $\pm\frac{1}{3}$E, $\pm\frac{2}{3}$E, $\pm$E, and $\pm\frac{4}{3}$E units of output voltage. The main cell switches experience a voltage of E and those of the auxiliary cell experience $\frac{1}{3}$E. The output power of each full bridge is different, as E_1 is charged when the output voltage is $\pm\frac{2}{3}$E. This means that by controlling the output waveform carefully, the capacity requirements of E_1 can

be decreased. Thus E_0 is called the main power source while the others are called assistant power sources. When the system operates at zero power factor, equal charging and discharging in a half cycle balances the assistant power source voltage. Therefore, in theory, such sources could be replaced by capacitors and in practice this indicates that the size of the assistant power transformer could be greatly decreased when the inverter is used to control reactive power. However the size and cost of the main power transformer remains a problem compared to diode clamped and flying capacitor multilevel inverters.

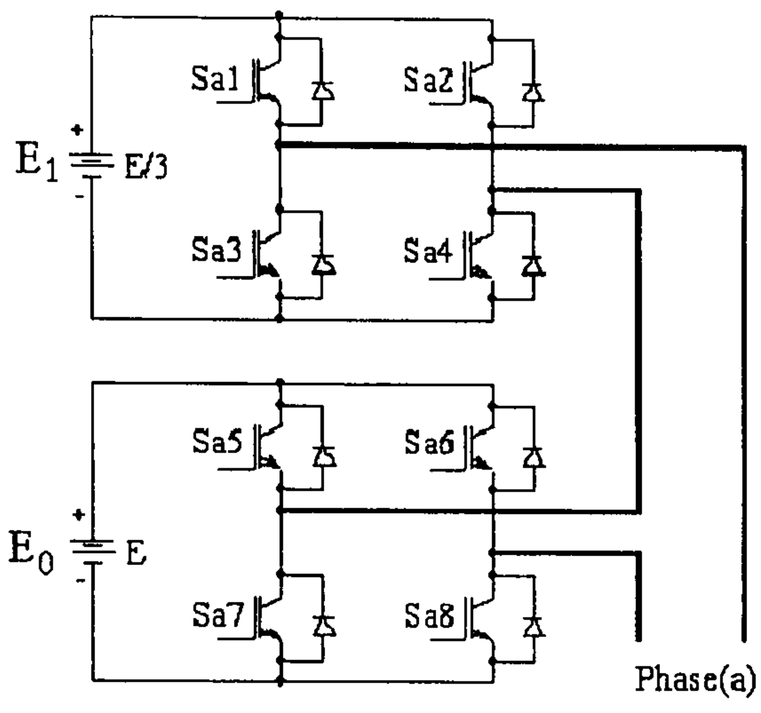


Figure 1.14. A nine-level (n = 2) inverter

4 Modified triple cascade multilevel voltage source inverter

A modified voltage source inverter topology [1.54] is shown in figure (1.15) for a 10 level (n = 2) inverter. The three main full bridges are replaced by a conventional three-phase full bridge. Every phase has n-1 full bridges acting as assistant power sources. The level number of V_{AN}, V_{BN}, and V_{CN} is $(3(2^n)-2)$. It is possible to obtain $\pm\frac{1}{6}V$, $\pm\frac{2}{6}V$, $\pm\frac{3}{6}V$, $\pm\frac{4}{6}V$, and $\pm\frac{5}{6}V$ units for V_{AN}, V_{BN}, and V_{CN}. Compared to the inverter in figure (1.14), only one transformer is needed for the main cell level. Thus the cost and size of the multi level inverter is decreased. Compared to diode clamped and flying capacitor multilevel inverters of the same level, the number of the power devices, size, and cost are decreased.

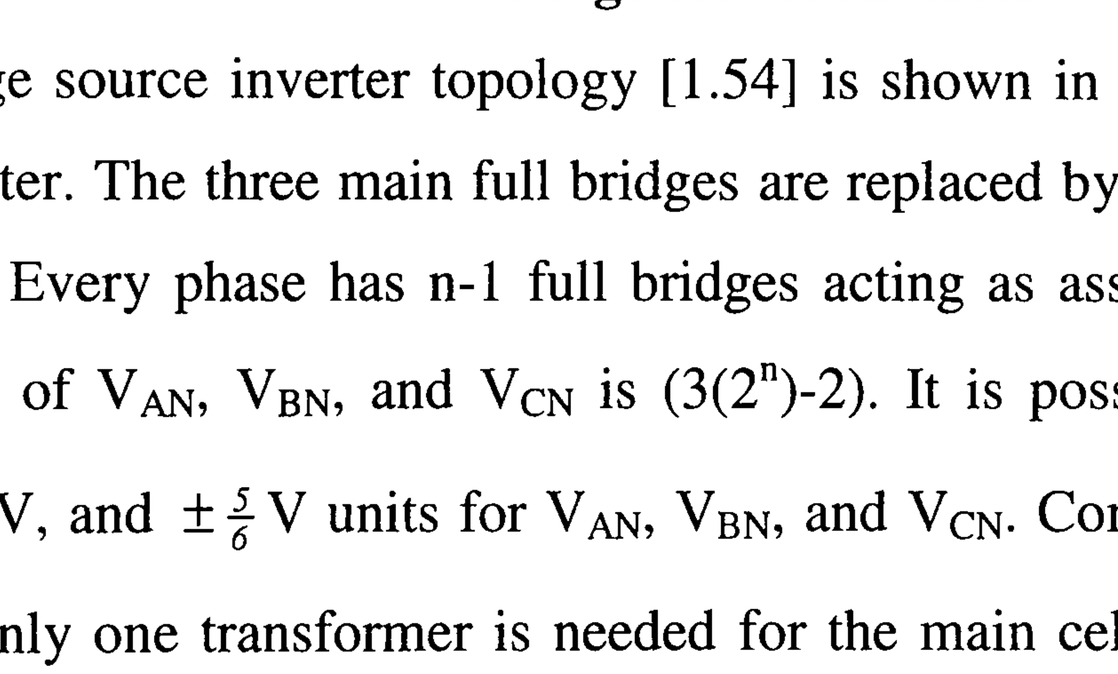


Figure 1.15. A modified ten level (n = 2) inverter

5 Hybrid switches cascaded multilevel inverter

The inverter topology in figure (1.16) is called the hybrid inverter and is derived from the cascaded structure. The cascaded series inverters have different internal DC bus voltages, each using different switching devices (IGCTs and IGBTs) and are modulated differently [1.54],[1.55]. The advantages of the topology are a reduction in switch count (36 down to 24 for a seven level inverter) and more effective usage of the natural switching speed and voltage blocking characteristics of the different silicon switching devices. Furthermore because the number of full bridge inverters required is reduced, the design of the multi-winding transformer for the DC supplies is simplified.

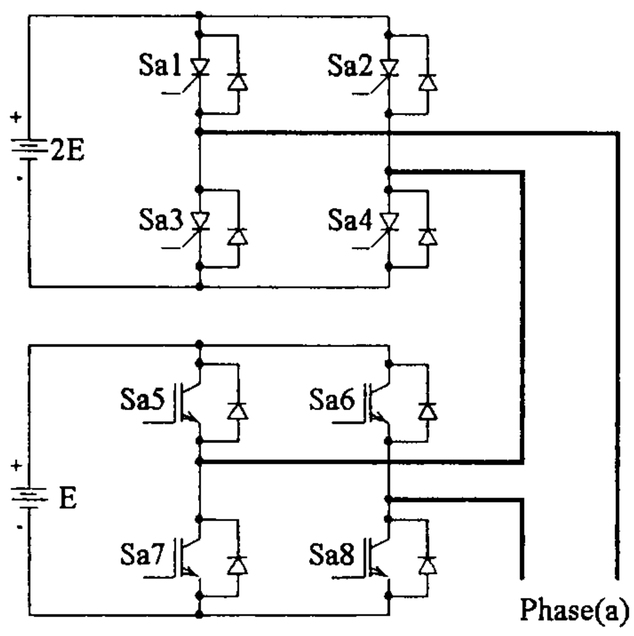


Figure 1.16. Structure of a seven-level hybrid inverter

6 Hybrid switching inverter

A study of the NPC and the cascaded multilevel configurations suggests that desirable features of the multilevel structure are: easy extension to an *m*-level output, fewer isolated DC sources, no voltage balancing problem, and a modular construction [1.57]. Such a structure can be obtained by using a NPC inverter as part of a full-bridge cascaded inverter. This multilevel structure is termed a hybrid multilevel switching inverter (HMSC), reflecting the fact that it is a combination of the NPC and the cascaded inverters. The simplest hybrid multilevel inverter structure is obtained by cascading two full-bridge NPC inverters as shown in figure (1.17). This results in nine output voltage levels, viz., ($\pm 4E$, $\pm 3E$, $\pm 2E$, $\pm E$, and 0). The output current ripple is significantly reduced due to the reduced differential steps at the output. Of the 16 switches available, 8 can be independently controlled to give the nine output voltage levels. Due to the availability of 8 independently controllable switches, more than one switching state results for a given output voltage level. Hence, the effective output switching frequency can be high even though individual device switching frequency is low.

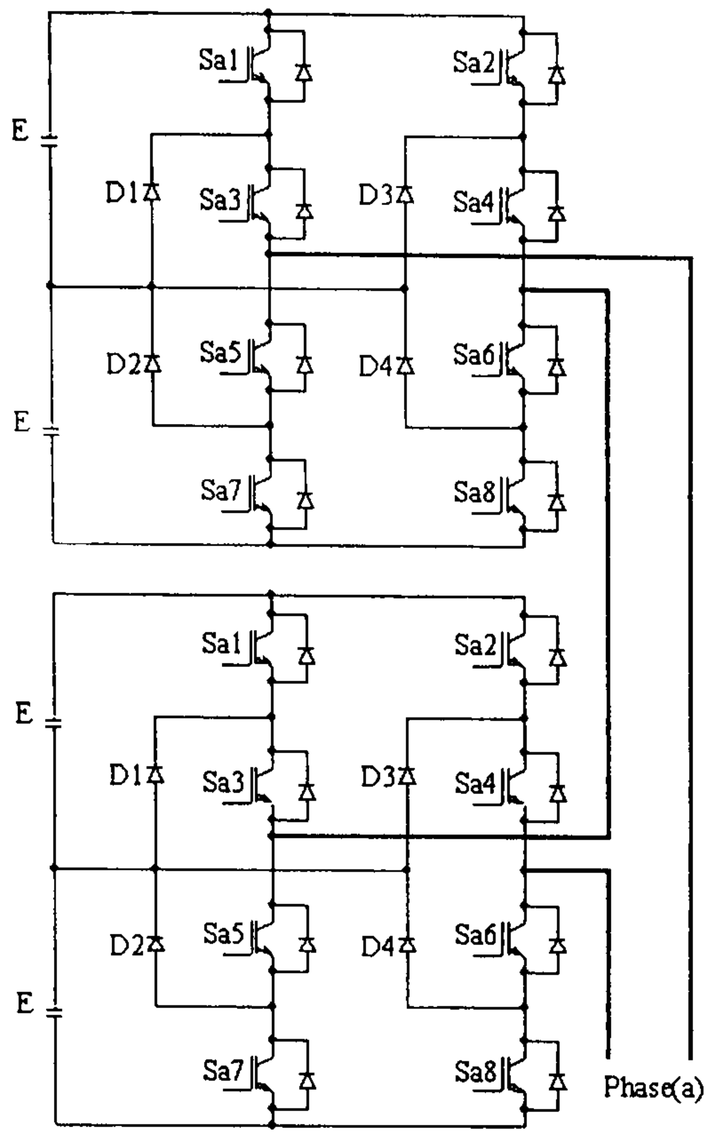


Figure 1.17. Hybrid multilevel inverter

1.5 Series stacked multilevel inverter

The series stacked topology uses a number of standard full-bridge inverters as shown in figure (1.18) for the two-cell series stacked case. Straight forward control and inherent balancing of the series stacked topology make it an ideal solution for high voltage applications. It is ideally suited for distributed control, because optimal control can be implemented with only local measurements and parameters [1.58]. The version in figure (1.18) consists of two standard full-bridge inverters with series stacked DC bus capacitor banks. The two inverter outputs are filtered and connected to identical transformer primaries. The total power rating of the inverter is equal to the sum of the power ratings of the individual full-bridge inverters. Although this topology requires an output transformer, there are a number of applications where this transformer forms an inherent part of the overall system. One such application is in series injection power quality equipment, where this topology has a number of advantages:

i. It does not require extra components like clamping diodes or flying capacitors. It exploits the presence of the injection transformer;
ii. It has excellent DC balancing properties; and
iii. It makes use of standard full-bridge inverter building blocks that can be readily purchased.

One key consideration when designing multilevel inverters is the balancing of the capacitor voltage. The balancing theory of two-cell inverters is discussed in detail in [1.59]. The balancing theory of the three-cell inverter is almost identical to that for the

two-cell case. The theory has not been extended to more than three cells. This topology is mainly applicable to applications on a supply (11 kV) where no input transformer is used.

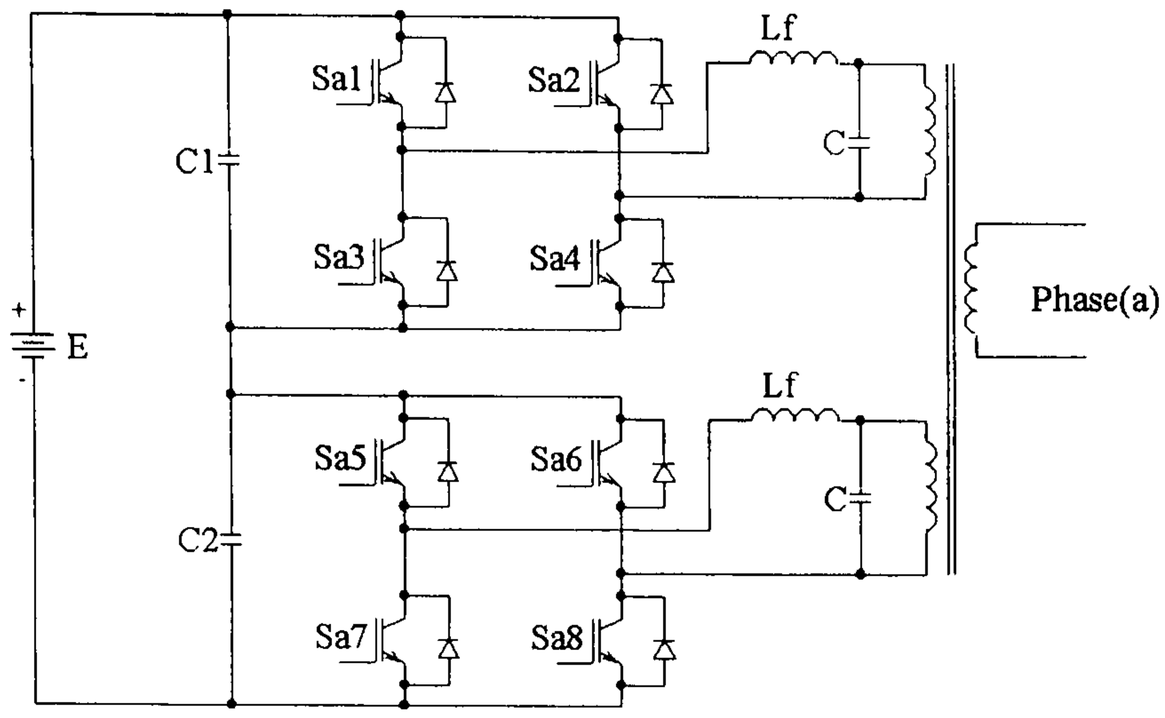


Figure 1.18. Series stacked multilevel inverter

1.6 Generalized multilevel inverter

The generalized multilevel inverter topology in figure (1.19) was presented by F. Z. Peng [1.60]. Existing multilevel inverters, such as diode-clamped and capacitor-clamped multilevel inverters, can be derived from this generalized inverter topology. Moreover, the generalized multilevel inverter topology provides a true multilevel structure that can balance each DC voltage level automatically, with any number of levels, whether performing active or reactive power conversion, without any assistance from auxiliary circuits. Thus in principle, it is a complete multilevel topology that embraces all existing multilevel inverters. From this generalized topology, several new multilevel inverter structures can be derived [1.60].

1.6.1 Operating principle

Figure (1.19) shows the generalized multilevel inverter topology phase leg, where each switching device, diode, or capacitor voltage rating is E, i.e., *(1/m-1)* of the dc-link voltage. Any inverter with any number of levels including the conventional two level-inverter, can be obtained from the generalized topology. For example, the two-level inverter is the shaded circled in figure (1.19). The five-level circuit in figure (1.19) is used to explain the operating principle and analysis of the circuit. The switches Sp1 to Sp4 and Sn1 to Sn4 and diodes Dp1 to Dp4 and Dn1 to Dn4 are the main devices used to produce the desired voltage waveforms. The remaining switches and diodes are for clamping and balancing capacitor voltages. All voltage levels are self-balanced through the clamping switches and clamping diodes.

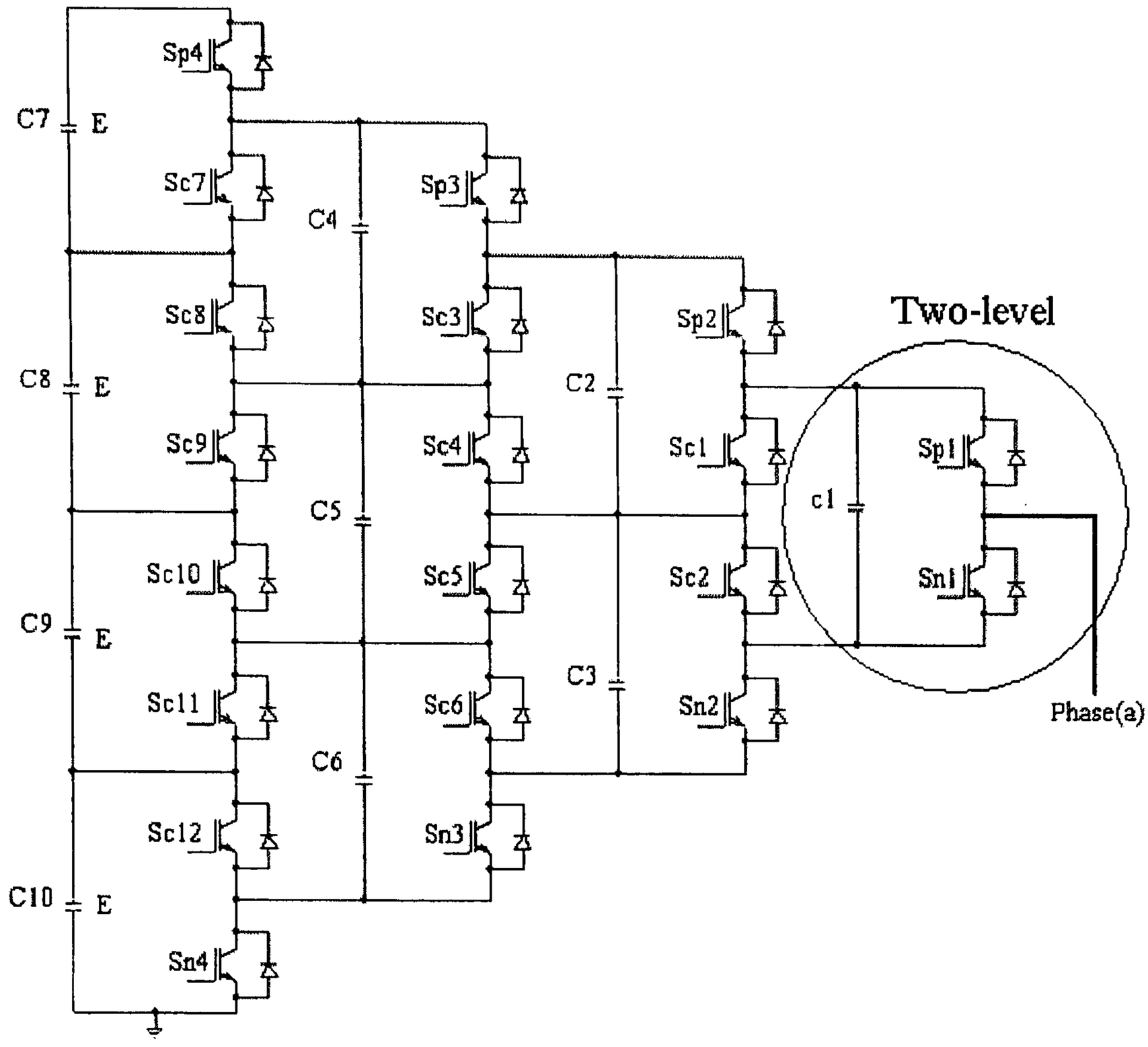


Figure 1.19. Generalized inverter topology (one phase leg).

For example, to obtain a voltage of E, there are four alternatives as in Table 1.3:

i. Switches Sp1, Sn2, Sn3, and Sn4 are on, figure (1.20a)

ii. Switches Sn1, Sp2, Sn3, and Sn4 are on, figure (1.20b)

iii. Switches Sn1, Sn2, Sp3, and Sn4 are on, figure (1.20c)

iv. Switches Sn1, Sn2, Sn3, and Sp4 are on, figure (1.20d)

The following switching rules apply for voltage balance:

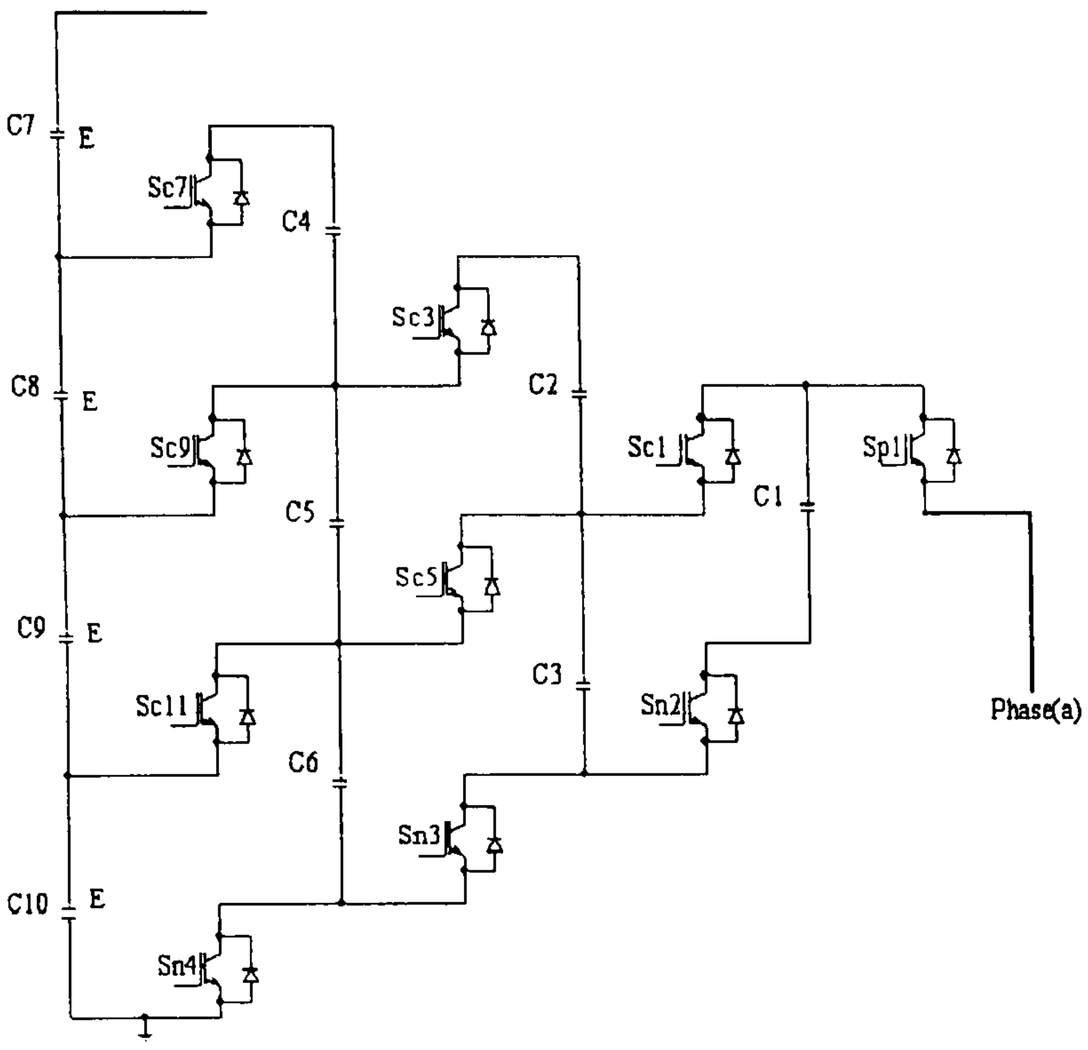
i. each switch pole is an independent switching unit;

ii. any adjacent switches of each switch pole are complementary, (i.e., if one is on the other is off and vice versa); and

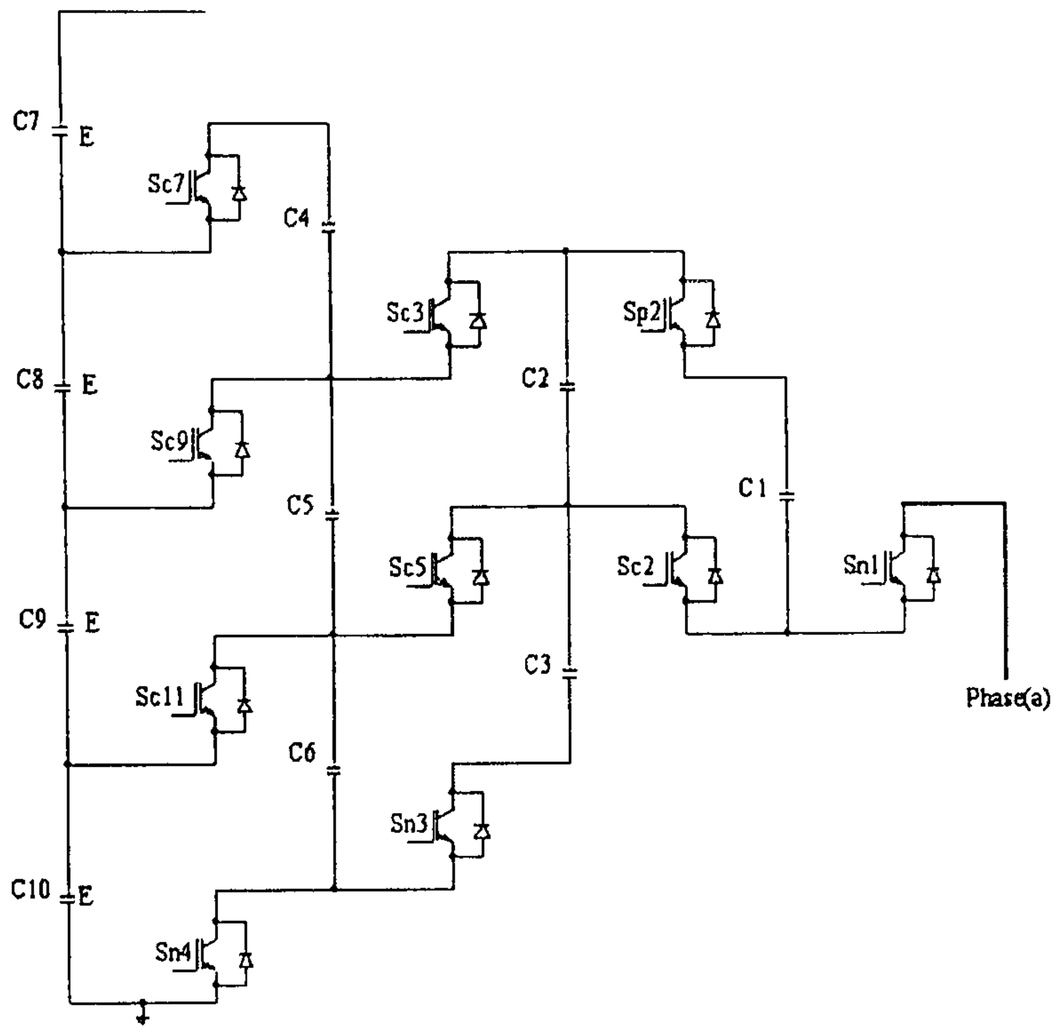
iii. if any switch's state is determined or known, then the state of the other switches of the pole are automatically specified because of the complementary rule.

For example in figure (1.20a), the hidden switches are off, therefore capacitors C_1, C_3, C_6, and C_{10} are connected in parallel, as well as C_2, C_5, and C_9. In figure (1.20b), capacitors C_3, C_6, and C_{10} are connected in parallel, as well as C_1, C_2, C_5, and C_9. Table 1.3 summarizes the switching states to generate the voltage levels 0, E, 2E, 3E, and 4E. From Table 1.3 it can be seen that it is possible to obtain each voltage level by a

combination that can charge or discharge all capacitors. Appropriate use of these states will ensure capacitor voltage balance. Parts a to c of figure (1.21) indicate how the diode clamped, flying capacitor, and mutual diode clamped inverters can be derived from the generalized multilevel inverter.



(a)



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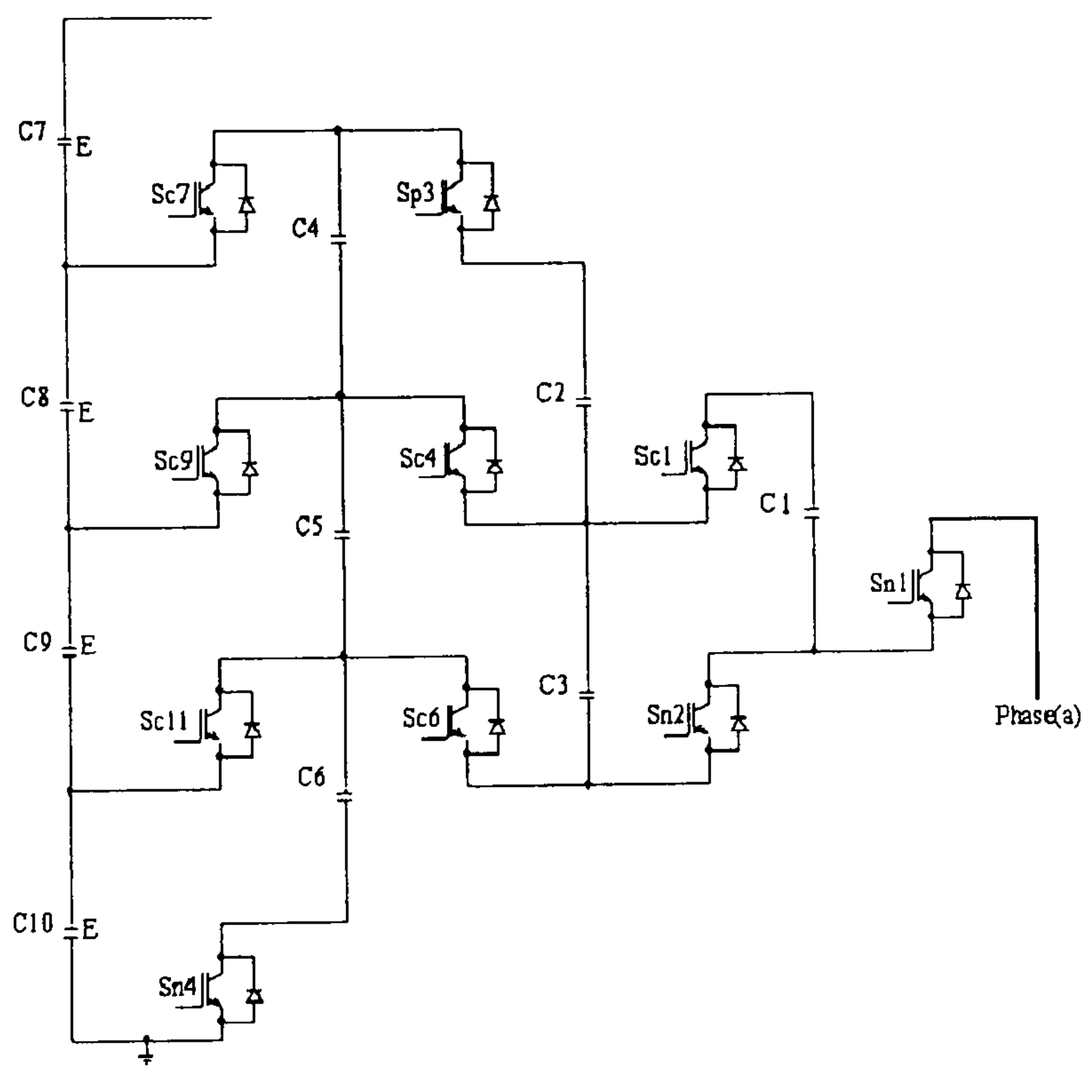

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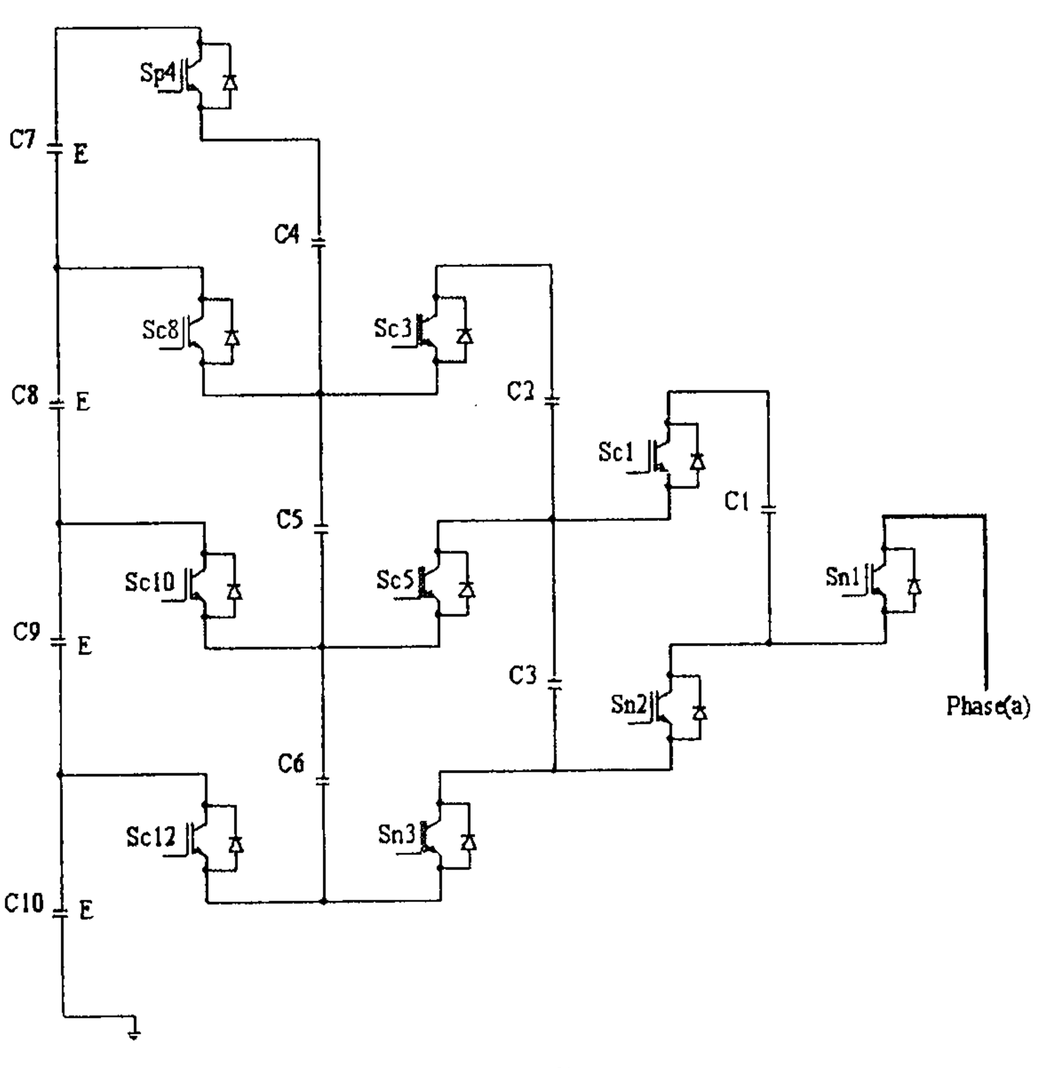


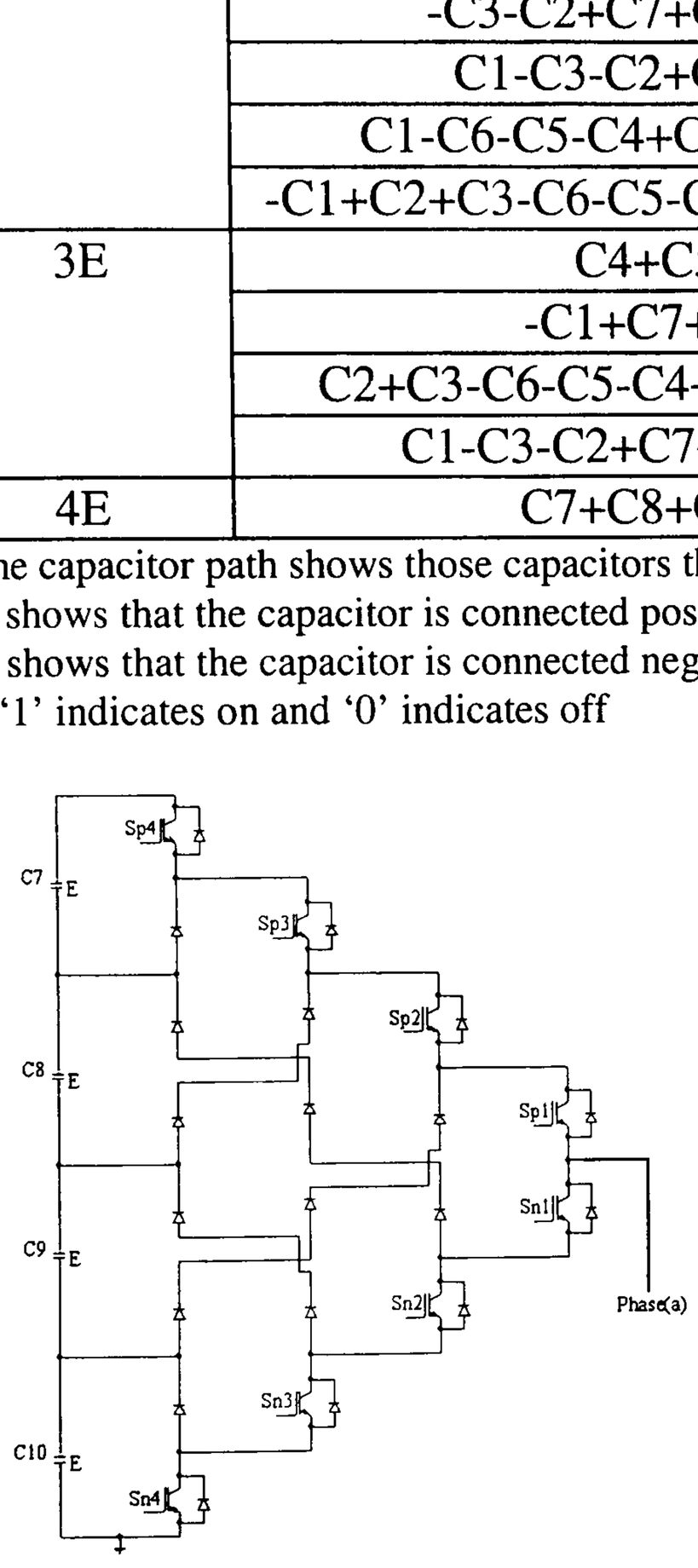
(d)

Figure 1.20. Switching state to balance capacitor voltages and to produce $V_o = E$

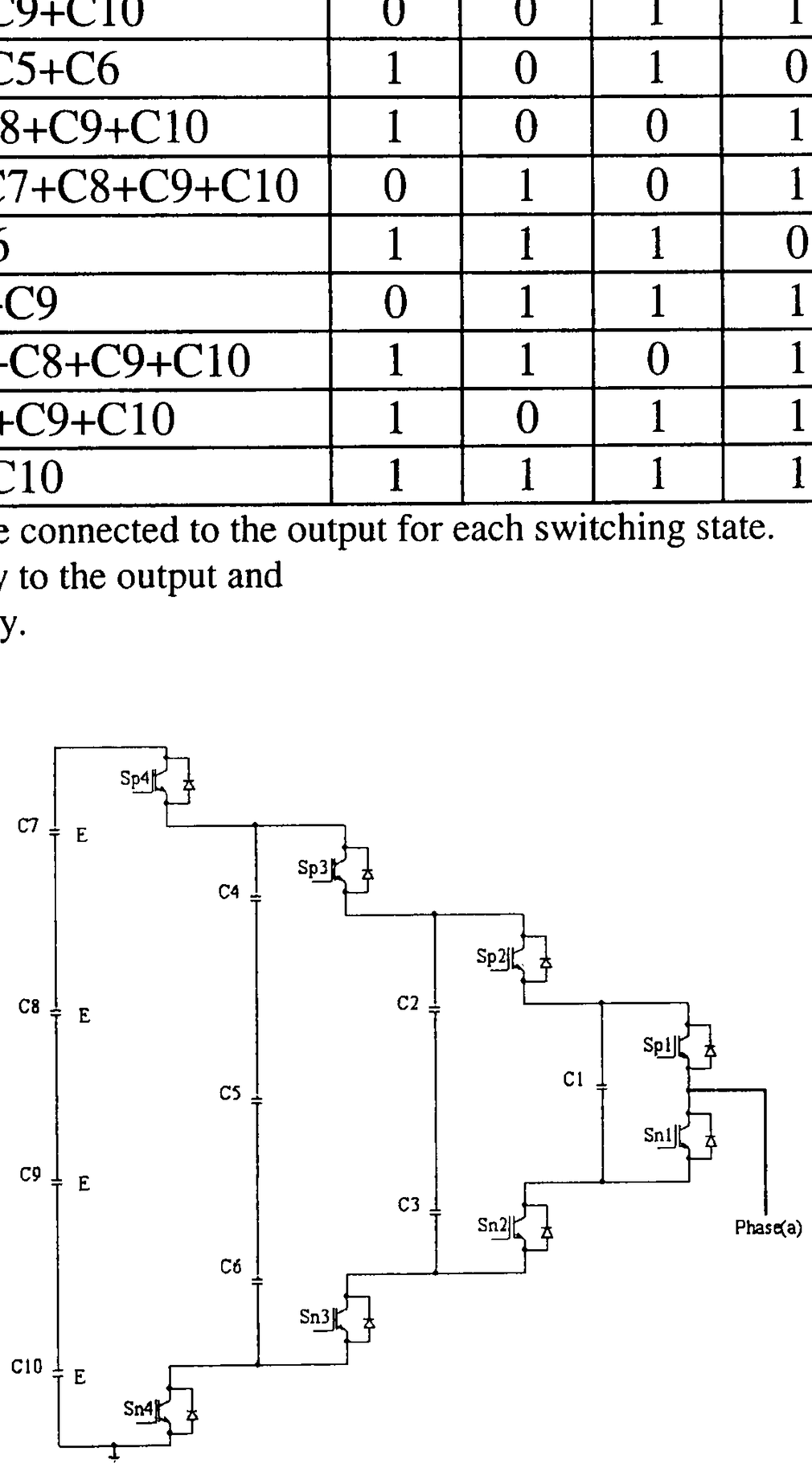
Table 1.3. Switching states to produce $V_o = 0$, E, 2E, 3E, and 4E voltage levels

Output voltage	Capacitor path	Switch states			
		Sp1	Sp2	Sp3	Sp4
0	None	0	0	0	0
E	C1	1	0	0	0
	-C1+C2+C3	0	1	0	0
	-C3-C2+C1+C5+C6	0	0	1	0
	-C6-C5-C4+C7+C8+C9+C10	0	0	0	1
2E	C2+C3	1	1	0	0
	-C1+C4+C5+C6	0	1	1	0
	-C3-C2+C7+C8+C9+C10	0	0	1	1
	C1-C3-C2+C4+C5+C6	1	0	1	0
	C1-C6-C5-C4+C7+C8+C9+C10	1	0	0	1
	-C1+C2+C3-C6-C5-C4+C7+C8+C9+C10	0	1	0	1
3E	C4+C5+C6	1	1	1	0
	-C1+C7+C8+C9	0	1	1	1
	C2+C3-C6-C5-C4+C7+C8+C9+C10	1	1	0	1
	C1-C3-C2+C7+C8+C9+C10	1	0	1	1
4E	C7+C8+C9+C10	1	1	1	1

*The capacitor path shows those capacitors that are connected to the output for each switching state.
'+' shows that the capacitor is connected positively to the output and
'-' shows that the capacitor is connected negatively.
** '1' indicates on and '0' indicates off



(a)



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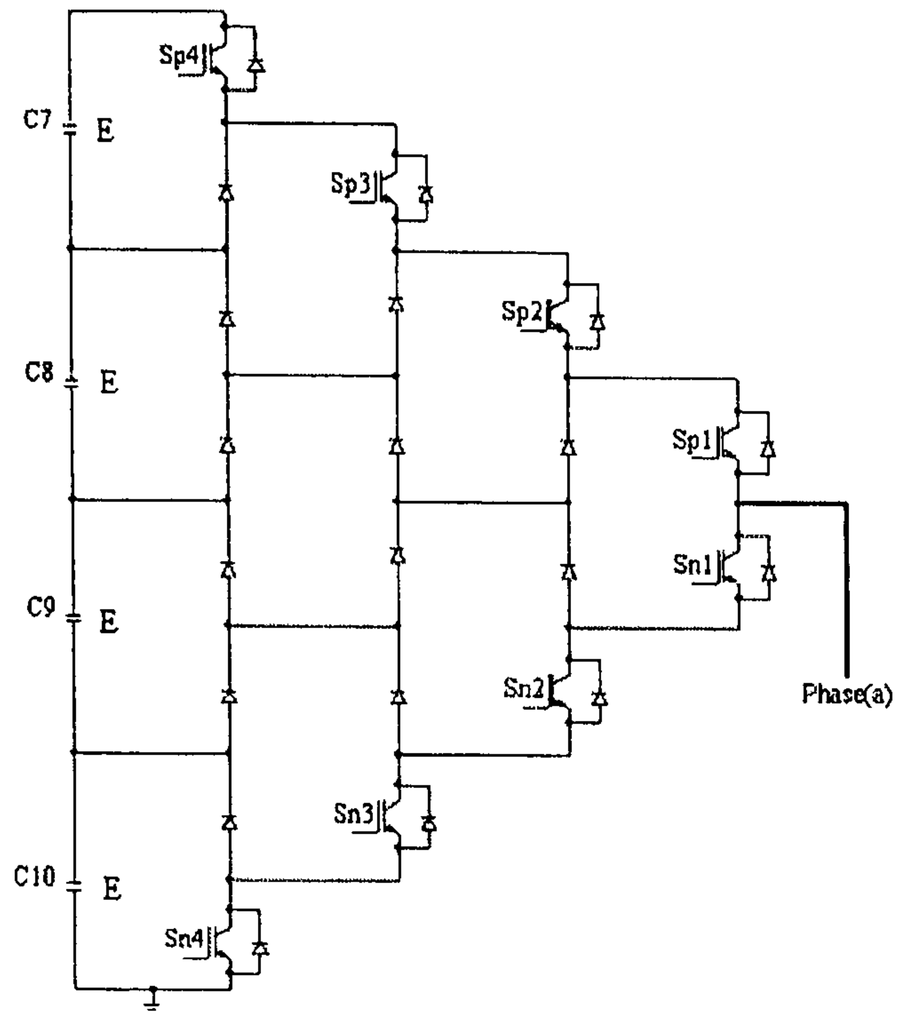

(c)

Figure 1.21. Generalized multilevel inverters:
(a) diode clamped, (b) flying capacitor, and (c) mutual diode clamped

1.7 Multilevel inverter applications

The multilevel inverter has many advantages. It reduces the output total harmonic distortion due to the increase in voltage levels. Also, it has the ability to be used above the rated voltage of the semiconductor devices, avoiding the need to series connect devices. Due to these advantages, there are many applications for the multilevel inverter:

- Static VAR compensation [1.19],[1.61]-[1.78];
- Active power filtering [1.79],[1.80];
- Drives [1.20],[1.28],[1.81]-[1.96];
- Traction [1.6],[1.7],[1.97]-[1.99];
- AC power supply applications [1.100]-[1.106];
- Power amplifiers [1.107],[1.108];
- DC transmission [1.109];
- Renewable energy systems [1.110]-[1.112];
- Unified power flow control (UPFC) [1.113],[1.114];
- Universal power conditioning [1.115],[1.116];
- AC/DC/AC inverters [1.117];
- Uninterruptible supplies (UPS) [1.118];
- X-Ray generators [1.119];
- Plasma stabilization [1.9];
- Satellites [1.52]; and
- Voltage dip compensation [1.120].

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Chapter 2

Multilevel Modulation

Multilevel inverters can be classified according to their output waveform control technique, namely stepped wave inverters or pulse width modulated (PWM) inverters. PWM inverters have gained popularity over stepped wave inverters due to their inherent advantages. In general PWM inverters should meet the following basic requirements [2.1]:

i. The number and magnitude of lower order harmonics should be small;

ii. Inverter weight, volume, and losses should be small; and

iii. PWM techniques should be simple and easy to be implemented on-line.

PWM techniques can be classified as single pulse PWM or multiple pulse PWM. Single pulse PWM inverters generate only one pulse per half-cycle [2.1]. Multiple pulse PWM inverters have inherent advantages over single pulse PWM inverters. Various PWM control schemes for multilevel inverters have been developed and analysed [2.2]-[2.18] so as to control the fundamental voltage and eliminate certain lower order output harmonics. With the multiple pulse PWM technique, the width of each pulse is controlled so as to eliminate lower order harmonics and control the fundamental voltage amplitude [2.1]. Multiple pulse PWM is pursued due to its advantages, and when used in conjunction with an inverter, the inverter is termed a PWM inverter. Figure (2.1) shows the different types of multilevel control techniques

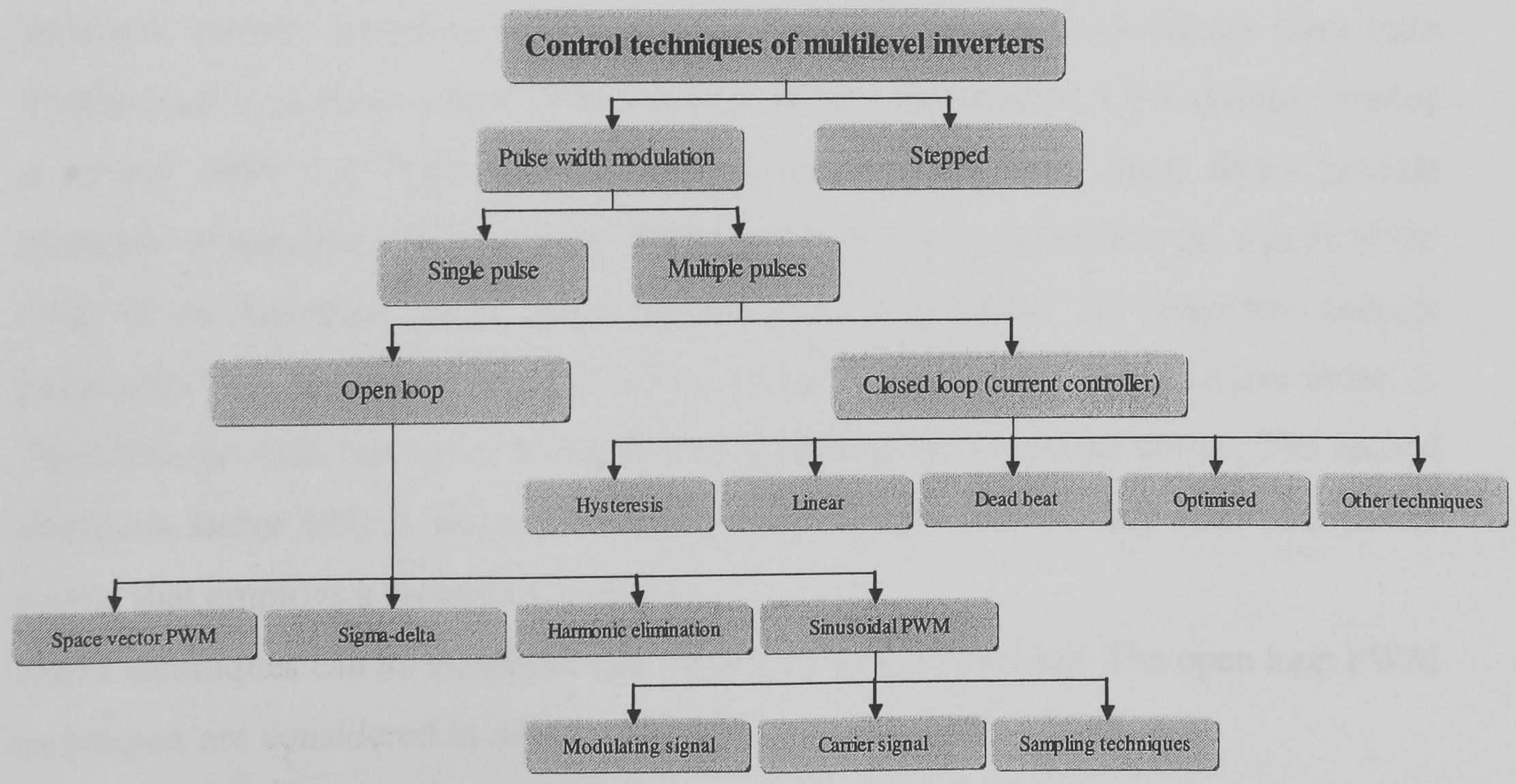


Figure 2.1. Multilevel inverter control techniques

2.1 Medium power PWM voltage source inverter

2.1.1 Features of the medium power PWM voltage source inverter

Among the other competitor converters, the PWM VSI has the following features [2.19]:

i. Good dynamic response compared to the load commutated inverter;
ii. Ride through of supply voltage dips compared to matrix converters; and
iii. Reduced cabling and transformer costs compared to cycloconverters.

2.1.2 Harmonic distortion factors

In most applications, varying the modulation index controls inverter output power. It is therefore important to investigate the quality of the various inverter waveforms for all modulation indices (linear and over modulation regions). Two harmonic distortion factors (DF) for first and second order AC filtering are defined, as well as total harmonic voltage distortion (THD). They are defined as follows:

$$THD = \frac{1}{V_1}\sqrt{\sum_{n\neq 1} V_n^2} \tag{2.1}$$

$$DF1 = \frac{1}{V_1}\sqrt{\sum_{n\neq 1}\left[\frac{V_n}{n}\right]^2} \tag{2.2}$$

$$DF2 = \frac{1}{V_1}\sqrt{\sum_{n\neq 1}\left[\frac{V_n}{n^2}\right]^2} \tag{2.3}$$

It should be noted that the factors are defined in such a way as to reflect actual levels of harmonic current distortion experienced in real applications. Such factors have been widely used to evaluate other PWM schemes [2.20], for instance, UPS systems employ a second order L-C filter between the inverter and the load. Such filters provide harmonic attenuation which is approximately inversely proportional to the square of the order of the harmonic, n. In motor applications, for instance, the respective leakage inductance provides first order attenuation of each harmonic by its respective order, n. Therefore the first distortion factor DF1 is applicable to AC motor drives. The second distortion factor DF2 is relevant to UPS inverter stages and for any other AC power supply that employs a second order filter.

PWM techniques can be classified into open loop and closed loop. The open loop PWM techniques are considered in detail.

2.2 Open loop modulation

For a three-phase multilevel inverter, suitable harmonic elimination techniques are described in [2.21]. In [2.22], a harmonic optimisation algorithm is proposed, and many pulse width modulation (PWM) techniques have been proposed in the technical literature [2.1]-[2.33]. Moreover, modulation techniques based on the space vector representation are widely used. This makes it possible to synthesize algorithms which are particularly suited for digital signal processor (DSP) implementation. Researchers have focused attention on the generalization of modulation algorithms and techniques for *m*-level inverters [2.29],[2.30],[2.32],[2.34]. Voltage vectors allow a precise modulation visualization for three phase inverters, and highlight the usefulness of DSP-based algorithms. Open loop modulation can be classified into:

- Space vector (SVPWM);
- Sigma delta (SDM);
- Selective harmonic elimination (SHE); and
- Sinusoidal PWM (SPWM).

2.2.1 Space vector modulation

Compared to sinusoidal triangular techniques, space vector PWM waveforms, as well as third harmonic injection, are shown to have advantages with respect to ease of generation, reduced motor losses, and motor current zero crossing distortion [2.35]. In multilevel inverters, space vector modulation (SVM) [2.36]-[2.53] identifies each switching state of the multilevel inverter as a point in the complex α-β space. Then a reference phasor rotating in the α-β plane at the fundamental frequency is sampled within each switching period, and the nearest three inverter switching states are selected with duty cycles calculated to achieve the same volt-second average as the sampled reference phasor. This directly controls the inverter line-to-line voltages, and implicitly develops the phase leg voltages. Recent work has shown how to do these calculations for a general *m*-level diode clamped inverter [2.52], but gives no insight into the optimal sequence of space vector states or the method's applicability to other multilevel inverter topologies. Previous work has shown that space vector and carrier modulation of two-level inverters produce identical space vector sequences despite their apparent differences [2.41].

Figure (2.2) shows the space vector diagram for a 3-level diode clamped system, where each digit of the space vector identifier represents the voltage level to which the A, B, and C phase legs are respectively switched. Note that some switch states are redundant

and create the same space vectors. The task of selecting the optimum set of space vectors for a given reference phasor was solved by Celanovic et al. [2.52]. The method uses a linear coordinate transformation and identified that the harmonic profile of the overall switched waveform is minimized when the nearest space vectors are used. However, this solution does not identify how to sequence or place these three nearest space vectors in the (half carrier equivalent) switching period so as to minimize the total number of switching transitions and fully optimise the harmonic profile of the output voltage. For a three-phase inverter, the minimum number of switch transitions in one switching cycle, under continuous modulation, is three (i.e. one per phase leg), so that the inverter cycles through 4 switched states in each switching period. At least the first and the last of these must be a redundant space vector state if only the three nearest space vectors are to be used (e.g. 101-201-211-212)

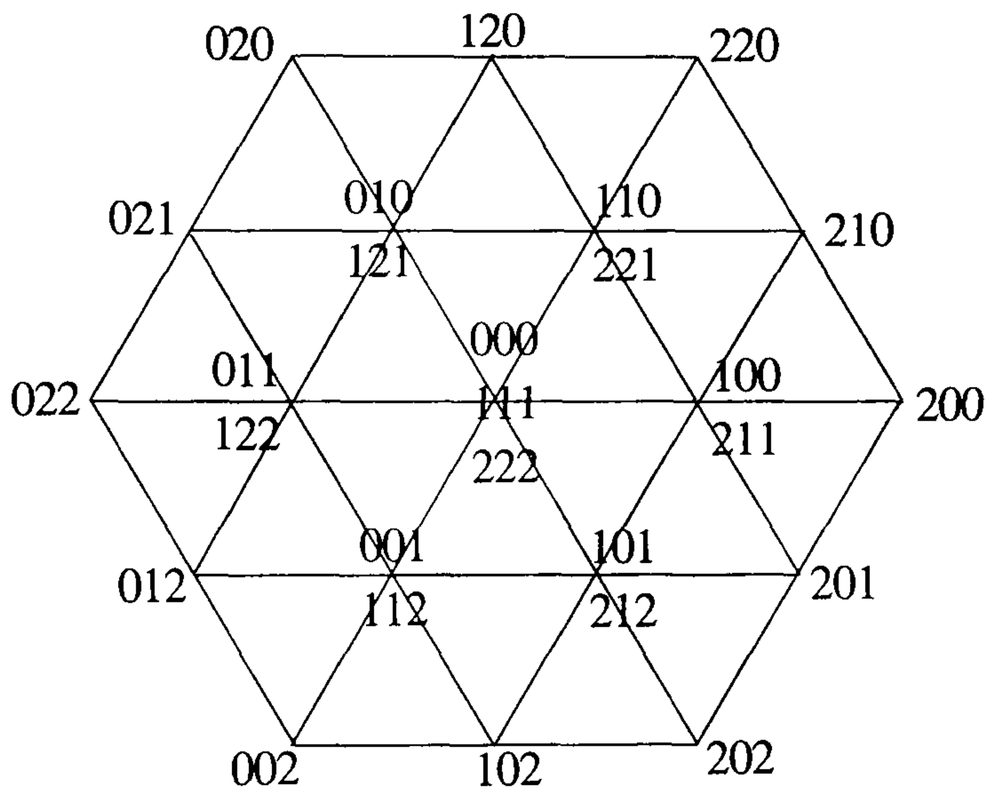
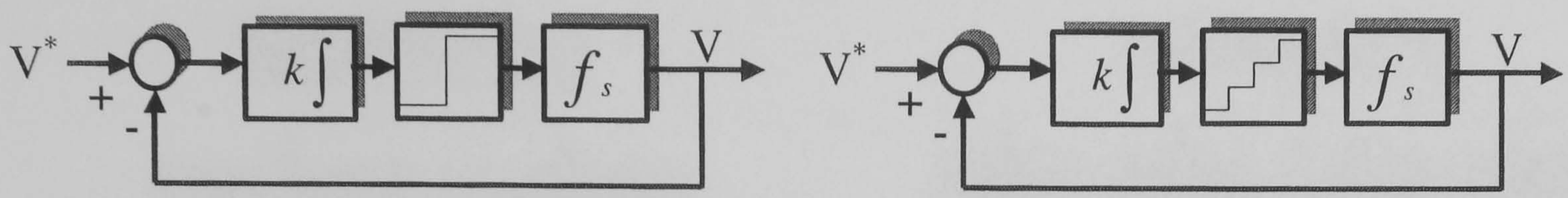


Figure 2.2. Space vector states for three-level NPC inverter

2.2.2 Multilevel sigma delta modulation

The technique of sigma delta modulation (SDM) has been employed successfully as a tool to synthesize voltage waveforms [2.54]-[2.63] in discrete pulse modulated systems such as a resonant DC link inverter. An SDM schematic for a conventional two level inverter is shown in figure (2.3a). V^* represents the desired output voltage, V is the synthesized output voltage, and f_s represents the system sampling frequency. SDM operates to equalize the integral of the continuous input demand and that of the discrete two-level output waveform. SDM can be extended to synthesize a multilevel waveform by replacing the binary quantizer in the forward path by an N-level quantizer, corresponding to the number of levels in the multilevel inverter, as shown in figure (2.3b). The multilevel sigma delta modulator (MLSDM) also operates to equalize integrals of the command and the output waveforms. Modulator design tasks involve the selection of integrator gain K and sampling frequency f_s, to obtain high fidelity

waveform synthesis. A higher sampling frequency results in a higher bandwidth controller, which results in better performance. But the upper bound on the frequency is restricted by the switching capability of the inverter switches. Hence the choice of f_s is dictated by power circuit considerations.



(a) (b)

Figure 2.3. Block diagram of:
(a) two-level sigma delta modulator and (b) multilevel sigma delta modulator

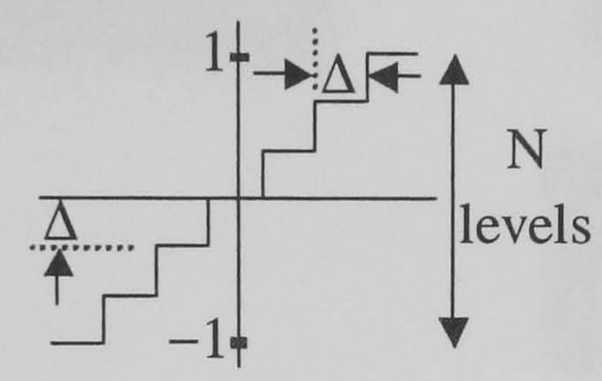


Figure 2.4. Static transfer characteristics of the normalized uniform multilevel quantizer

2.2.3 Selective harmonic elimination modulation

The generalized harmonic elimination technique to selectively eliminate harmonics generated by switching voltage waveforms was suggested in 1973 by Patel and Hoft [2.64],[2.65]. It has been widely used in two-level inverters [2.64]-[2.75] and multilevel inverters [2.76]-[2.79]. The technique suffers from the following disadvantages.

- The initial guess is important in reducing the number of iterations for faster convergence.
- The switching angles have to be stored with adequate resolution. The storage (memory) space, depends upon the number of harmonics to be eliminated, carrier to modulating frequency ratio, and the operating range of the fundamental
- Due to the above reasons, the technique is mainly restricted to off-line use. On-line implementation is rather difficult though desirable in many applications.

For the multilevel inverter, there are two different approaches. The first uses multiple pulses for each level to eliminate certain harmonics as discussed in [2.21]. The second uses only one pulse per half cycle as discussed in [2.80], assuming that the number of levels is high enough to eliminate the required number of harmonics.

2.2.4 Classification of PWM techniques

PWM techniques can be classified, as shown in figure (2.5), according to:

i. Sampling technique;
ii. Carrier signal; and
iii. Modulating signal.

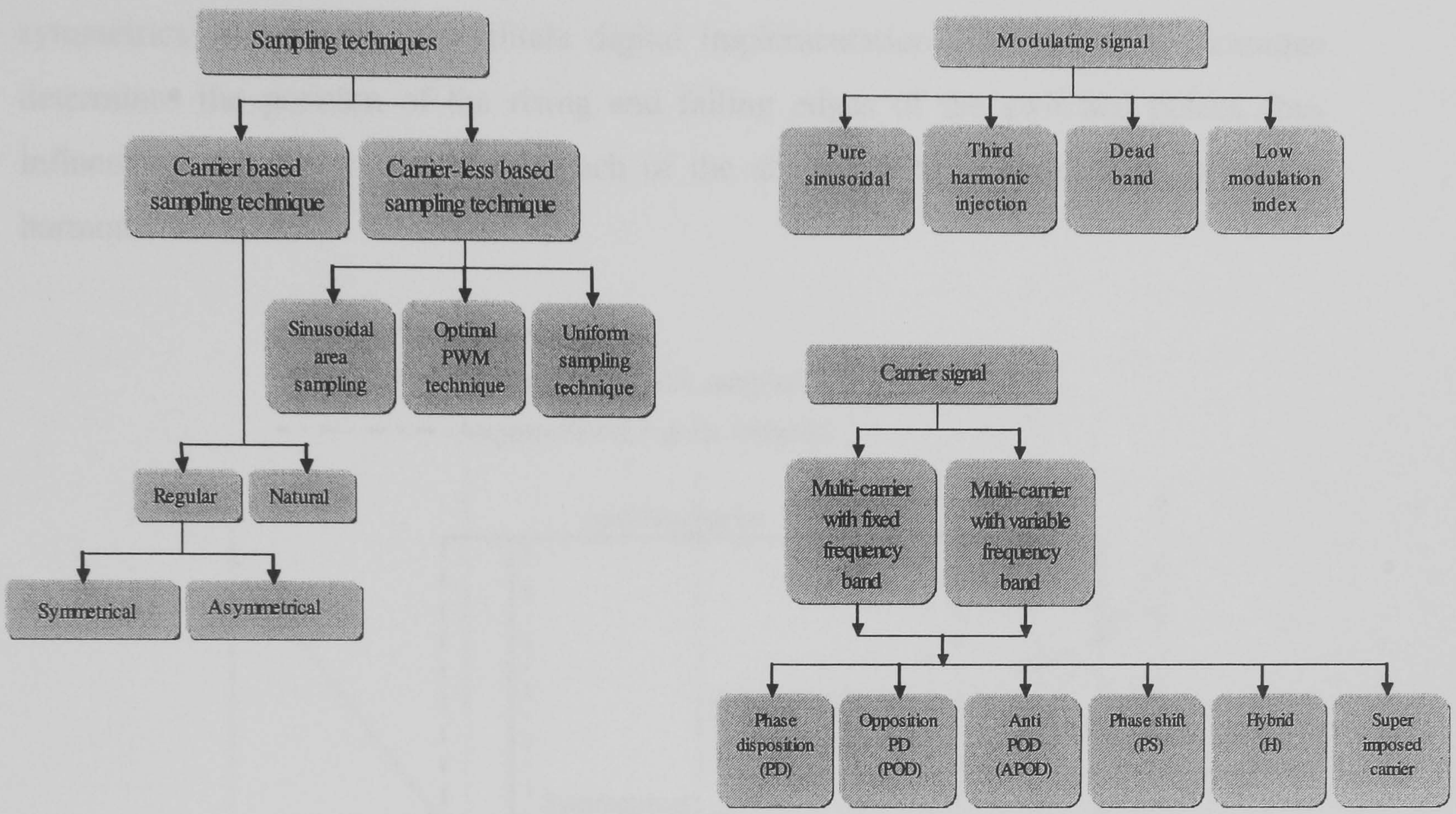


Figure 2.5. Classification of PWM techniques

i. Sampling techniques

The sampling technique can be classified into:

i. Carrier-based sampling and
ii. Carrier-less sampling.

(a) Carrier based sampling technique

The sampling technique may be natural, symmetric regular sampled or asymmetric regular sampled [2.81], [2.82]. Figure (2.6) illustrates the influence that the sampling technique can have on the switched output waveform. The natural sampling technique [2.24] was the first widely accepted PWM technique where a triangular wave carrier signal is compared with a sinusoidal reference wave known as the modulating wave. The resultant intersection instants form the PWM control signal for the inverter where switching is performed on both carrier slopes. Hence, the pulse width varies at both edges, and the resulting process is called the double-edge natural sampling PWM. Generally, both the reference and the carrier waves are synchronized. The ratio of the

carrier to the modulating reference frequency determines the number of lower order harmonics to be eliminated or minimized. The carrier's peak amplitude is constant; whilst the modulating signal amplitude (and frequency) is varied so as to vary the inverter output terminal voltage. Regular sampled PWM holds the reference waveform fixed during a half or full carrier interval, (respectively termed asymmetrical and symmetrical sampling), to facilitate digital implementation. The sampling technique determines the position of the rising and falling edges of the switched pulses, thus influencing the spectra produced. Each of the above PWM variations has particular harmonic benefits.

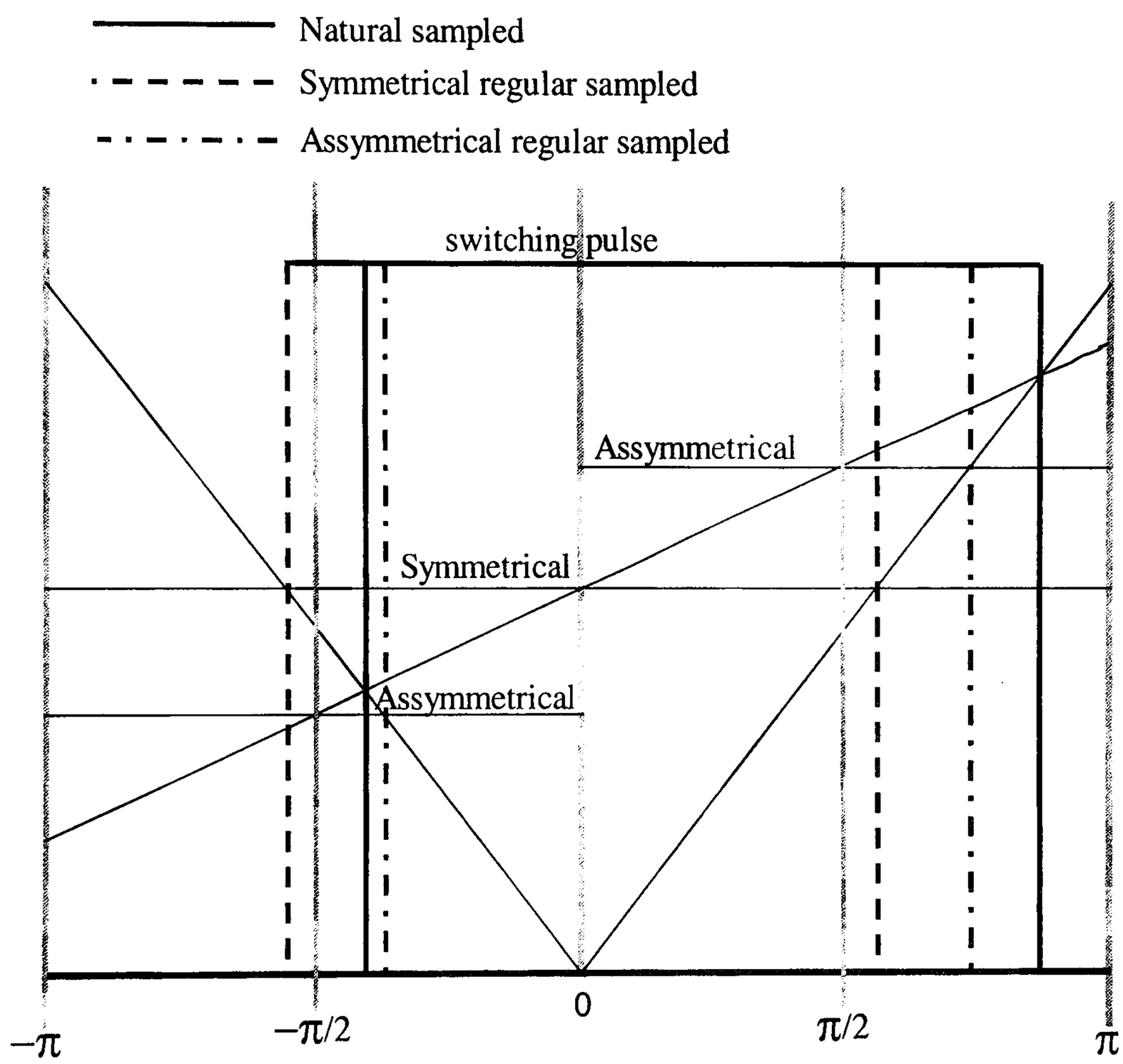


Figure 2.6. Position of rising and falling edges resulting for three common sampling techniques

(b) Carrierless sampling technique

Carrierless sampling techniques can be classified into:

- Uniform area sampling;
- Sinusoidal area sampling; and
- Optimal sampling.

(1) Uniform area sampling technique

The uniform sampling technique [2.25]-[2.27] is based on the sample and hold principle, where the sampling points are fixed at every positive going peak, or sometimes, at every positive and negative peak of carrier frequency. The reference waveform is sampled and held or simulated analytically at every sampling point, then compared with the carrier to generate the PWM control signal. This technique is easy to implement on-line using a DSP or digital circuitry.

The uniform area technique was developed for the neutral point clamped inverter, in which the area sampling is performed uniformly. Each pulse width of the PWM pattern is varied proportionally to the area covered by uniformly (evenly) divided segments of the sine wave being simulated [2.23]. The area of each uniformly divided segment (carrier period) is computed, and the pulse width during each carrier period is fixed proportional to the area under the segment. This process is repeated only up to 90 degrees during the positive half cycle of the modulating signal. The rest of the PWM pulses are fixed by reversing the count from 90 to 180 degrees, counting up between 180 and 270 degrees, and again down from 270 to 360 degrees. The uniform area sampling technique can be subdivided into symmetrical and asymmetrical.

(2) Sinusoidally sampled PWM technique

A number of PWM techniques were developed to realize an output sinewave voltage. The sinusoidally sampled area computation technique was designed to improve motor performance at relatively high frequency or to reduce the filter size for a three-phase, four-wire-system.

The modulating sine wave is equally divided, i.e. all the reference points are equally separated, but with this technique, each reference point or segment is chosen in a sinusoidal fashion, as shown in figure (2.7a), (2.7b). There are two sampling types, symmetrical and asymmetrical sinusoidal sampling.

(3) Optimal PWM technique

The optimal PWM switching technique [2.28] can be generated depending on certain performance criteria, which may eliminate certain harmonics. The patterns have to be stored in memory in the form of a look-up table

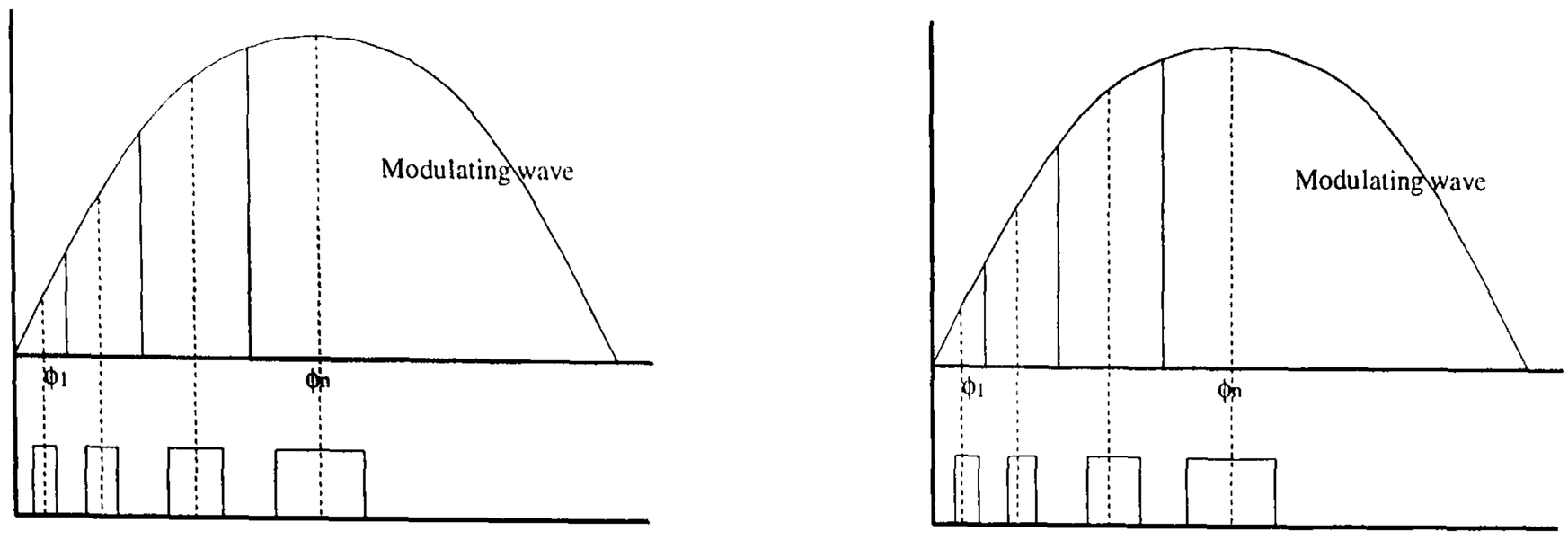


Figure 2.7. (a) Symmetric sinusoidally sampled PWM technique
(b) Asymmetric sinusoidally sampled PWM technique

ii. Carrier signal

Sinusoidal PWM can be classified according to the carrier:

- Multi-carrier fixed frequency band
- Multi-carrier variable frequency band

This section only explains fixed frequency band PWM, and multi-carrier fixed frequency band PWM is referred to as a multi-carrier PWM technique. Fixed frequency band carrier can be classified into:

- Phase disposition (PD);
- Phase opposition disposition (POD);
- Alternative phase opposition disposition (APOD);
- Phase shift (PS);
- Hybrid (H); and
- Superimposed carrier (SIC).

Multi-carrier PWM techniques

Multi-carrier PWM techniques entail the natural sampling of a single modulation or reference waveform, typically sinusoidal, with carrier signals, typically triangular waveforms [2.83]. They can be categorized as follows:

1. Carrier disposition methods where the reference is sampled through a number of carrier waveforms displaced by contiguous increments of the reference waveform amplitude (PD, POD, APOD)
2. The sub-harmonic PWM method with multiple carriers phase shifted (PS)
3. The hybrid carrier disposition method incorporates carriers displaced in time, where a reference is sampled through a combination of the aforementioned techniques (H).
4. The superimposed carrier technique (SIC)

For each technique the following parameters introduce a degree of freedom:

- The frequency modulation index, m_f, with $m_f = f_c/f_o$, where f_c is the triangle frequency and f_o is the modulating frequency.
- The amplitude modulation index, m_a, with m_a defined for each modulation technique in Table 2.1, where A_o is the modulating signal amplitude and A_{cpp} is the carrier peak to peak value
- The angle of displacement, Φ, between the modulating signal (sinusoidal) and the first positive slope of the triangular carrier signal

Table 2.1. Definition of amplitude modulation indices for various multi-carrier modulation techniques

	APOD	PD	POD	H	PS	SIC
m_a	$\frac{A_o}{\frac{m-1}{2}A_{cpp}}$	$\frac{A_o}{\frac{m-1}{2}A_{cpp}}$	$\frac{A_o}{\frac{m-1}{2}A_{cpp}}$	$\frac{A_o}{A_{cpp}}$	$\frac{2A_o}{A_{cpp}}$	$\frac{A_o}{\frac{m-1}{2}A_{cpp}}$

Multi-carrier modulation techniques are used with fixed and variable frequency bands, where the carrier frequency is fixed or variable. Carrier frequency modulation, as in [2.84], is when the carrier frequency is variable. Variable frequency carrier bands have some advantages, such as balancing the active switching among the levels as in [2.85]. Here, only fixed frequency band PWM is considered.

(1) Alternative phase opposition disposition (APOD)

This technique requires each of the *(m–1)* carrier waveforms, for an *m* level phase waveform, to be phase displaced from another by 180 degree alternatively, as shown in figure (2.8a).

(2) Phase disposition (PD)

This technique is similar to APOD, except the carriers are in phase as shown in figure (2.8b).

(3) Phase opposition dispositions (POD)

The carrier waveforms are all in phase above and below the zero reference value, however there is a 180 degree phase shift between those above and those below zero, as shown in figure (2.8c).

(4) Hybrid (H)

This technique combines the previous dispositions technique and the phase shifted

multi-carrier PWM technique. Two bands are used for modulation, however, each time the level of the inverter is increased, more triangular carriers are introduced and phase shifted accordingly, as shown in figure (2.8d). The two carriers above zero have the same peak-to-peak value and the same frequency f_c, however, there is a phase shift of 180 degree between them. The same principle is applied for the two carriers below zero.

(5) Phase shifted (PS)

This technique employs a number of carriers, all of which are appropriately phase shifted. The harmonics are positioned as sidebands around $(m-1)f_c$ and the higher the number of inverter levels, the wider the gap between the fundamental and the first significant harmonics as shown in figure (2.8e).

(6) Super imposed carrier (SIC)

Figure (2.8f) illustrates the carrier modulation method. This technique [2.86] uses only one carrier source. The carrier signal is super imposed on the modulating signal. The carrier signal has the same peak-to-peak value as in the PD, POD, and APOD methods. The modulating signal with the super imposed carrier signal is compared with m-1 constant levels. Each level is the average value at each carrier signal, as in the PD, POD, and APOD methods.

iii. Modulating signal

Sinusoidal PWM can be classified according to the modulating signal:

- Sinusoidal PWM
- Third harmonic injection
- Dead band
- Modulating signal for low modulation index

(1) Sinusoidal PWM (S-PWM):

In the sinusoidal PWM technique, the modulating signal is a sinusoidal waveform as shown in figure (2.9a).

(2) Third harmonic injection (THI-PWM)

A method to improve the gain of the pulse width modulator is to inject a third harmonic (THI-PWM 1st and 3rd) [2.87]-[2.90]. This technique is derived from conventional sinusoidal PWM with the addition of a 17% third harmonic component to the sine reference waveform. The hardware implementation of this technique is straightforward.

It should be noted that the 15% increase in gain over the conventional S-PWM technique is achieved at the expense of introducing third harmonics on the line to neutral waveforms. However for a balanced load with a floating neutral point, third harmonic current cannot flow and therefore third harmonic voltages are not present on the line-to-line waveforms [2.87].

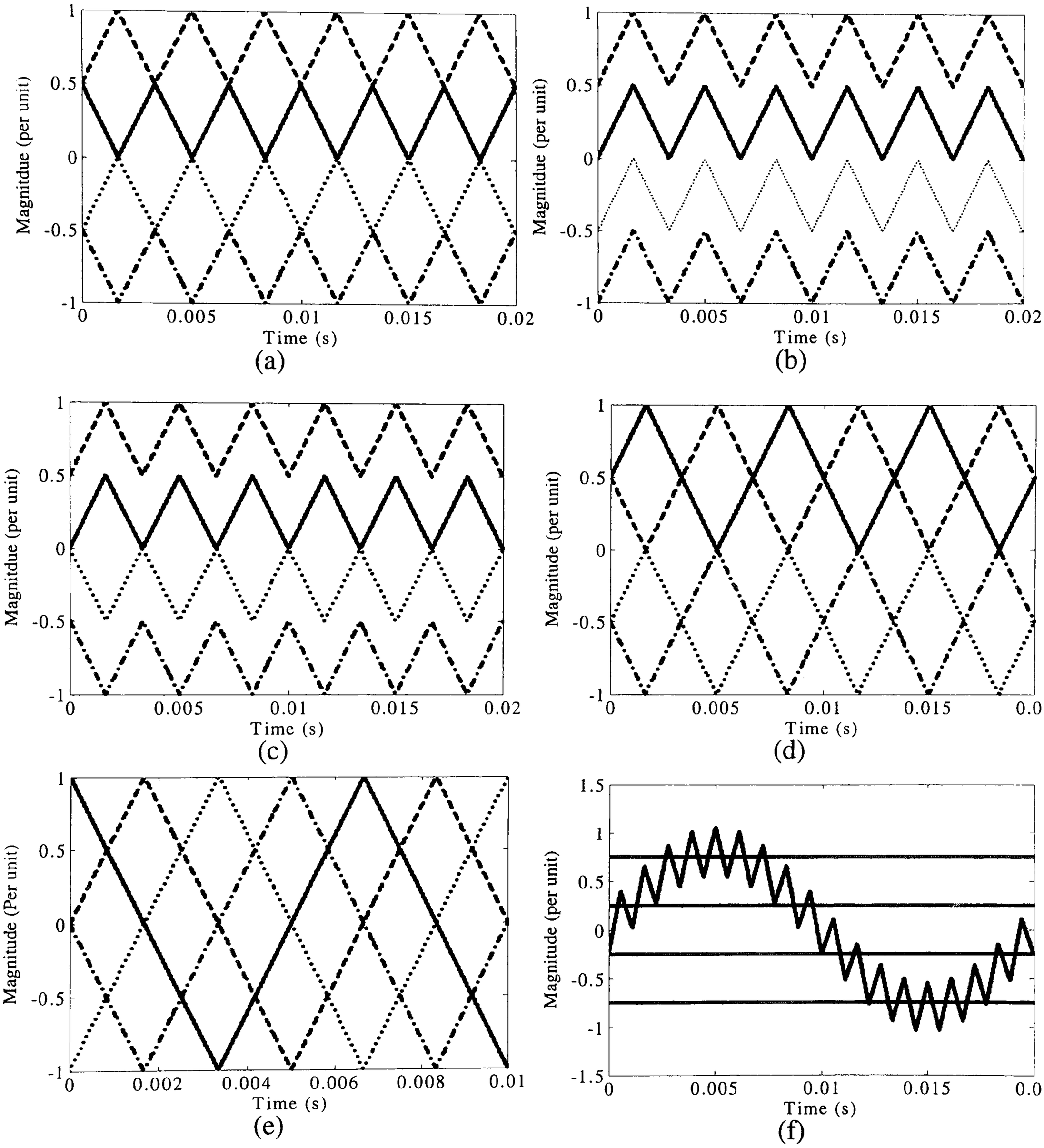


Figure 2.8. Different carrier techniques for multilevel voltage source inverter: (a) APOD, (b) PD, (c) POD, (d) H, (e) PS, and (f) SIC

Based on the same idea, an alternative pattern is the (THI-PWM 1st, 3rd, and 9th)[2.91]. This technique is a variation of the previously presented (THI-PWM 1st, and 3rd). In particular, an addition harmonic component, a multiple of 3 is also injected in the reference waveform.

Although, the above mentioned switching patterns for PWM inverters provide increased gain compared with the conventional S-PWM technique, they also imply the reference or modulating waveforms have to be continuous regardless of their shape. As a result they do not provide any reduction in switching frequency compared with the S-PWM. However there exists PWM techniques which provide increased gain similar to the previous ones but also a reduction in the switching frequency since switching elements are kept inactive for a specified time interval [2.87]. For third harmonic injection PWM, shown in figure (2.9b), the reference waveform is defined as

$$f(\omega_o t) = 1.15 m_a \sin(\omega t) + 0.19 m_a \sin(3\omega t) \qquad 0 \le \omega t \le 2\pi \tag{2.4}$$

This method is called, switching frequency optimal PWM. Steink proposed [2.92] a carrier based method termed, switching frequency optimal PWM (SFO-PWM) which is similar to Carrara's method except that a zero sequence component (triple harmonic) is added to the modulating waveform. This method takes the instantaneous average of the maximum and minimum of the reference voltage (V_a^*, Vb^*, Vc^*) and subtracts this average from each of the individual reference voltages to obtain the modulation waveform [2.93], that is

$$V_{offset} = \frac{\max(V_a^*, V_b^*, V_c^*) + \min(V_a^*, V_b^*, V_c^*)}{2} \tag{2.5}$$

$$\begin{aligned} V_{aSFO}^* &= V_a^* - V_{offset} \\ V_{bSFO}^* &= V_b^* - V_{offset} \\ V_{cSFO}^* &= V_c^* - V_{offset} \end{aligned} \tag{2.6}$$

V_{offset} can be expressed as

$$V_{offset} = (1 - 2k_0) + k_0 \max(V_a^*, V_b^*, V_c^*) + (1 - k_0) \min(V_a^*, V_b^*, V_c^*) \tag{2.7}$$

If $k_0 = 0.5$ then the technique gives THI-PWM

(3) Dead band PWM (DB-PWM)

Since the load neutral point is floating, on an instantaneous basis, keeping one inverter leg inactive does not result in loss of controllability of any of the three output line currents [2.94]. Control of the inverter phases can be relaxed to achieve a lower switching frequency by avoiding intersections for specified time intervals. This can be done either by modifying the modulating waveform or the carrier waveform [2.87].

One technique that belongs to the first case (when the carrier waveform is modified to avoid intersections) is known as modified sinusoidal PWM [2.91]. This technique however results in a more complex hardware implementation. A similar technique has

also been proposed in [2.95], which needs to regulate the inverter DC bus voltage in order to get variable output voltage, since only 240 of 360 degrees are modulated [2.87]. The second case introduces a modified reference waveform, which results in a dead band totalling of 360 degrees for a three-phase inverter. Examples of such dead band PWM switching patterns are presented in [2.96],[2.97]. Dead band modulating waveforms are based on the fact that any function phase shifted by 120 degrees can produce a sinusoidal waveform if and only if it is comprised of sextants of a balanced three-phase system of sinusoidal waveforms [2.87].

Increased output to input voltage ratios are realized. However minimization of switching loss results [2.94], the output ripple current is increased. In equation (2.11), if k_0 is a square wave, dead banding occurs as shown in figure (2.11c).

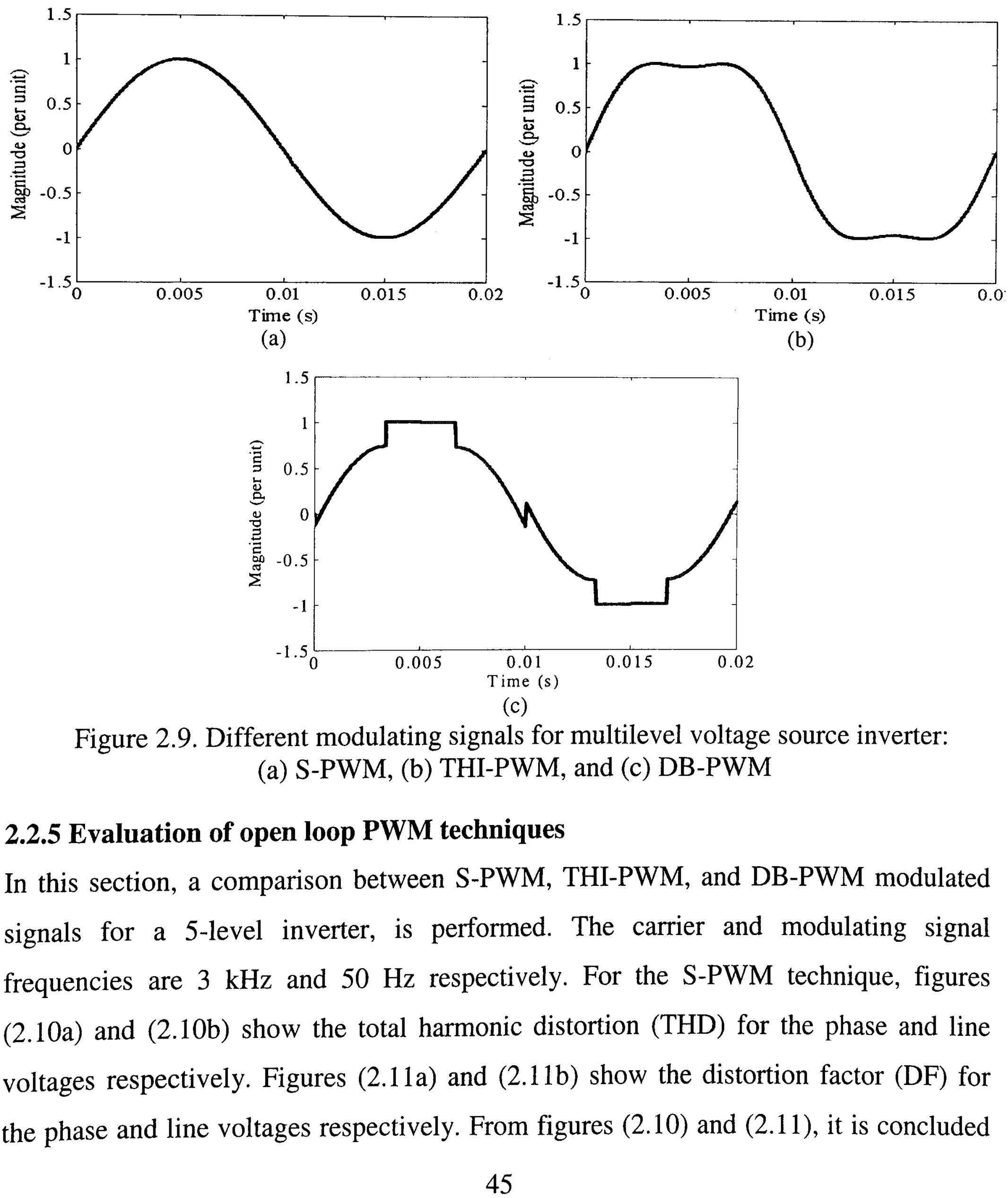


Figure 2.9. Different modulating signals for multilevel voltage source inverter: (a) S-PWM, (b) THI-PWM, and (c) DB-PWM

2.2.5 Evaluation of open loop PWM techniques

In this section, a comparison between S-PWM, THI-PWM, and DB-PWM modulated signals for a 5-level inverter, is performed. The carrier and modulating signal frequencies are 3 kHz and 50 Hz respectively. For the S-PWM technique, figures (2.10a) and (2.10b) show the total harmonic distortion (THD) for the phase and line voltages respectively. Figures (2.11a) and (2.11b) show the distortion factor (DF) for the phase and line voltages respectively. From figures (2.10) and (2.11), it is concluded

that SIC and PD have the lowest line voltage THD, while PS has the lowest phase and line voltage DF.

For the THI-PWM technique, figures (2.12a) and (2.12b) show the THD for the phase and line voltages respectively. Similarly, figures (2.13a) and (2.13b) show the DF. From figures (2.12) and (2.13) it is concluded that SIC and PD have the lowest line voltage THD, while PS has the lowest line voltage DF.

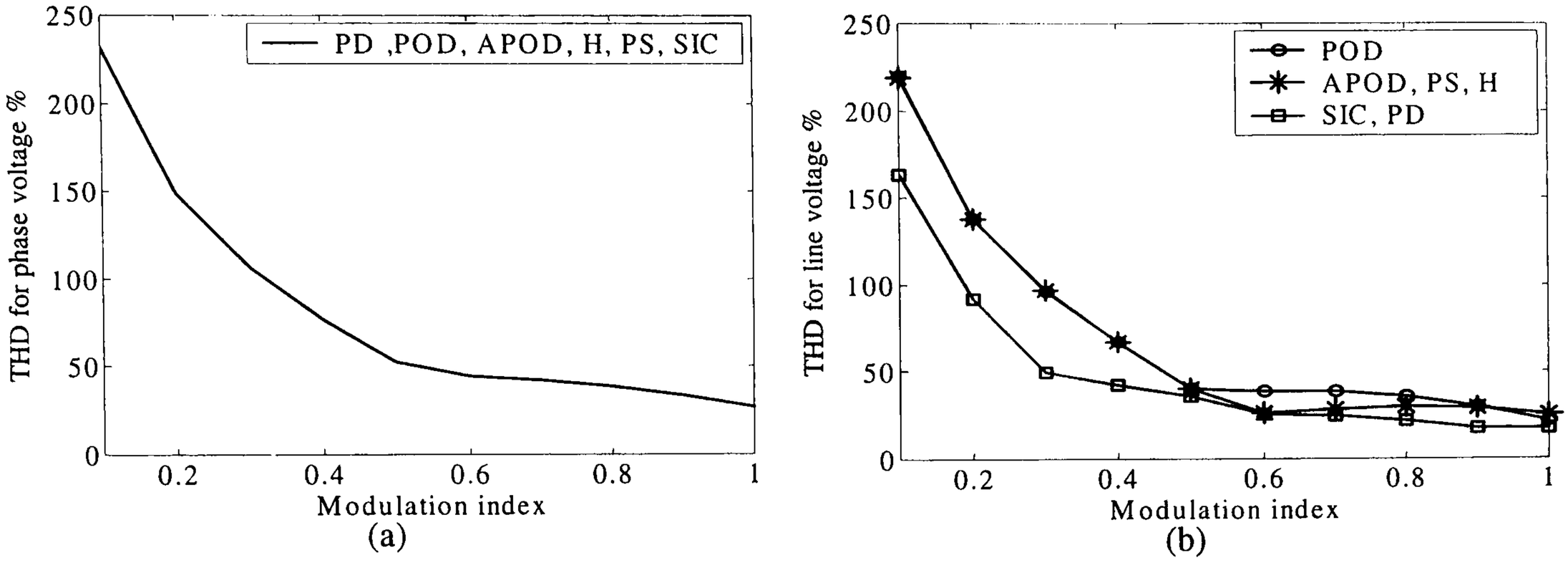


Figure 2.10. THD for S-PWM technique using different carrier techniques (a) phase voltage and (b) line voltage

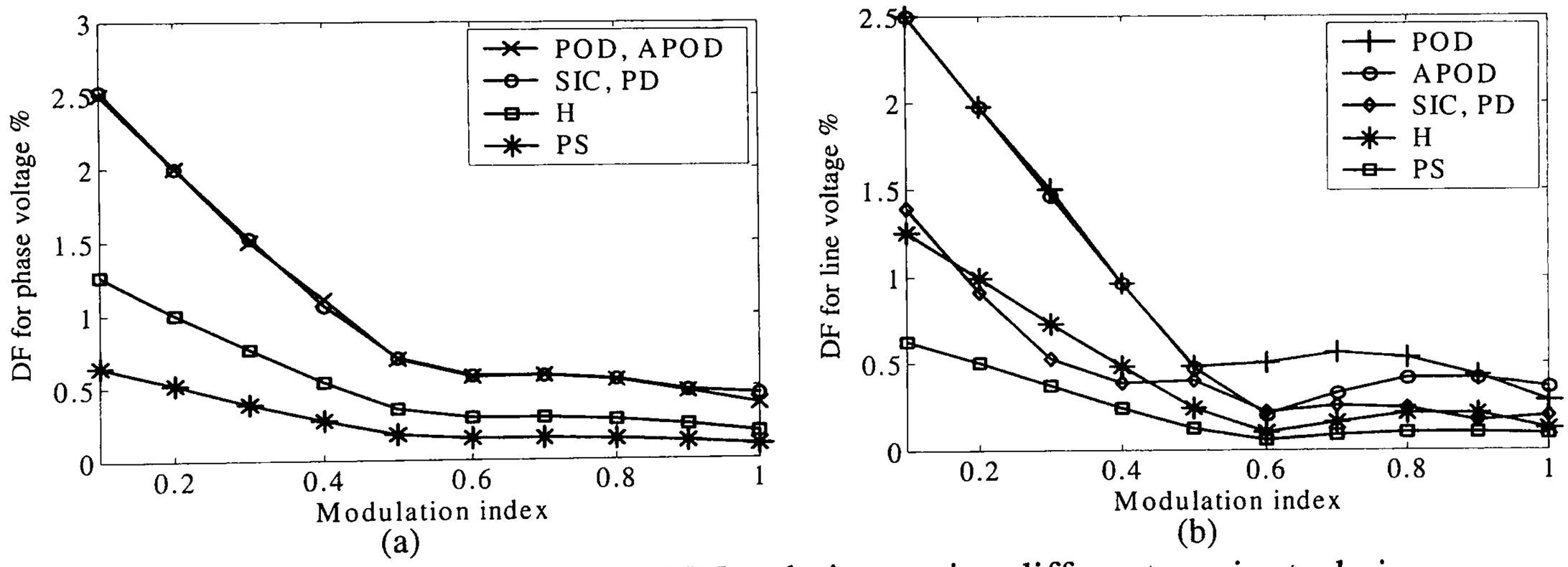


Figure 2.11. DF for S-PWM technique using different carrier techniques: (a) phase voltage and (b) line voltage

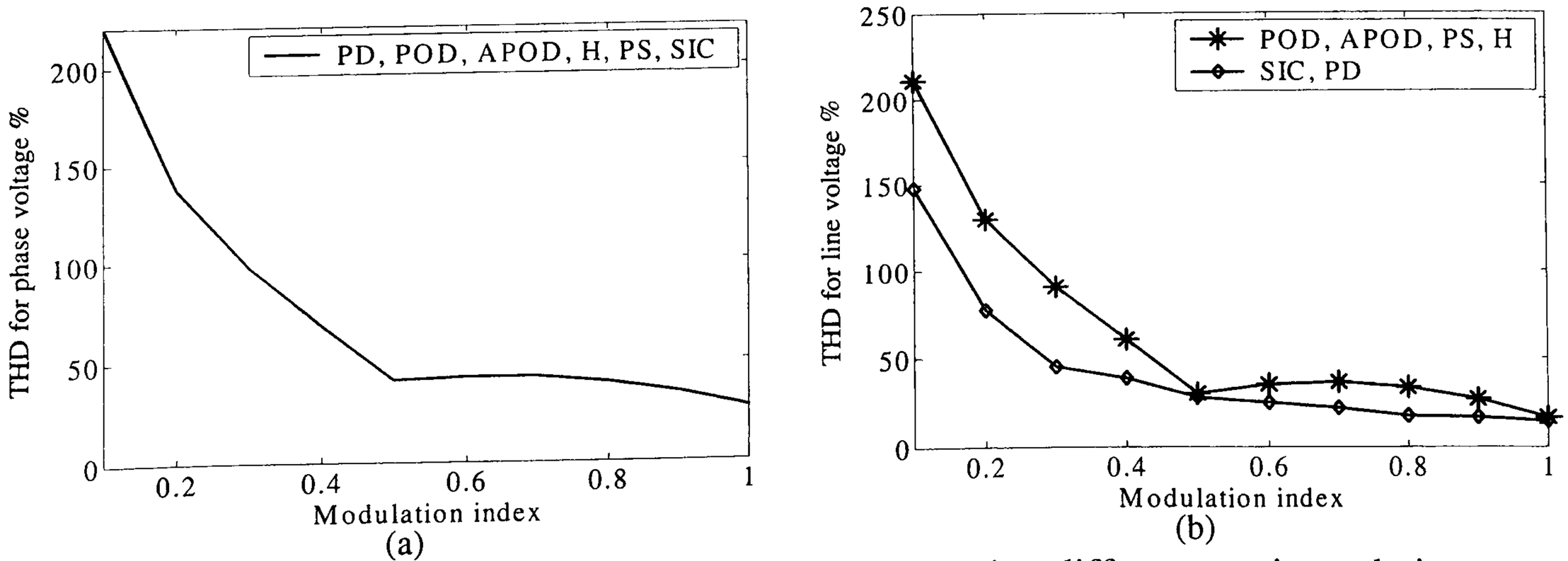


Figure 2.12. THD for THI-PWM technique using different carrier techniques: (a) phase voltage and (b) line voltage

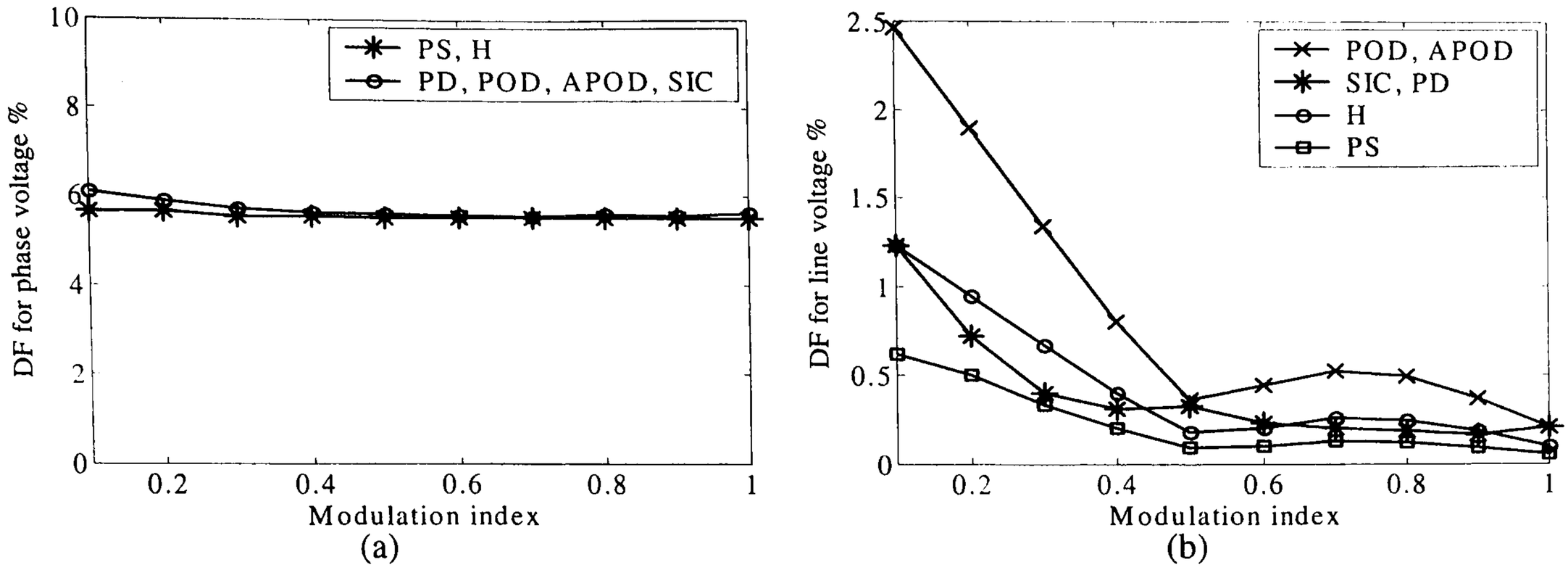


Figure 2.13. DF for THI-PWM technique using different carrier techniques: (a) phase voltage and (b) line voltage

For the DB-PWM technique, figures (2.14a) and (2.14b) show the THD for the phase and line voltages respectively and figures (2.15a) and (2.15b) show the corresponding DF. From figures (2.14) and (2.15), PS has the lowest line voltage DF. Note that the switching frequency of the PS and H techniques is four and two times, respectively, that of the PD, POD, APOD, and SIC techniques. For DB-PWM the switching frequency is two thirds that of S-PWM and THI-PWM, for the same carrier technique.

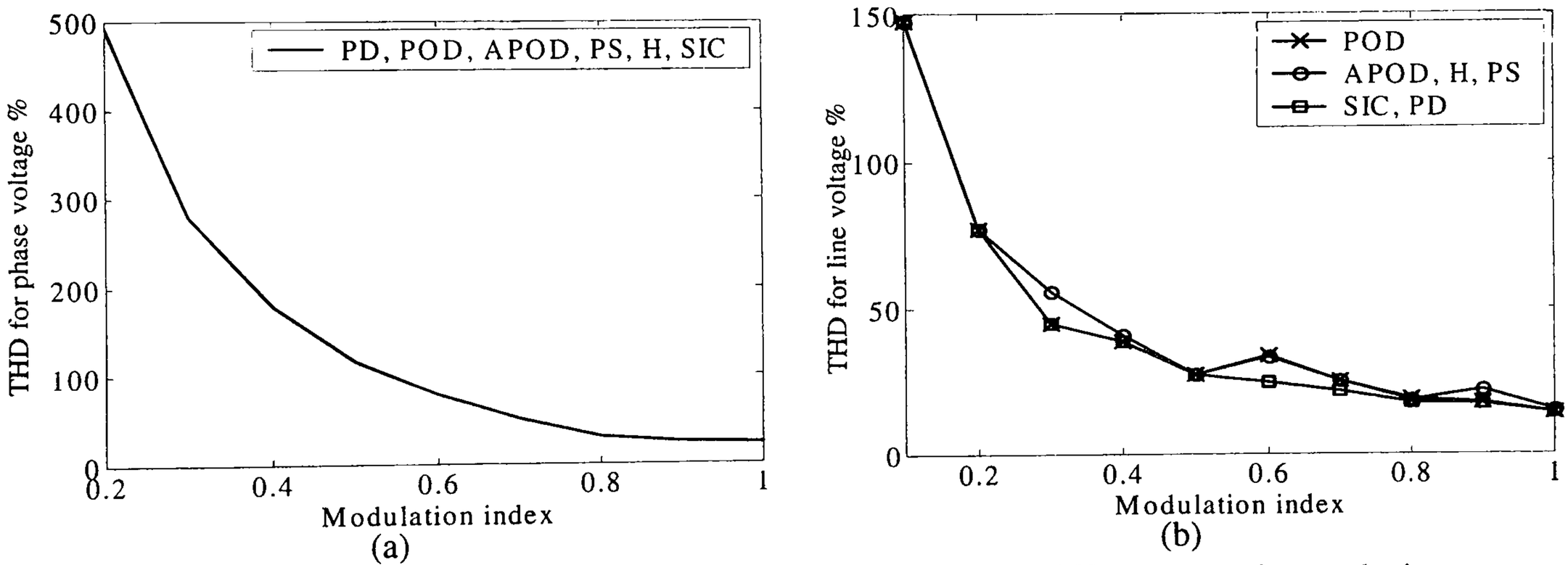


Figure 2.14. THD for DB-PWM technique using different carrier techniques: (a) phase voltage and (b) line voltage

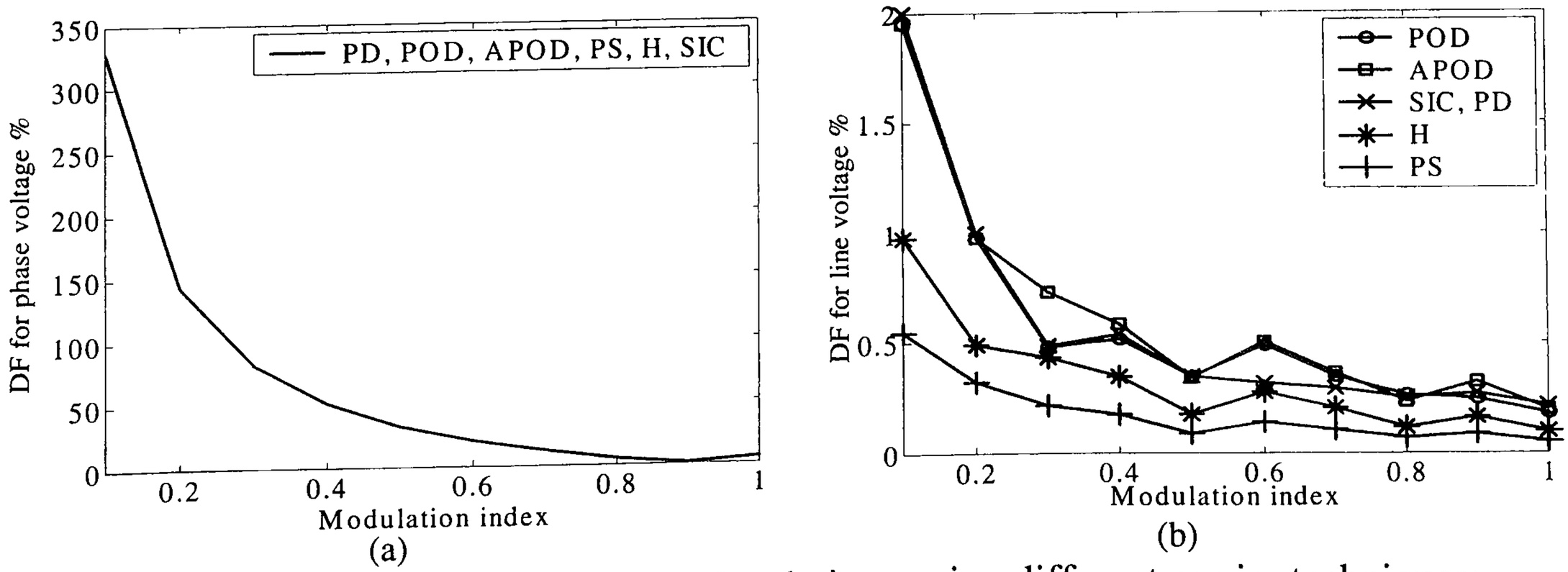


Figure 2.15. DF for DB-PWM technique using different carrier techniques: (a) phase voltage and (b) line voltage

A comparison between the different modulating signals in sinusoidal PWM (S-PWM, THI-PWM, and DB-PWM), space vector modulation (SVM), and sigma-delta modulation (SDM) is performed for a 3-level inverter at a switching frequency of 3 kHz using the PD carrier technique. Note that, the value of integrator gain and sampling frequency in SDM is adjusted to give approximately the same switching frequency as with the other techniques.

From figure (2.16a), SVM and THI-PWM have the lowest line voltage THD and DF at high modulation indices. Also SVM, THI-PWM, and DB-PWM give a higher fundamental component, for the same modulation index, as shown in figure (2.17a) From figure (2.17b), SDM introduces the highest harmonics r.m.s.

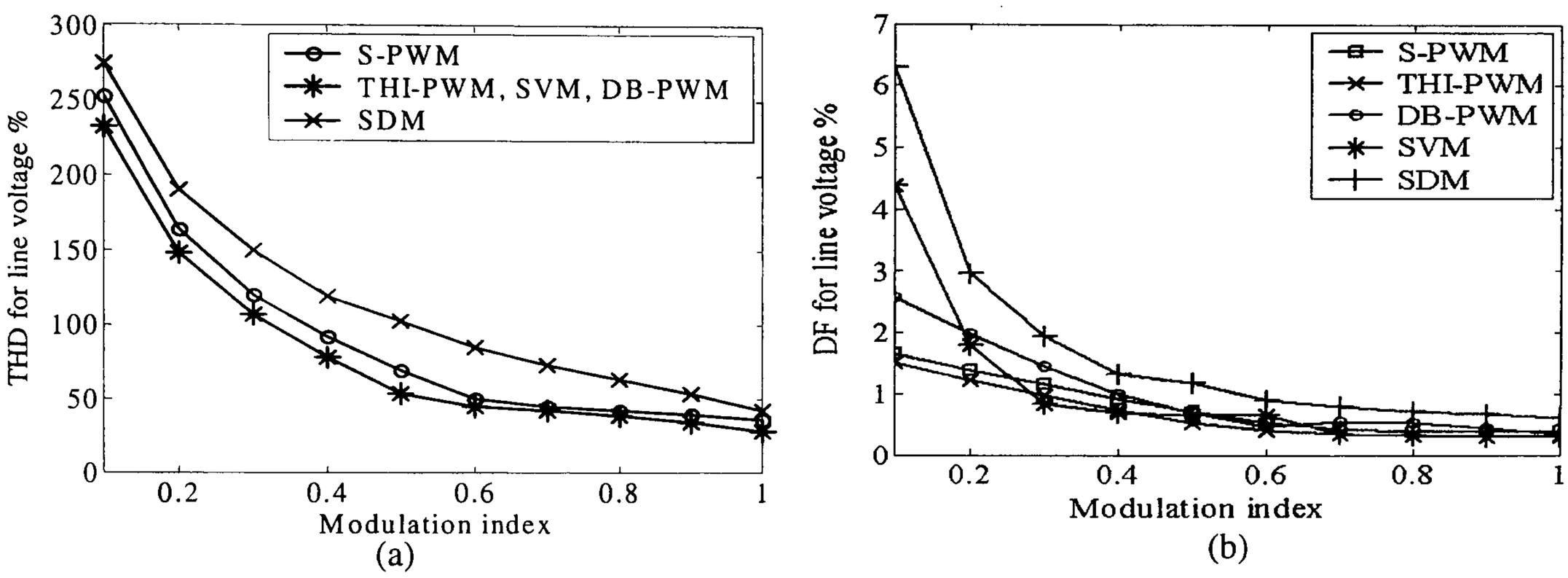


Figure 2.16. THD and DF for the line voltage of three-level inverter:
(a) THD and (b) DF

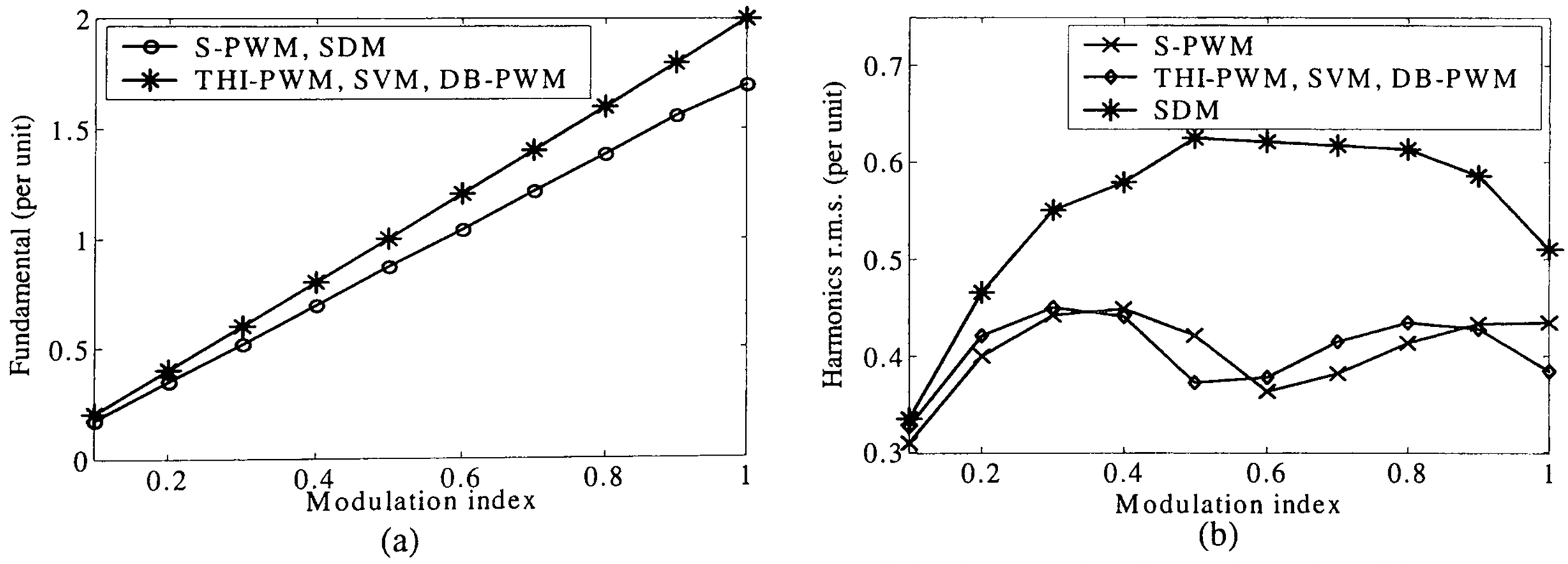


Figure 2.17. Line voltage fundamental and r.m.s. of the harmonics for a three-level inverter:
(a) fundamental and (b) harmonics r.m.s

It can be concluded that, when the switching loss and the line voltage THD are considered with the same switching cycle, SIC and PD are the best choice because of the asymmetry around the time axis introduced by both carrier techniques, which in turn improves the harmonic spectrum of the line voltage waveform. SIC and PD have the same performance because they are represented by one carrier but with different shifts.

At high modulation indices, SVM and THI-PWM introduce the lowest line voltage THD and DF. The gain of the inverter is increased when using THI-PWM and SVM, but a third order harmonic is present in the phase voltage, which may cause serious problems when the load neutral point is grounded. Although reducing the switching frequency, DB-PWM introduces lower order harmonics in the phase voltage, which has the same effect as in THI-PWM when the load neutral point is grounded.

2.3 Closed loop modulation

The open loop modulation techniques described in the previous subsections can be utilized in a closed loop by means of suitable feedback. However there exist some techniques, which appear to be substantially different, where the modulation and control processes are not separated [2.34]. For instance, in the case of an AC motor drive using field orientation ideal impressed stator current offers substantial advantages, in that the stator dynamics can be eliminated. To this end, current controlled VSI can be usefully used.

Given the modulation techniques to be considered in this thesis are open loop, no specific closed loop modulation methods are considered. Figure (2.18) provides reference information on the various closed loop modulation methods.

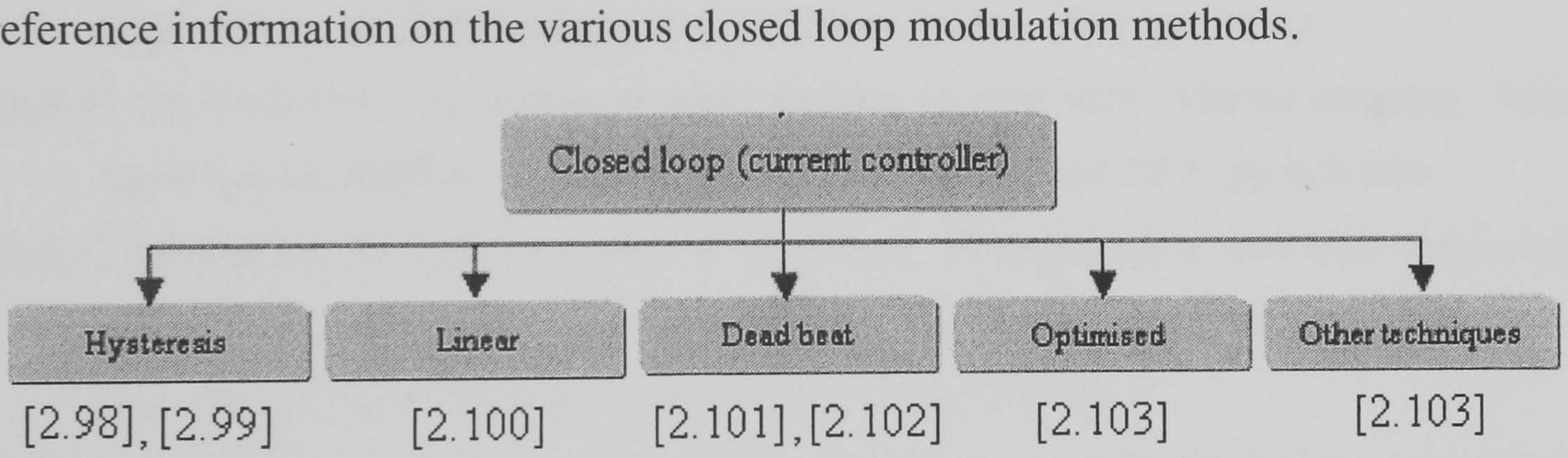


Figure 2.18. Closed loop current control techniques

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Chapter 3

Multilevel and Series Device Connected Inverters

In this chapter a detailed quantitative comparison between two competing high voltage inverter technologies is performed, namely series connection of power devices versus multilevel inverters. The comparison is based on inverter losses (conduction and switching), total harmonic distortion, and distortion factor for the output phase and line voltages, at different modulation frequency ratios. A new method is presented for conduction loss calculation for cascaded multilevel inverters which uses carrier-based pulse width modulation.

3.1 Multilevel and device series connected inverters

High-voltage power inverter applications, such as utility active filters, require the use of power electronic circuits that can operate at supply voltages greater than the ratings of the individual power devices. Extending semiconductor power switching device voltages beyond their ratings is a technological bottleneck. Two principal approaches exist to overcome this problem; viz., series connection of semiconductor power devices and multilevel inverter operation. In the former case, a single high-voltage switch is synthesised by the series connection of multiple semiconductor devices. In the latter case, multilevel inverters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the rating of the individual power devices. Of the three basic multilevel inverters, for this comparison, the cascaded multilevel inverter is considered because of the advantages mentioned in chapter one and section 3.3.

3.2 Series connection of semiconductor power switching devices

Series connection of devices is an established technique that was initially used to produce high-voltage stacks of GTO or thyristor devices. Series operation faces problems of unbalanced static and dynamic voltage sharing, due to the spread of device characteristics and/or mismatch of drive circuits. The problem of static voltage sharing may be solved by the use of parallel connected, series resistor networks whilst dynamic sharing requires the use of passive capacitive snubber networks. Such snubber networks incur losses when energy storage components are reset, but decrease turn off losses. In recent years, high-voltage IGBTs have displaced GTOs in such applications. Whilst IGBTs do not require snubbers to satisfy safe operating area restrictions, voltage sharing problems remain. With IGBTs, voltage balance may be achieved by the use of

conventional passive circuits or by means of active gate control [3.1], [3.2]. Where gate control is used, the transient characteristics are redefined such that all turn-on and turn-off times are compatible with that of the slowest device. This increase in overall switching time will lead to a switching loss increase. Matching the switching speeds will minimize the loss increase. Well established two-level PWM techniques, developed for low-voltage operation, may be applied to inverters based on series connect devices. A circuit diagram indicating the series connection of IGBTs in a three phase voltage source inverter, is shown in figure (3.1). Provided voltage balance is maintained, each device sustains a maximum voltage of E. The IGBTs in this chapter have an anti-parallel diode within their package. Figure (3.3a) shows the output phase voltage.

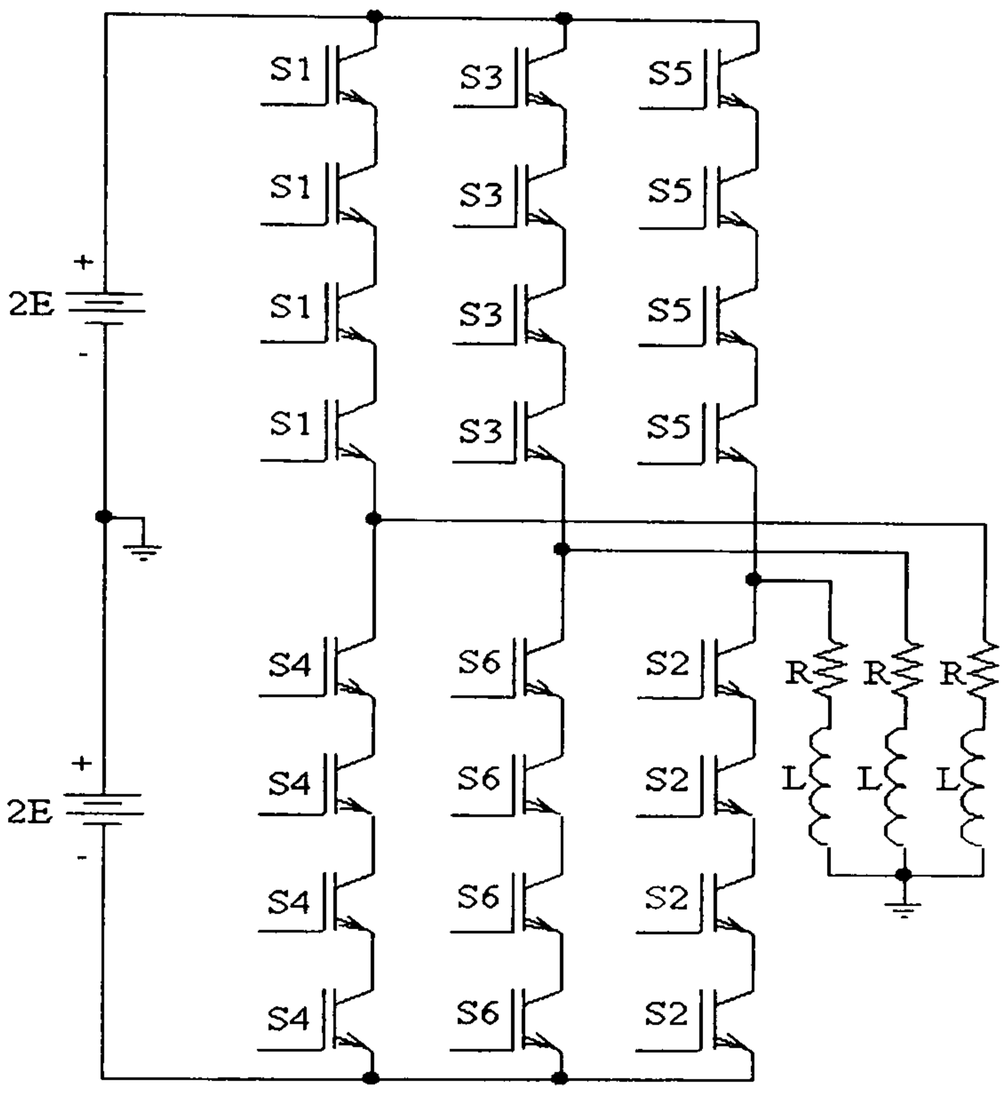


Figure 3.1. Three-phase two-level voltage source inverter using series connected IGBTs (freewheel diodes not shown)

3.3 The cascaded multilevel inverter

The cascaded multilevel full-bridge inverter was proposed by Marchesoni et al. [3.3]. However such a structure utilizes isolated DC sources [3.4]. The cascaded multilevel inverter can be classified, as stated in chapter one, into: normal cascading [3.5], split neutral connection [3.6], modified cascaded [3.7], modified triple cascaded [3.7], hybrid cascaded [3.8], and hybrid switching [3.9]. The normal cascaded type is the most common and will be referred to as the cascaded multilevel inverter. It has many advantages over neutral point clamped and flying capacitor inverters [3.5]. It requires the least number of components among all multilevel inverters to achieve the same number of voltage levels, has a modularised circuit layout, and allows packaging because each level has the same structure. Also, there are no extra clamping diodes or voltage balancing capacitors, and safe switching can be achieved without the need for

bulky and lossy R-C-D snubbers. As a disadvantage, it needs separate DC sources for real power conversion.

Multilevel inverters are promising for high power applications. The circuit diagram of the cascaded multilevel inverter is shown in figure (3.2). The voltage experienced by all the power semiconductor devices is limited to the cell voltage E and the output voltage is made up of a series of E steps as shown in figure (3.3b).

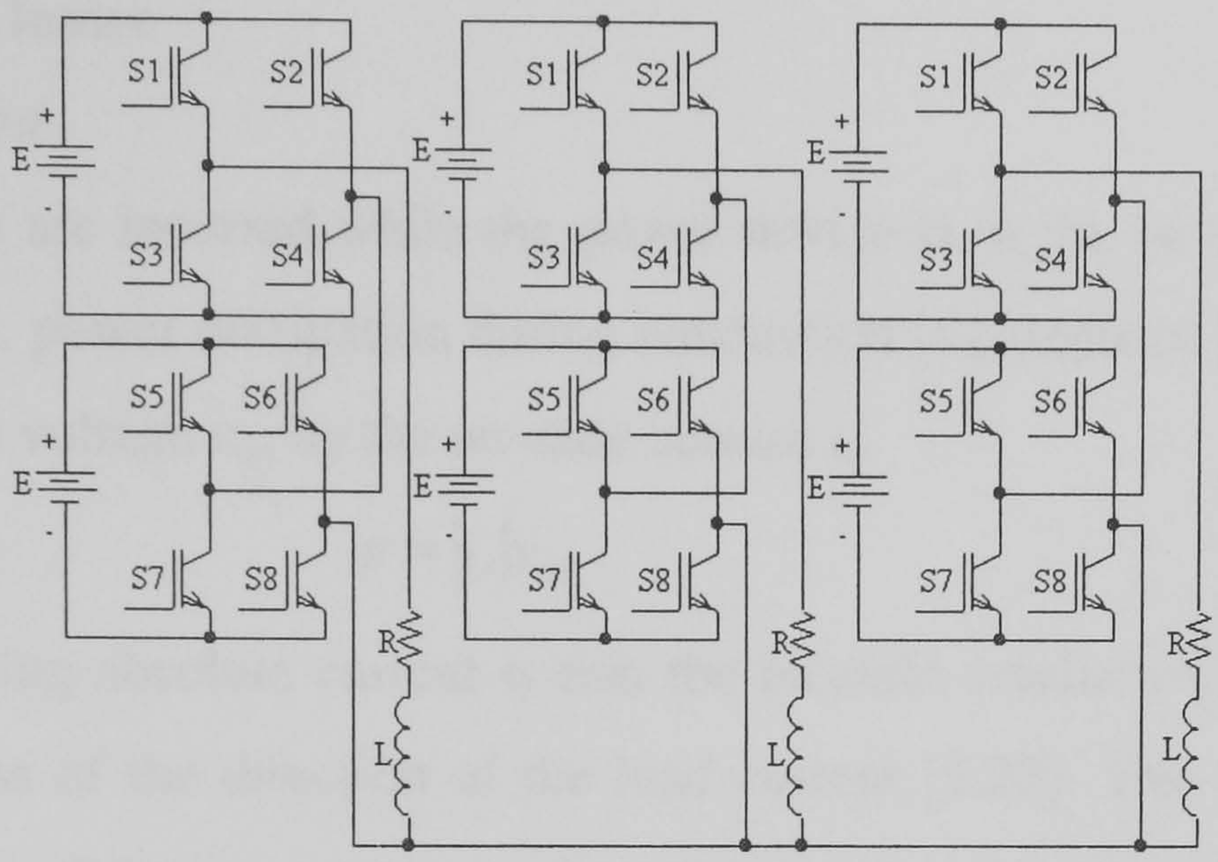
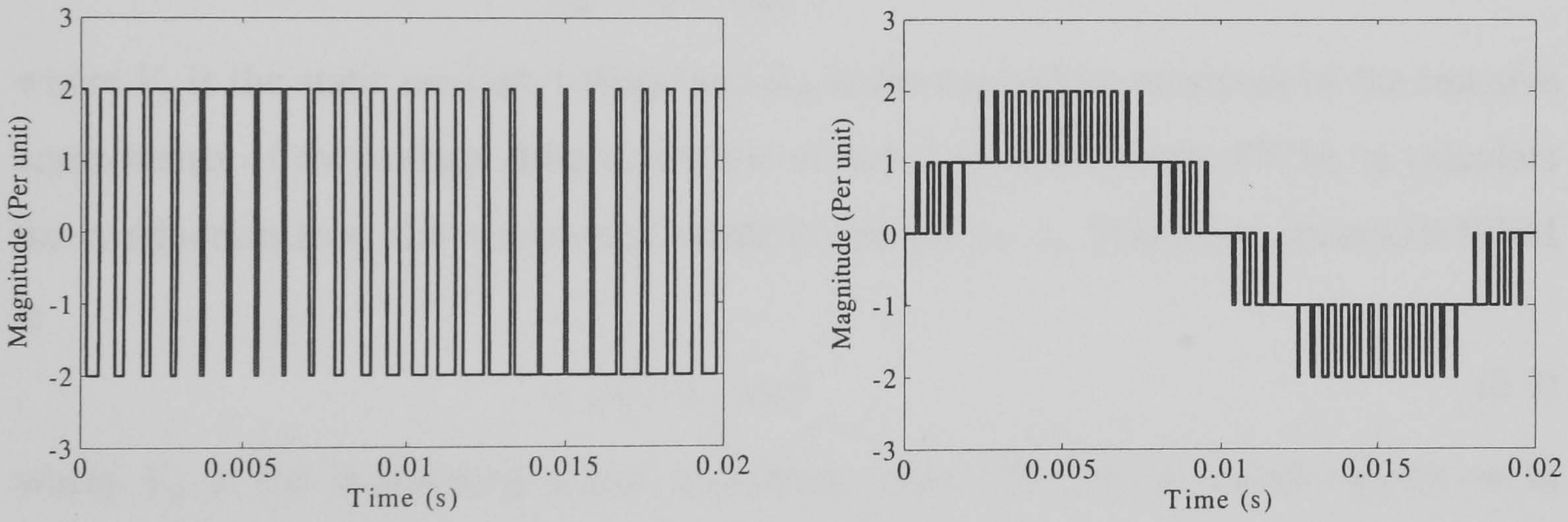


Figure 3.2. Three-phase, cascaded multilevel inverter (5-level phase voltage)



(a) (b)

Figure 3.3. Output phase voltage waveform of:
(a) the two-level inverter and (b) the multilevel inverter

3.4 Comparison of inverter losses in multilevel and device series connected inverters

3.4.1 Multilevel inverter losses

The losses in a device can be classified as: conduction, switching, and off-state [3.18]. Since the leakage current during the device off-state is relatively small, the associated power loss can be neglected. Thus the device power loss is composed of conduction and switching losses. Various methods for analysing conduction and switching losses, for the two-level inverter, have been published [3.19]-[3.21]. Here, analysis is proposed for conduction loss calculation in the cascaded multilevel inverter which can be used for

any carrier-based PWM technique applied to multilevel inverters. The phase opposition disposition (POD) carrier based PWM technique is analysed. A number of carrier waveforms, *m-1*, are displaced by contiguous increments of the reference waveform amplitude, where *m* is the number of phase voltage levels. The carrier waveforms are in phase above the zero reference. Those below zero are in phase but 180^0 phase shift from those above the reference, as shown in figure (3.4a).

3.4.2 Conduction losses

i. Proposed method

Conduction losses are incurred while the power device is in the on-state and conducts current. Therefore, power dissipation during conduction is computed by multiplying the on-state saturation voltage v_{on} by the on-state current i_c.

$$p = |i_c| v_{on} \tag{3.1}$$

The reason for using absolute current is that the on-state conducting current is always positive, regardless of the direction of the load current [3.22]. The saturation voltage, which is a function of device current, can be approximated as a linear function [3.21]

$$v_{on} = V_o + R_{on}|i_c| \tag{3.2}$$

where V_o is the static on-state voltage and R_{on} is the equivalent resistance of the resistive components of the voltage drop across the switch. For multi-carrier PWM, to calculate the conduction loss, the modulating signal is defined as v_m, which for sinusoidal PWM is

$$v_m(\theta) = V_m \sin\theta \tag{3.3}$$

where V_m is the modulating signal maximum value. The carrier signal expression in multi-carrier multilevel PWM, has a unique expression despite the carrier disposition shown in figure (3.4a) for the five-level inverter shown in figure (3.4b). The carrier signal can be expressed as

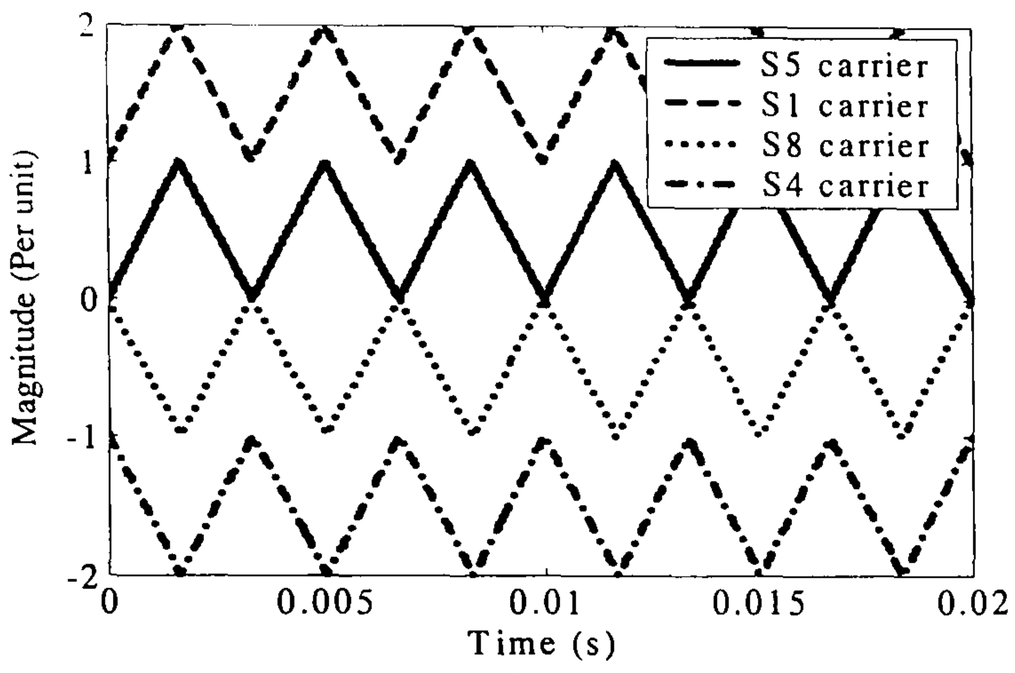
$$v_c(\theta) = qV_c + \begin{cases} \dfrac{V_c}{(\pi/p)}\left(\theta - (n-1)\dfrac{\pi}{p}\right) & (n\text{-}1)\dfrac{\pi}{p} < \theta < n\dfrac{\pi}{p}, \quad n = odd \\ \dfrac{-V_c}{(\pi/p)}\left(\theta - n\dfrac{\pi}{p}\right) & (n\text{-}1)\dfrac{\pi}{p} < \theta < n\dfrac{\pi}{p}, \quad n = even \end{cases} \tag{3.4}$$

q: is the ratio of the peak-to-peak amplitude to carrier signal, at zero crossing of the modulating signal. For example, in parts a and b of figure (3.5), $q = 1$ and 2 for the upper carrier (switch S1).

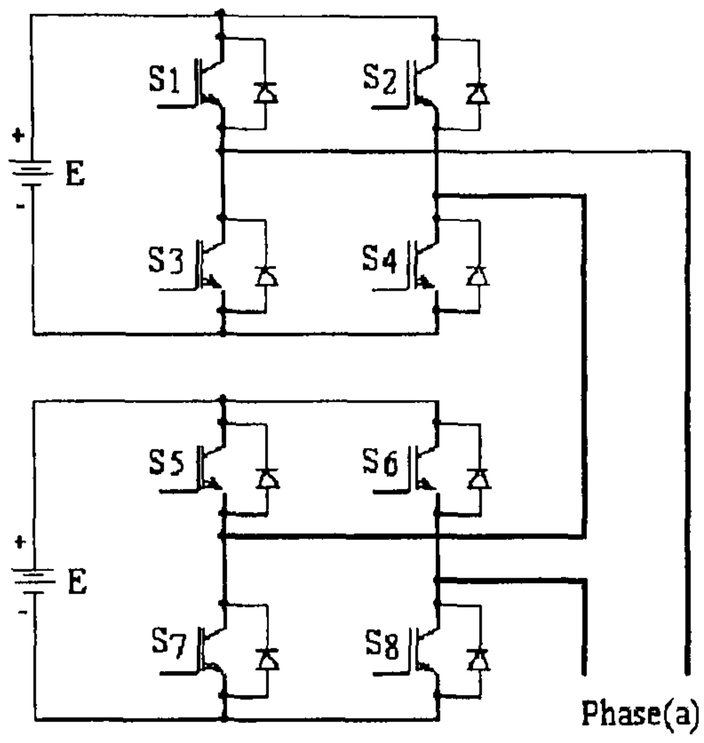
V_c : is the peak-to-peak amplitude of the carrier signal

p : is the frequency modulation ratio (frequency of carrier signal/modulating signal)

$1 \le n \le 2p$ for a complete cycle



(a)



(b)

Figure 3.4. (a) The carrier signals and (b) Single phase of the five-level inverter

Equation (3.4) can be represented as a unique expression

$$v_c(\theta) = qV_c + r\frac{V_c}{(\pi/p)}\left(\theta - (n-1)\frac{\pi}{p}\right) - (1-r)\frac{V_c}{(\pi/p)}\left(\theta - n\frac{\pi}{p}\right) \tag{3.5}$$

where $r = 0$, when n is even, otherwise $r = 1$. Equation (3.5) can be simplified to:

$$v_c(\theta) = V_c\left(q + s\left(-2rn + r + n + \frac{\theta}{(\pi/p)}(2r-1)\right)\right) \tag{3.6}$$

The factor s is added into equation (3.6) to account for the normal carrier signal shown in parts a, c, e, and g of figure 3.5 where $s = 1$, and $s = -1$ for the inverted carrier (180^0 phase shift) shown in parts b, d, f, and h . Figure (3.6) summarizes these different carrier states. The modulation index for POD from Table 2.1 is defined as:

$$m_a = \frac{V_m}{\frac{(m-1)}{2}V_c} \tag{3.7}$$

where m is the number of levels per phase voltage. Note that, the modulation index can be defined in other forms according to the modulation technique used. For sinusoidal PWM, the modulating signal is

$$v_m(\theta) = m_a\frac{(m-1)}{2}V_c\sin\theta \tag{3.8}$$

The difference between the modulating signal and the carrier signal will be

$$f(\theta) = V_c\left(m_a \frac{m-1}{2}\sin\theta - q + s\left(2rn - r - n - \frac{\theta}{(\pi / p)}(2r-1) \right) \right) \tag{3.9}$$

From equations (3.2) and (3.9), the voltage drop across the switch during conduction is defined by two equations

$$v_{on}(\theta) = \begin{cases} \dfrac{V_{on-ce}}{2}(\text{sign}(f(\theta))) + \dfrac{V_{on-ce}}{2} + \dfrac{i_{load}(\theta)}{2}R_{on-ce}(\text{sign}(f(\theta))) + \dfrac{i_{load}(\theta)}{2}R_{on-ce} \\ \text{when the load voltage and current have the same sign} \\ \dfrac{V_{on-D}}{2}(\text{sign}(f(\theta))) + \dfrac{V_{on-D}}{2} + \dfrac{i_{load}(\theta)}{2}R_{on-D}(\text{sign}(f(\theta))) + \dfrac{i_{load}(\theta)}{2}R_{on-D} \\ \text{when the load voltage and current have a different sign} \end{cases} \tag{3.10}$$

where ***sign*** is the sign function (gives 1 for a positive value otherwise –1).

$V_{on\text{-}ce}$ is the IGBT collector-emitter voltage drop;

$R_{on\text{-}ce}$ is the IGBT on-state resistance;

$V_{on\text{-}D}$ is the anti parallel diode voltage drop; and

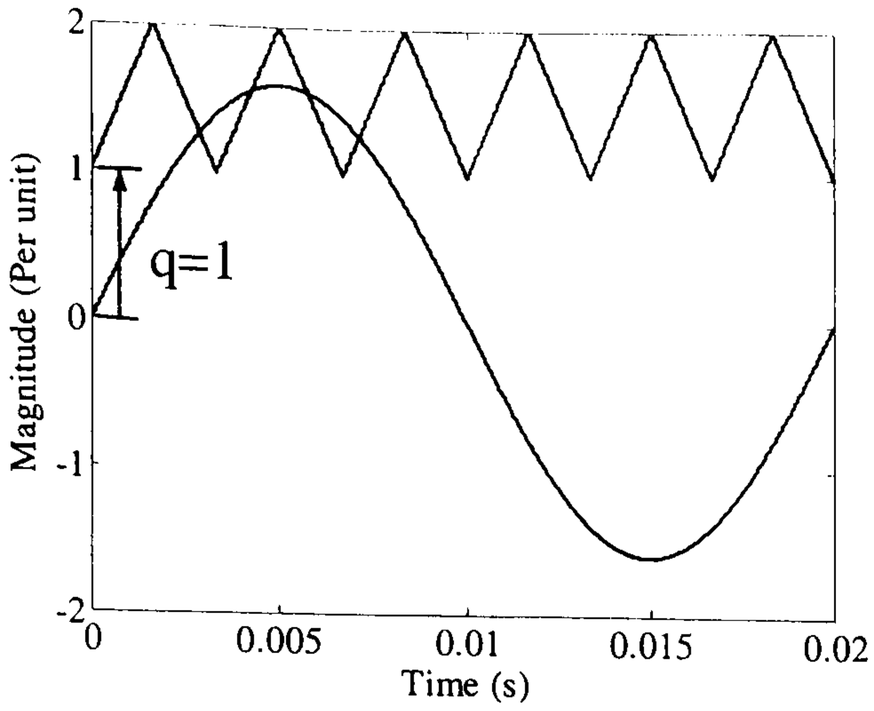
$R_{on\text{-}D}$ is the diode on-state resistance.

The load current is assumed to be sinusoidal and of the form:

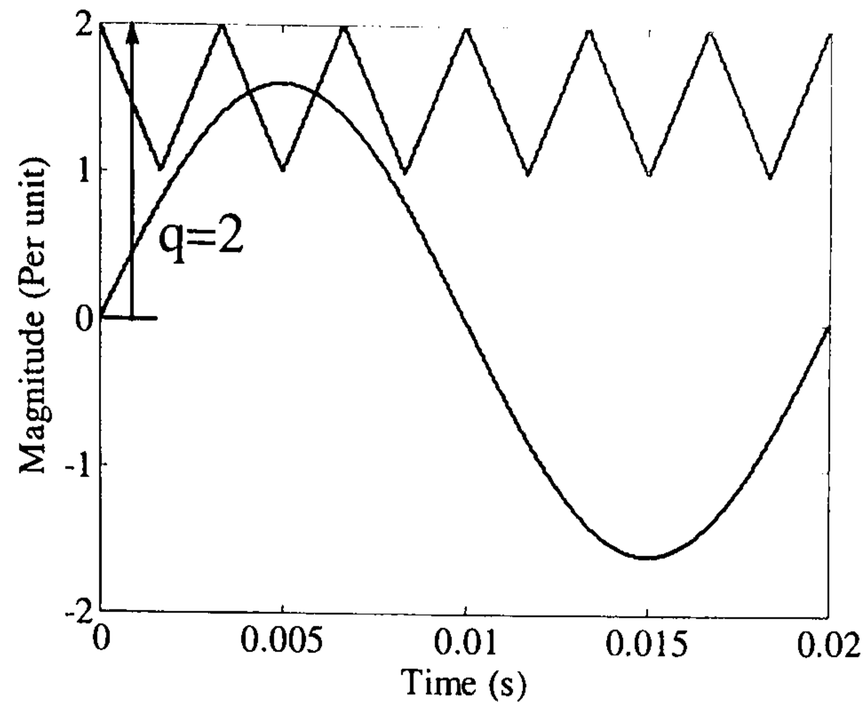
$$i_{load}(\theta) = \hat{I}.\sin(\theta - \phi) \tag{3.11}$$

where $\hat{I}$ is the maximum load current and ϕ is the power factor load angle, which is positive when the load is inductive and negative for a capacitive load. The switch conduction loss during one modulation waveform period is

$$P_{cond} = \frac{1}{2\pi}\int_0^{2\pi} v_{ce}(\theta).i_{load}(\theta)\ d\theta \tag{3.12}$$



(a)



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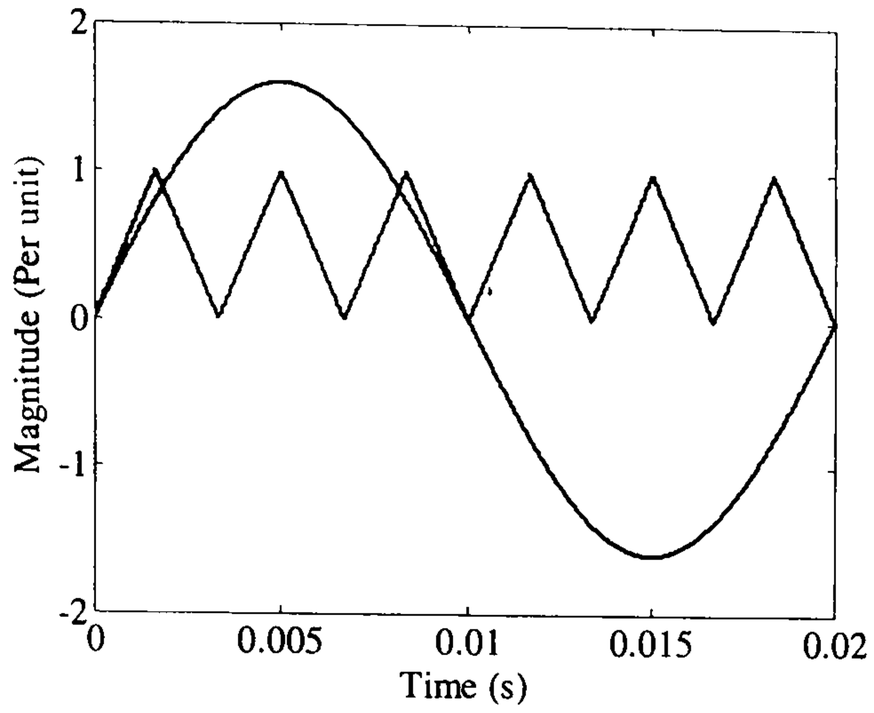
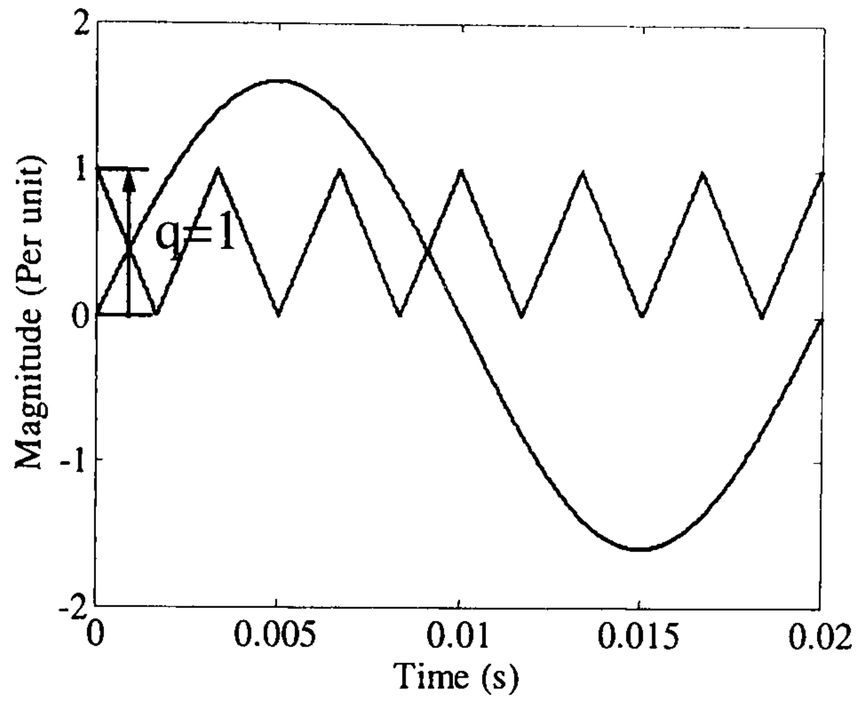
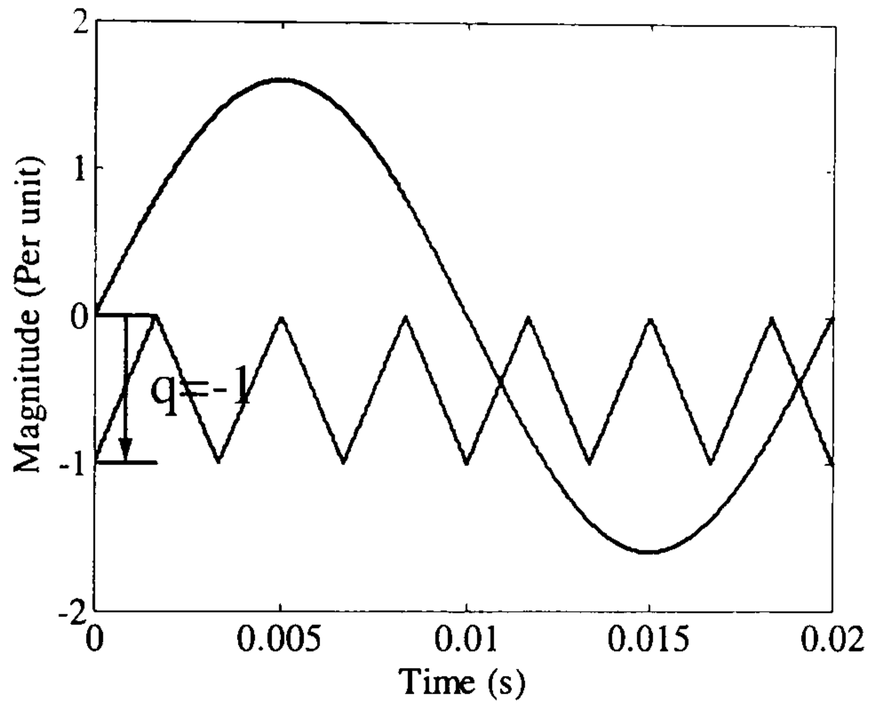


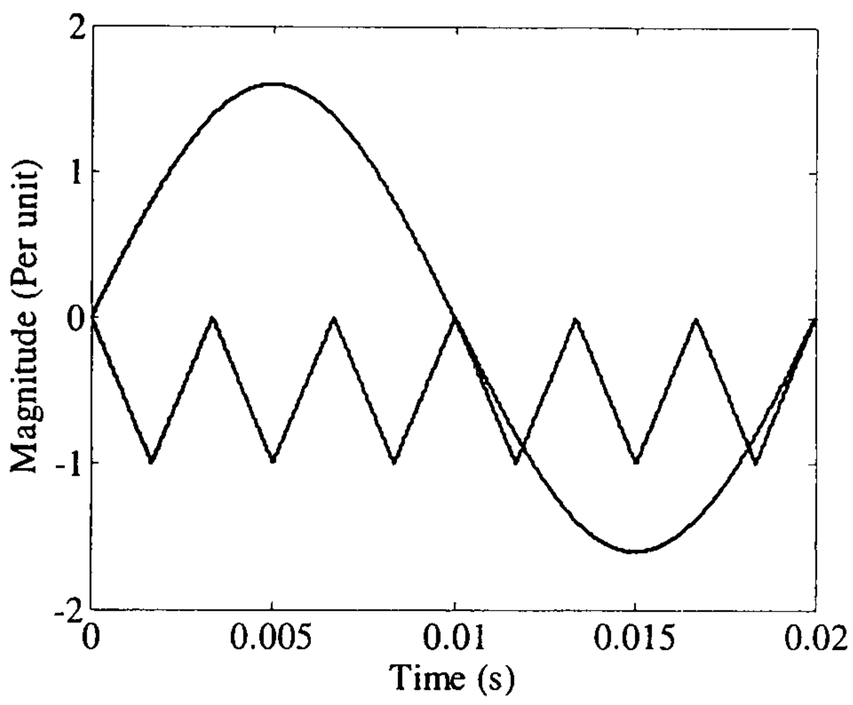
(c)



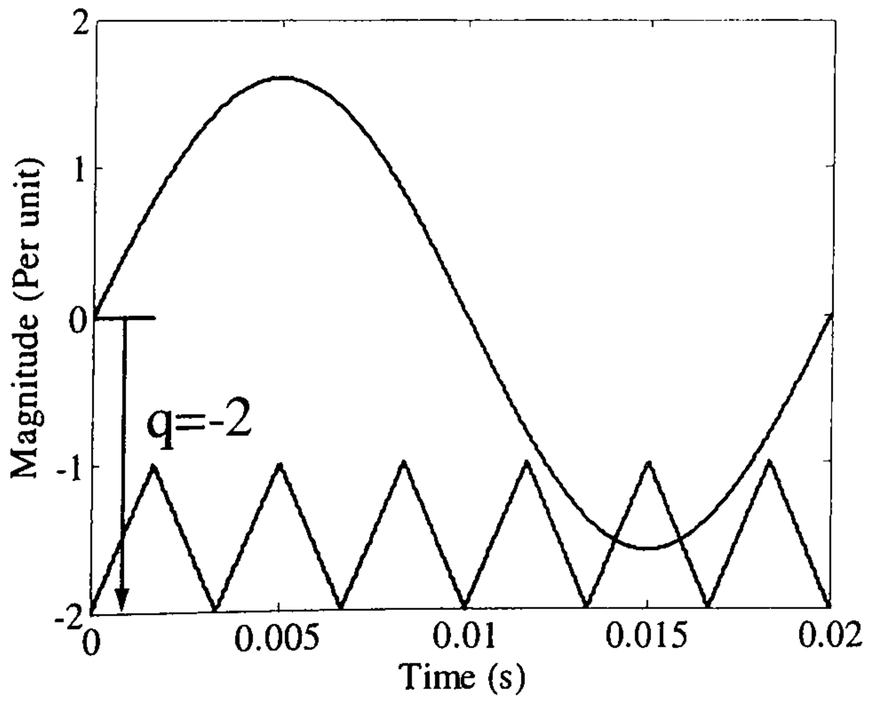
(d)



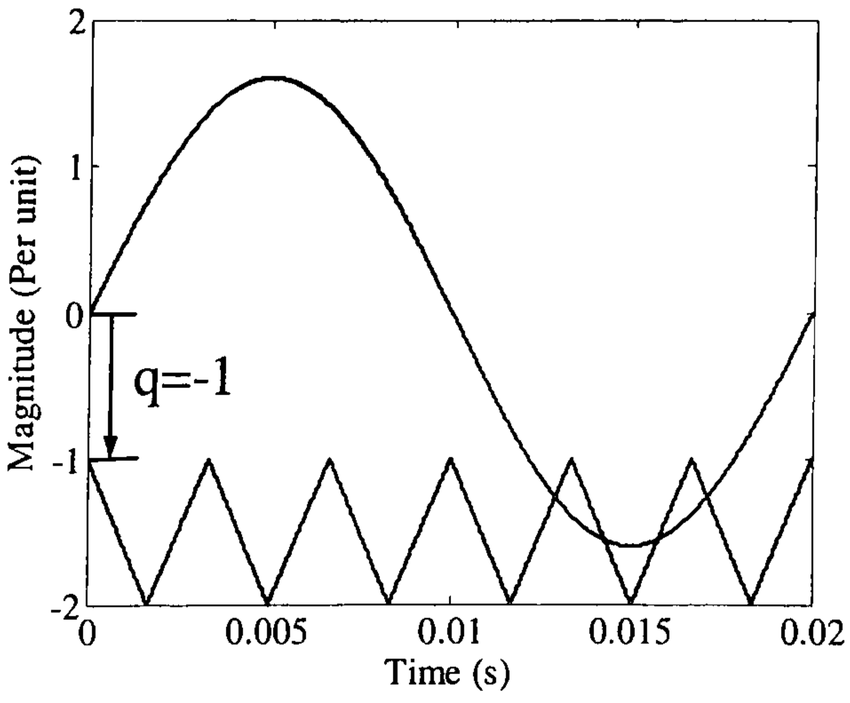
(e)



(f)



(g)



(h)

Figure 3.5. Carrier signal for switch

(a) S1 (*q = 1 & s = 1)* and (b) S1 (*q = 2 & s = -1)*
(c) S5 (*q = 0 & s = 1)* and (d) S5 (*q = 1 & s = -1)*
(e) S8 (*q = -1 & s = 1)* and (f) S8 (*q = 0 & s = -1)*
(g) S4 (*q = -2 & s = 1)* and (h) S4 (*q = -1 & s = -1)*

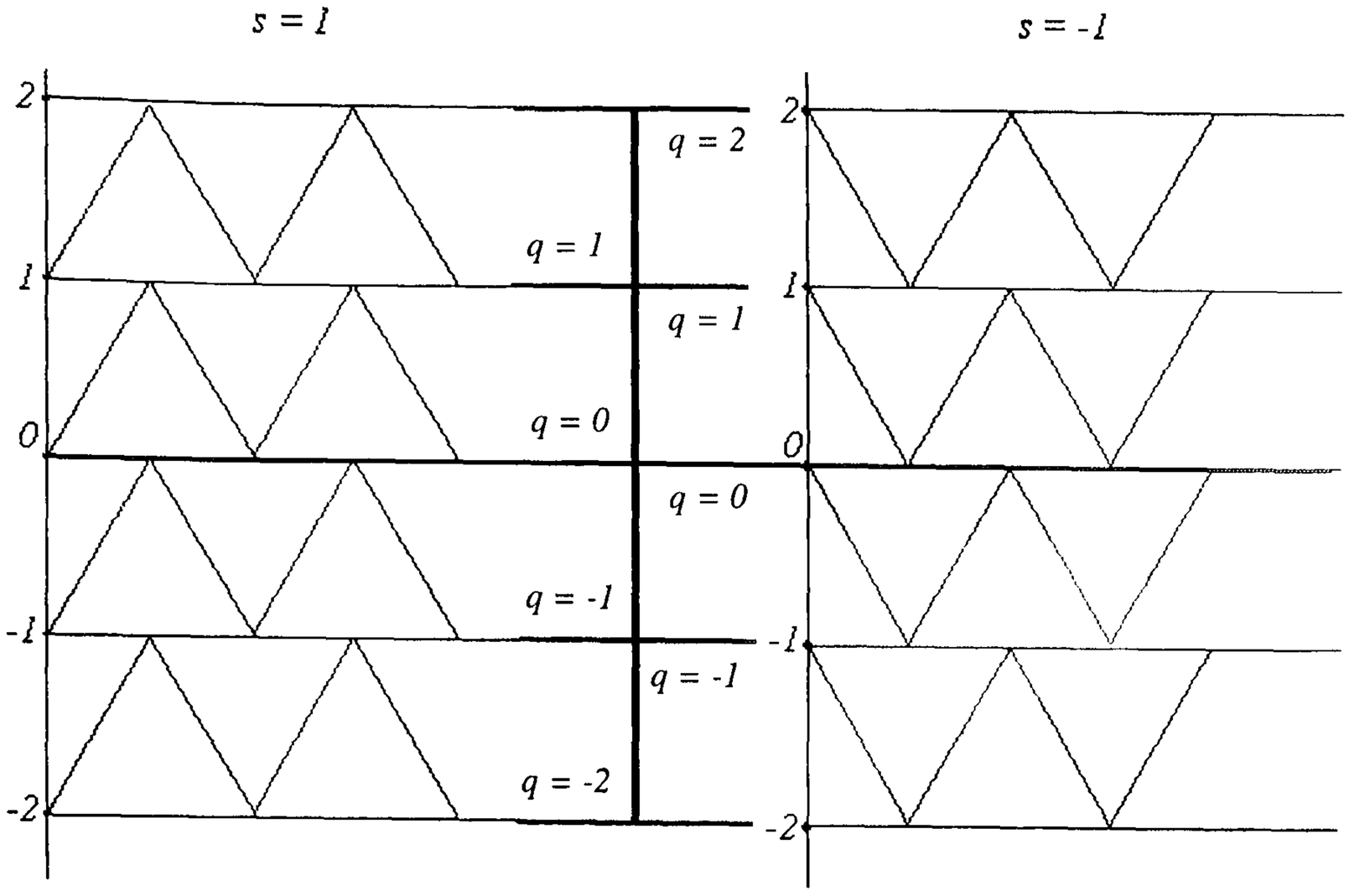


Figure 3.6. Summary of the different carrier states in figure 3.5

ii. Current paths in the cascaded multilevel inverter

In cascaded multilevel inverters, there are $2^{(m-1)}$ states for the phase voltage and m^3 for the line voltage. Table 3.1 indicates the states of the five-level inverter shown in the ten parts of figure (3.7). Note that '1' indicates that the switch is on and '0' is off. S1, S4, S5, and S8 are complementary to S3, S2, S7, and S6, respectively. The shaded columns show the state used for each level, and indicates the current path.

Table 3.1. The total states for a five-level inverter

Case	Case (1)	Case (2)				Case (3)						Case (4)				Case (5)
Voltage	2E	E				0						-E				-2E
S1	1	1	1	1	0	1	1	0	0	1	0	1	0	0	0	0
S4	1	1	1	0	1	0	0	1	1	1	0	0	1	0	0	0
S5	1	1	0	1	1	1	0	1	0	0	1	0	0	1	0	0
S8	1	0	1	1	1	0	1	0	1	0	1	0	0	0	1	0

The following five cases clarify the current paths:

Case 1: When the output load voltage is 2E, if the current is

positive: S1, S4, S5, S8 conduct, figure (3.7a).

negative: D1, D4, D5, D8 conduct, figure (3.7b).

Case 2: When the output load voltage is E, if the current is

positive: D3, S4, S5, S8 conduct, figure (3.7c).

negative: S3, D4, D5, D8 conduct, figure (3.7d).

Case 3: When the output load voltage is 0, if the current is

positive: D3, S4, D7, S8 conduct, figure (3.7e).

negative: S3, D4, S7, D8 conduct, figure (3.7f).

Case 4: When the output load voltage is -E, if the current is

positive: D3, S4, D7, D6 conduct, figure (3.7g).

negative: S3, D4, S7, S6 conduct, figure (3.7h).

Case 5: When the output load voltage is -2E, if the current is

positive: D2, D3, D6, D7 conduct, figure (3.7i).

negative: S2, S3, S6, S7 conduct, figure (3.7j).

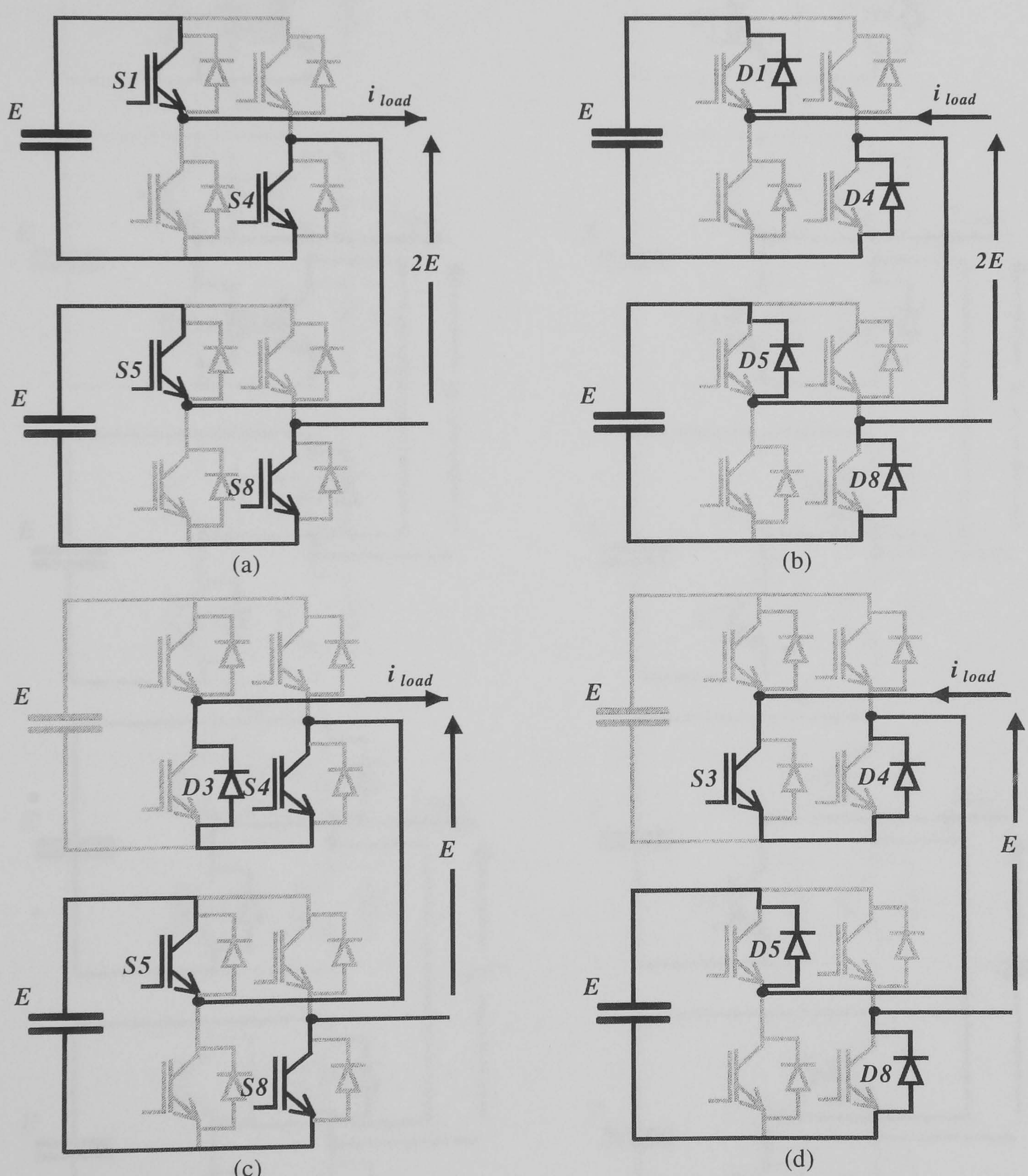


Figure 3.7. The current direction and switches path

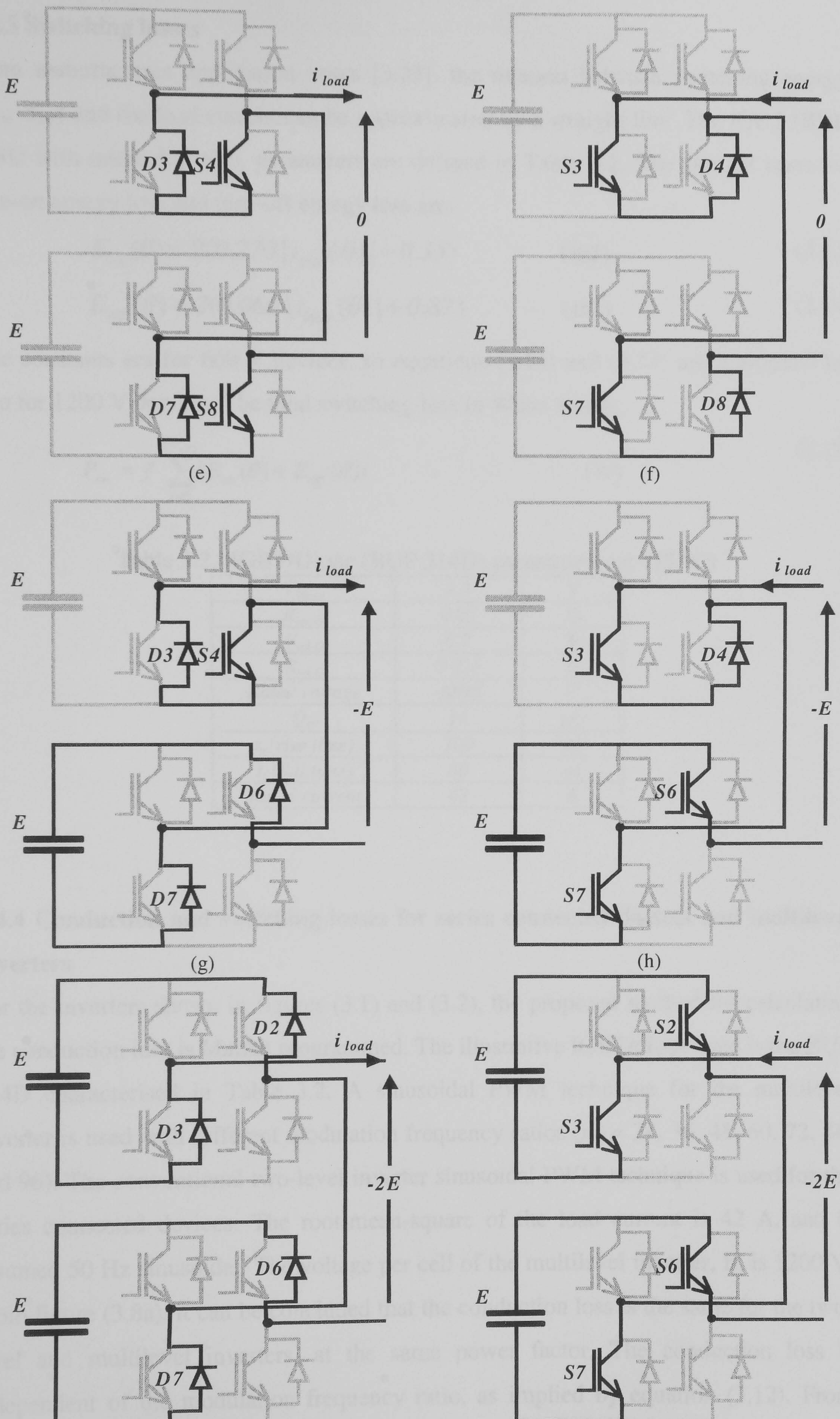


Figure 3.7. The ten different current paths in the five-level cascaded inverter

3.4.3 Switching losses

From manufactures application notes [3.23], the relation between switching energy (E_{on}, E_{off}) and the load current can be approximated by a straight line. The IGBT (BUP 314D with internal diode), parameters are defined in Table 3.2. The straight lines for turn-on energy loss and turn-off energy loss are:

$$E_{on}(\theta) = 2(0.270\,|\,i_{load}(\theta)\,| - 0.35) \quad \text{(mJ)} \tag{3.13}$$

$$E_{off}(\theta) = 2(0.066\,|\,i_{load}(\theta)\,| + 0.87) \quad \text{(mJ)} \tag{3.14}$$

The constants are for 600 V devices, so equations (3.13) and (3.14) are multiplied by two for 1200 V devices. The total switching loss in Watts equals:

$$P_{sw} = f \sum_{t=0}^{t=1/T_s} (E_{on}(\theta) + E_{off}(\theta)) \quad \text{(W)} \tag{3.15}$$

Table 3.2. IGBT/Diode (BUP 314D) parameters (at 125 °C)

$V_{on\text{-}ce}$	4.3	V
$R_{on\text{-}ce}$	0.05	Ω
$V_{on\text{-}D}$	0.7	V
$R_{on\text{-}D}$	0.025	Ω
Rated voltage	1200	V
Q_{rr}	11	μC
t_r (rise time)	100	ns
t_f (fall time)	60	ns
Rated current	42	A

3.4.4 Conduction and switching losses for series connected devices and multilevel inverters

For the inverters shown in figures (3.1) and (3.2), the proposed method for calculating the conduction loss is Matlab programmed. The illustrative IGBT/diode used is the BUP 314D characterised in Table 3.2. A sinusoidal PWM technique for the multilevel inverter is used with different modulation frequency ratios (m_f = 24, 36, 48, 60, 72, 84, and 96). The conventional two-level inverter sinusoidal PWM technique is used for the series connected devices. The root-mean-square of the load current is 42 A, and is assumed 50 Hz sinusoidal. The voltage per cell of the multilevel inverter, E, is 1200 V. From figure (3.8a), it can be concluded that the conduction loss is the same for the two-level and multilevel inverters, at the same power factor. The conduction loss is independent of the modulation frequency ratio, as implied by equation (3.12). From figure (3.8b), it is concluded that, the switching loss for the two-level inverter is much higher than that of the multilevel inverter, at the same modulation frequency ratio m_f.

For example, the switching loss of the multilevel inverter at $m_f = 96$ is the same as for the 2-level inverter but at $m_f = 24$. In the series connection, the IGBTs will require active gate control or passive snubber networks. Both sharing techniques result in increased switching loss.

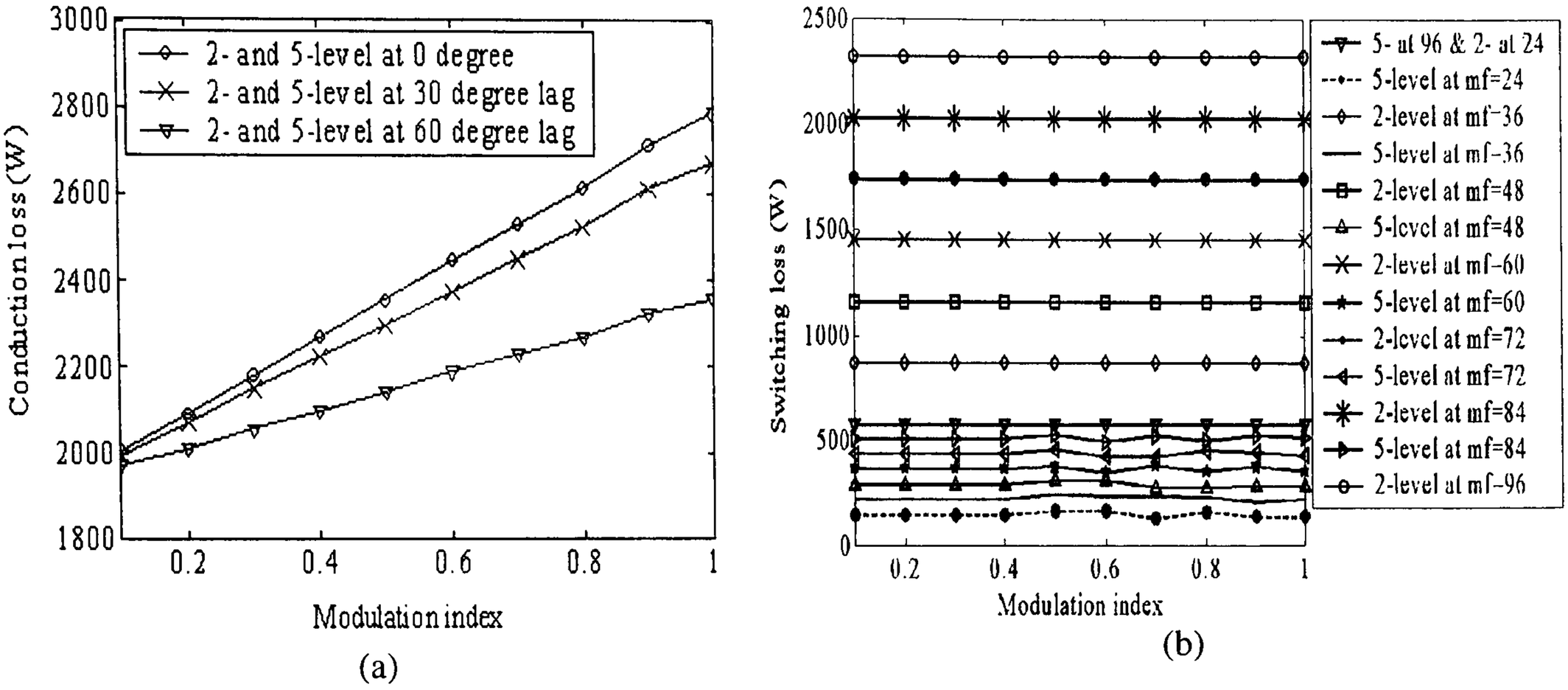


Figure 3.8. Losses of five-level and two-level inverters:
(a) conduction and (b) switching losses

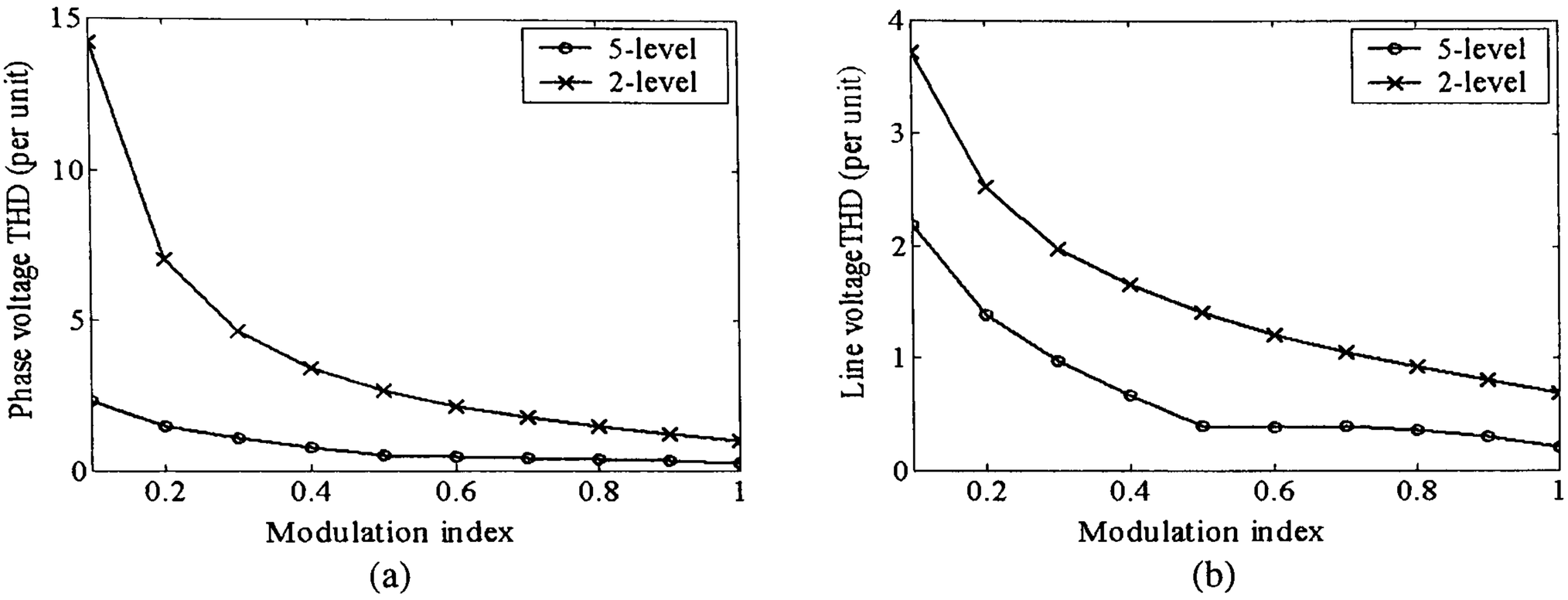
3.5 Output voltage spectrum of series connected devices and multilevel inverters

Total harmonic distortion (THD) and distortion factor (DF) (both defined in chapter two) are investigated for both the multilevel and IGBTs series connection inverters at different modulation frequency ratios (m_f = 24, 36, 48, 60, 72, 84, and 96). Sinusoidal PWM is used for the five-level inverters and standard sinusoidal PWM is used for the two-level case. Figure (3.9a) shows the total harmonic distortion (THD) for the phase voltage of the two-level and five-level inverters, while figure (3.9b) shows the corresponding THD for the line voltage. The THD figures are not dependent on m_f with m_f = 24, 36, 48, 60, 72, 84, and 96. The THD for the five-level inverter is much lower than for the two-level inverter, for the same modulation index.

Distortion factor provides a better performance indication in non-machine power applications. Figure (3.10) shows the DF for the phase voltage for different modulation frequency ratios, while figure (3.11) shows the corresponding line voltage results. From figure (3.10), it is concluded that the phase voltage DF of the five-level inverter is lower than that of the two-level inverter for the same modulation frequency ratio. Even if the modulation frequency ratio is increased to six times that of the five-level case, the five-level inverter DF is still better. From figure (3.11), the line voltage DF of the five-level inverter is better than that of the two-level inverter at high modulation index ratios (for

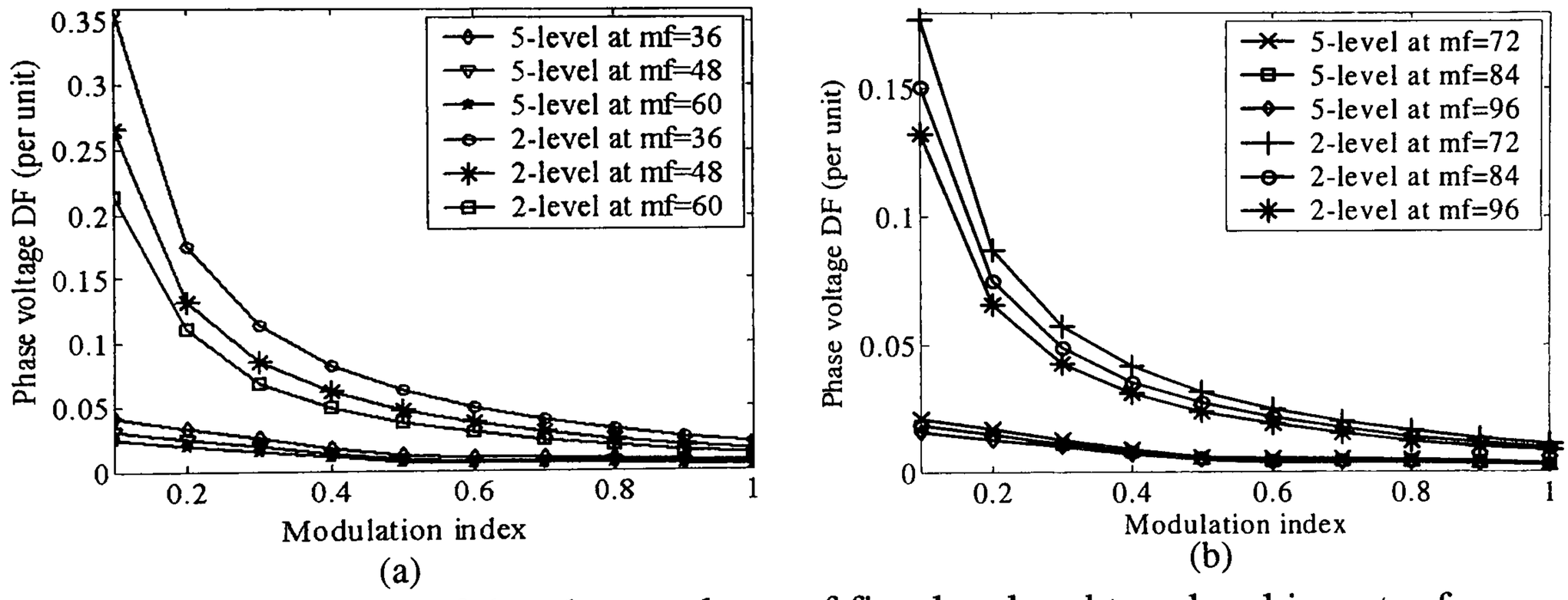
the same modulation frequency ratio). The two-level inverter has a better line voltage DF than the multilevel inverter at modulation indices of less than 0.4.

Figures (3.12) shows the harmonic spectrum for the output phase and line voltages for the five-level and two-level inverters, respectively. The modulation index range is 0.1 to 1 in 0.1 steps.



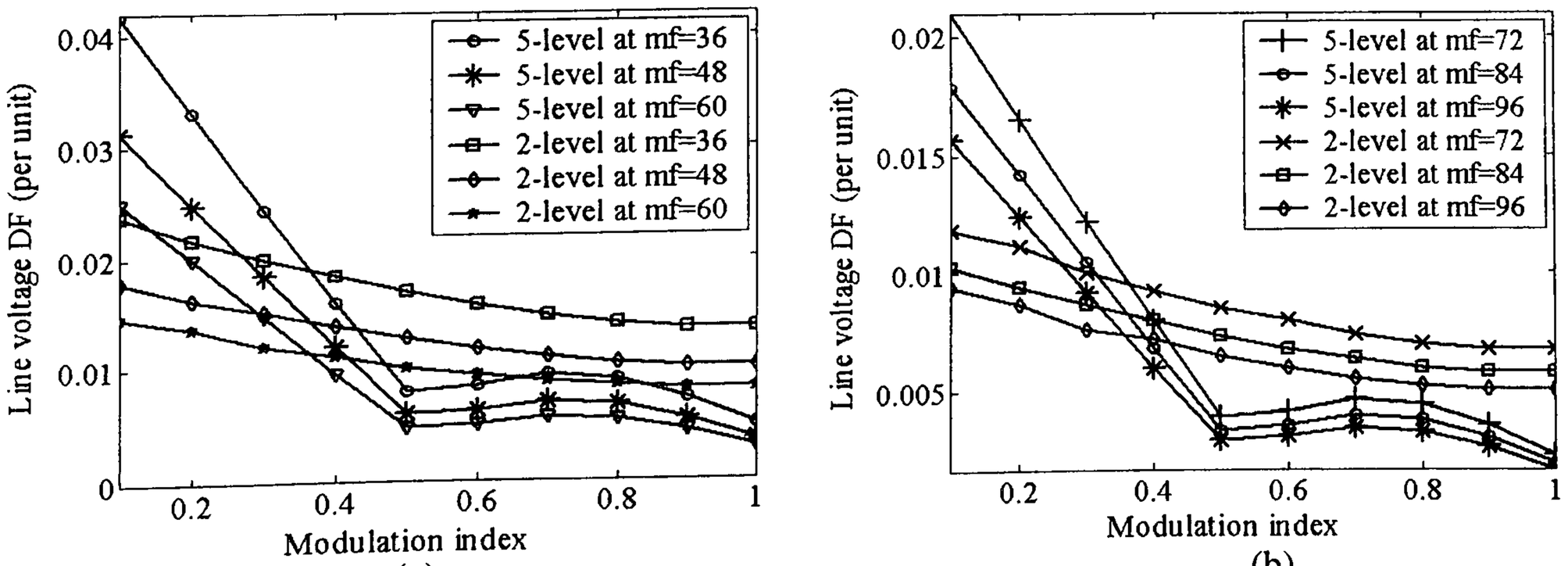
(a) (b)

Figure 3.9. THD for five-level and two-level inverter
(a) Phase voltage THD and (b) Line voltage THD



(a) (b)

Figure 3.10. DF of the phase voltage of five-level and two-level inverter for
(a) $m_f = 24$, 36, 48, and 60 (b) $m_f = 72$, 84, and 96



(a) (b)

Figure 3.11. DF of the line voltage of five-level and two-level inverter for
(a) $m_f = 24$, 36, 48, and 60 (b) $m_f = 72$, 84, and 96

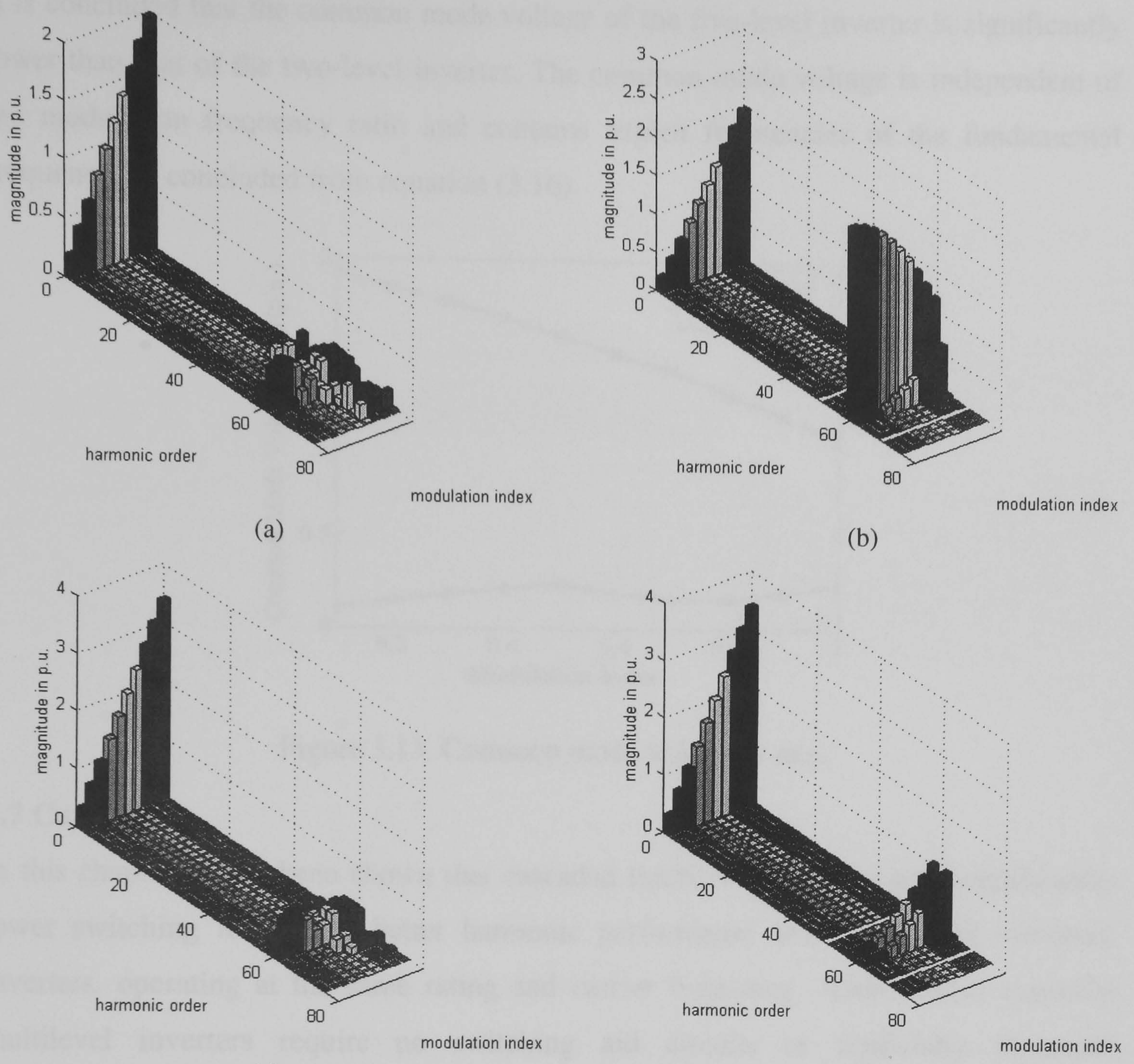


Figure 3.12. Spectrum at $m_f = 60$
Phase voltage (a) five-level and (b) two-level inverter
Line voltage (c) five-level and (d) two-level inverter

3.6 Common mode voltage

If the load neutral is isolated (as in star connected machines), the common mode voltage is defined as the load neutral-to-ground voltage. The disadvantage of a common mode voltage is that it circulates current through the stray capacitance between the neutral and ground (e.g. the capacitance between the motor outer frame and the winding)[3.24],[3.25]. This current causes EMI and may harm machine bearings. The common mode voltage is defined as:

$$v_{cm}(t) = \frac{v_{ao}(t) + v_{bo}(t) + v_{co}(t)}{3} = v_{no}(t) \tag{3.16}$$

where $v_{no}(t)$ is the voltage difference between the load neutral and ground. The r.m.s. value of the common mode voltage for the two-level and five-level inverter, at different modulation frequency ratios (24, 36, 48, 60, 72, 84, and 96), are shown in figure (3.13).

It is concluded that the common mode voltage of the five-level inverter is significantly lower than that of the two-level inverter. The common mode voltage is independent of the modulation frequency ratio and contains triplen frequencies of the fundamental frequency, as concluded from equation (3.16).

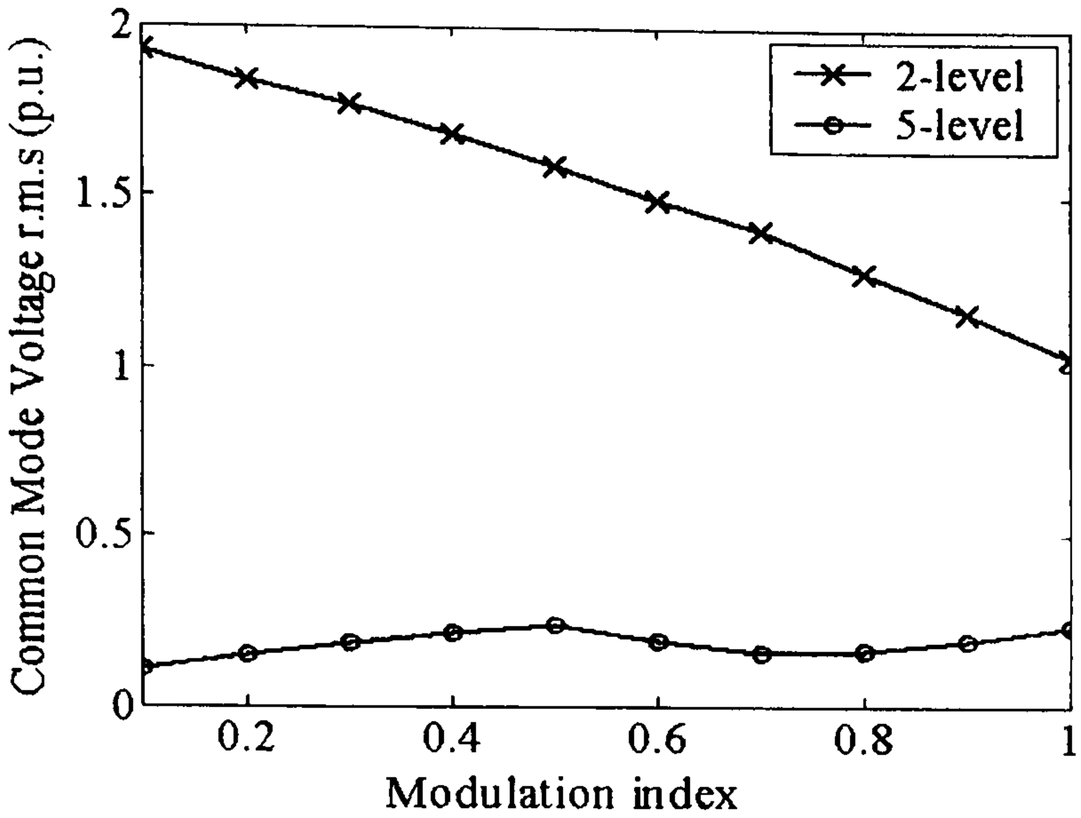


Figure 3.13. Common mode voltage, r.m.s.

3.7 Conclusion

In this chapter, it has been shown that cascaded multilevel inverters give significantly lower switching losses and better harmonic performance than equivalent two-level inverters, operating at the same rating and carrier frequency. Additionally, cascaded multilevel inverters require no switching aid circuits or artificially increased commutation times to achieve equal voltage sharing between semiconductor devices. Comparisons of the output waveforms have been based on THD and DF, as figures of merit. The THD figures for multilevel inverters are better than those of the equivalent two level inverters, for both phase and line voltages. When DF is considered, it is seen that the phase voltage DF for the multilevel inverter shows significant improvements over a two-level inverter for all modulation indices. The line voltage DF for both multilevel and two-level waveforms is improved relative to the phase voltage due to better harmonic cancellation. Line voltage harmonic cancellation does not act advantageously on the multilevel inverter and two-level waveforms are better for modulation indices below 0.4. Generally, it is concluded that for high-voltage high-power applications, when the rail voltage exceeds the rating of a single switch, the multilevel inverter offers advantages in terms of improved harmonic performance and reduced switching loss. This is counterbalanced by multilevel drawbacks such as, isolated DC power supplies for the cascaded type, balancing of the capacitors and the increased number of clamping diodes used in neutral point clamped version, and

balancing of the capacitors and the increased number of flying capacitors used in the flying capacitor type. Table 3.3 indicates facets of comparison between two-level and multilevel inverters.

Table 3.3. Facets of comparison between the 2-level and 5-level three phase inverter

	Two level	Multilevel
Number of semiconductor devices	24	24
Gate drives	24 with more complexity to ensure the transient balance	24
Isolated DC power supply	Does not need to be isolated	6
Conduction loss	The same	
Switching loss	Higher	Lower
THD	Higher	Lower
DF	Higher	Lower
dv/dt	Higher	Lower
Common mode voltage	Higher	Lower

Note the figures expressed in this table are based on the case investigated in this chapter

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Chapter 4

Overview of Hardware and Software Platforms

The software and hardware components of the system are described in this chapter. Figure (4.1) shows the hardware test rig used for the experimentation. To provide a flexible system, a high power TMS320C6701 DSP is combined with an expansion daughter board which has additional analogue interfaces and FPGA functions. The FPGA allows the synthesis of additional peripheral functions necessary for power applications. This produces a powerful configurable platform for the development of inverter control applications. The hardware, software, and recording systems incorporate:

Hardware system

i. Digital signal processor (DSP)
ii. Analogue expansion daughter board (AED)
iii. Antialiasing filter
iv. Current and voltage transducers
v. Insulated gate bipolar transistors (IGBT) and their gate drive circuits.

Software system

i. Code composer for the DSP
ii. Xilinx (foundation series) for the AED
iii. Matlab/Simulink V6.5 for simulation

Recording system

i. Digital oscilloscope

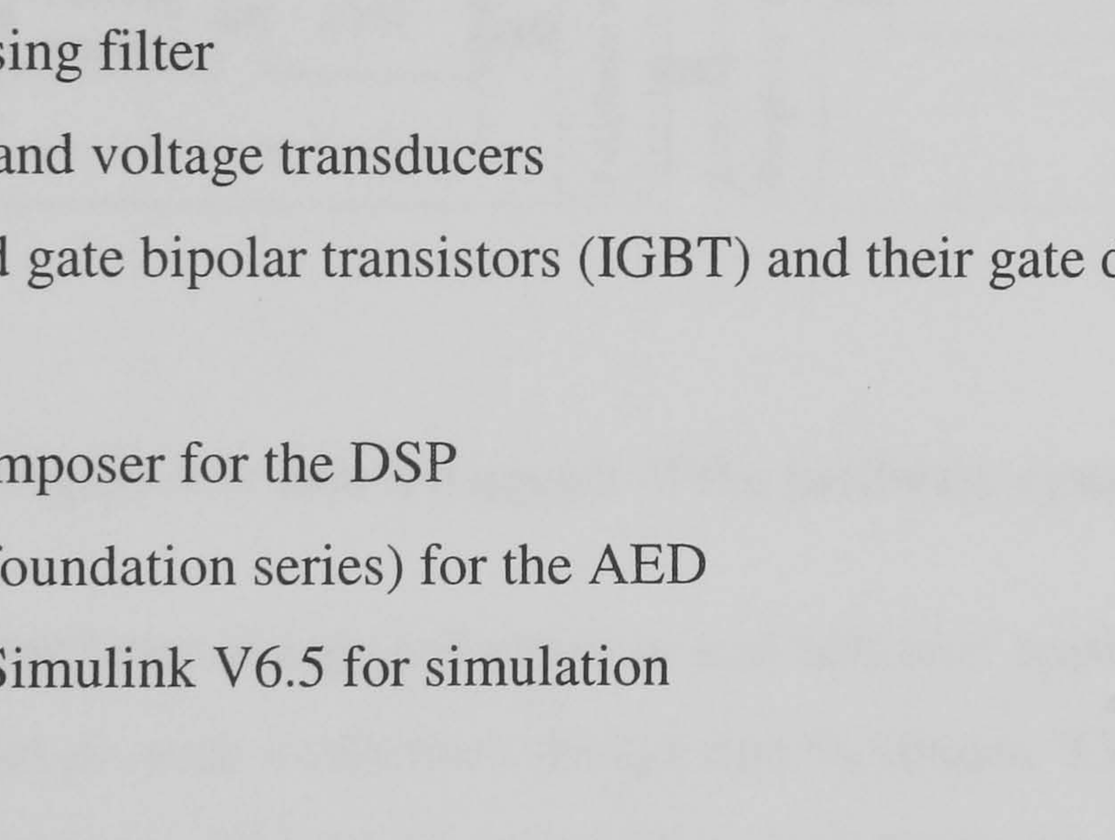

Figure 4.1. The test rig used in the experiments

4.1 Hardware

The main hardware components are shown in figure (4.2).

4.1.1 Texas Instruments TMS320C6701 Evaluation Module

All the algorithms are executed in the Texas Instruments TMS320C6701 evaluation module (EVM) shown in figure (4.3). The EVM is a low-cost, general-purpose platform for the development, analysis, and testing of 'C6X digital signal processor (DSP) algorithms and applications [4.1].

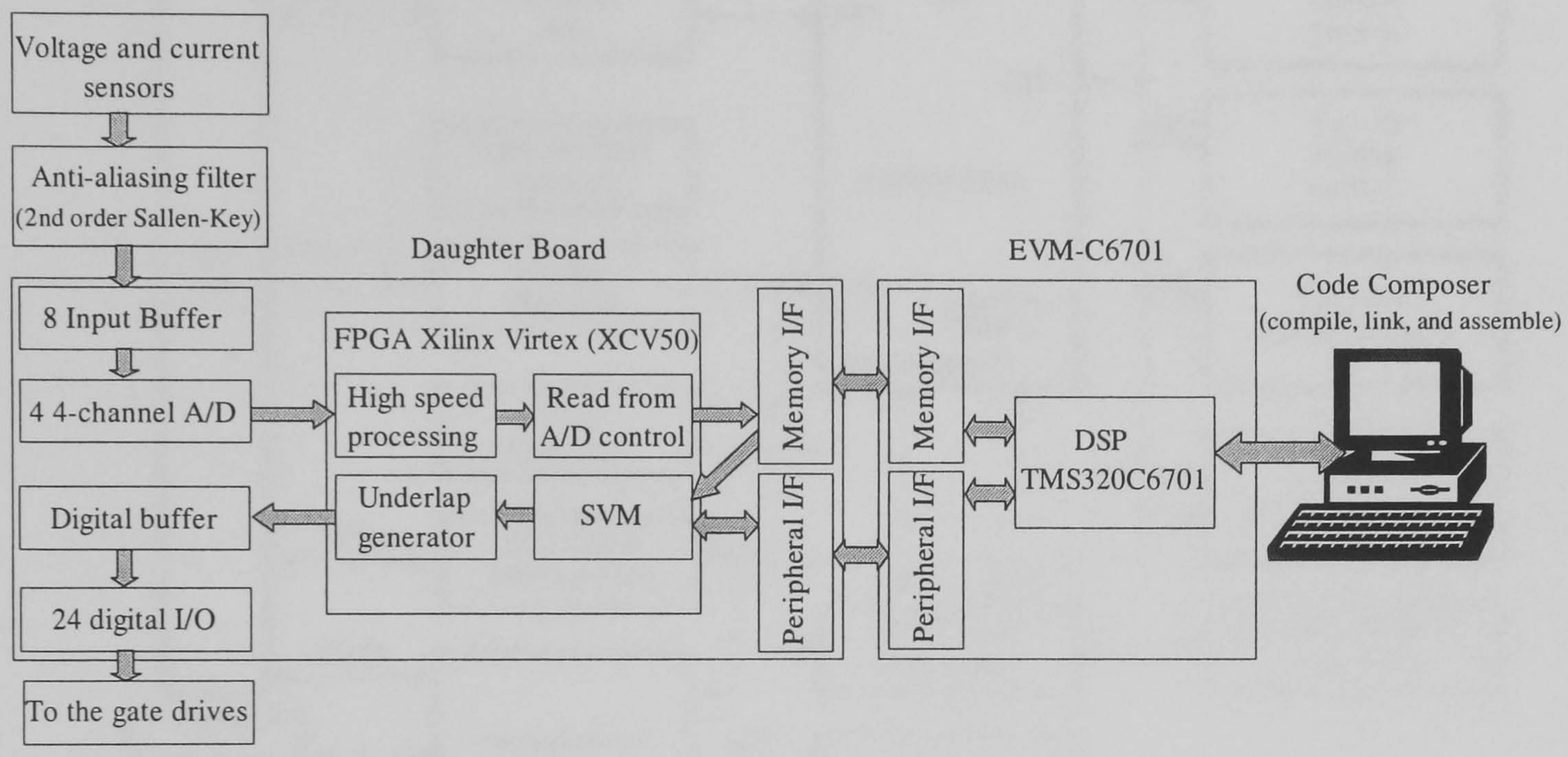

Figure 4.2. Block diagram of the hardware system

The 'C6701 EVM hardware design information and software application programming interfaces (APIs) also provide a reference design that facilitates 'C6701-based hardware and software development. The EVM is bundled with Code Composer, Windows 98 and NT drivers, host PC and DSP software APIs, example applications with source code, and various utility applications. The hardware and software bundle provides an integrated package that allows quick evaluation of the 'C6701 DSP's performance and developed custom applications.

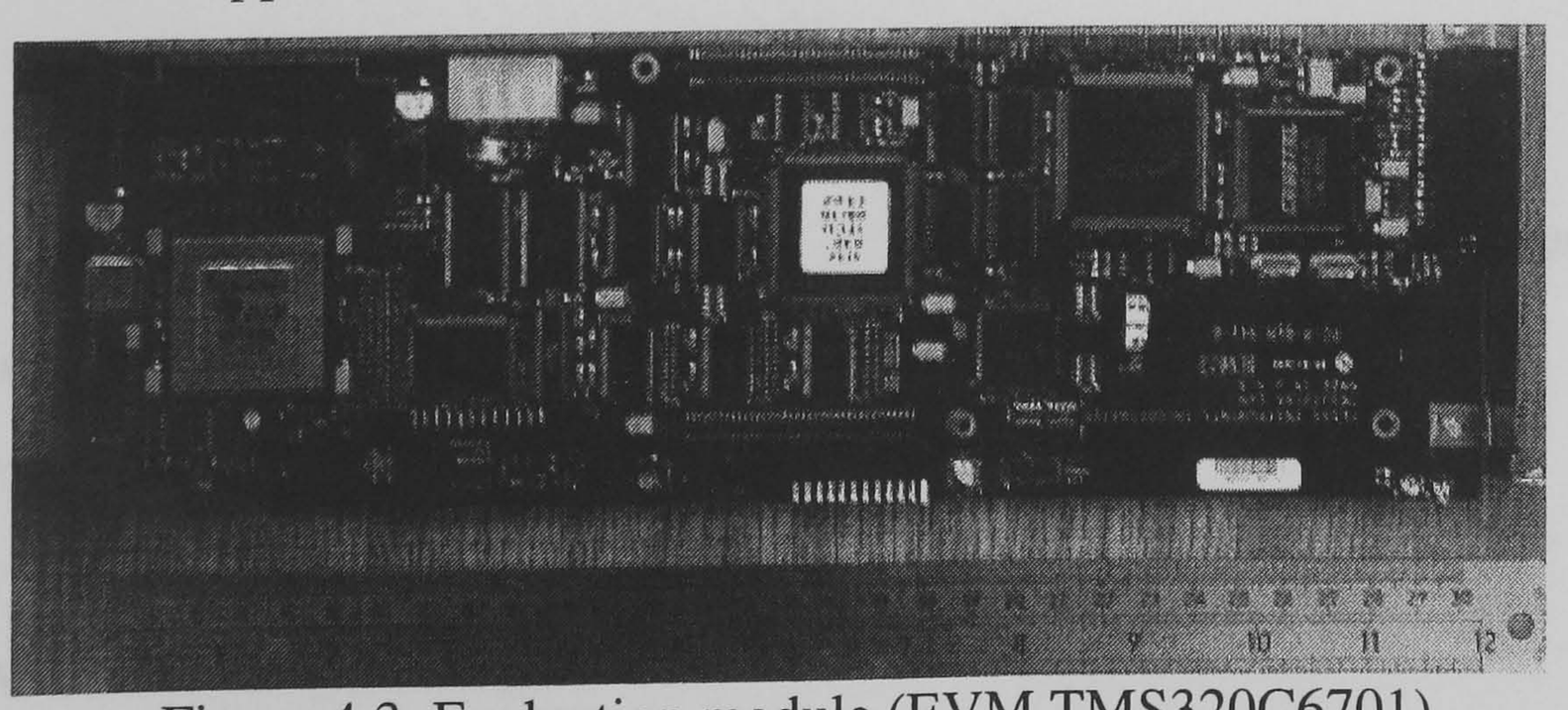

Figure 4.3. Evaluation module (EVM TMS320C6701)

TMS320C6701 EVM Hardware Functional Overview

Figure (4.4) shows the basic functional block diagram and interfaces of the 'C6701 EVM. The EVM hardware has 13 functional areas.

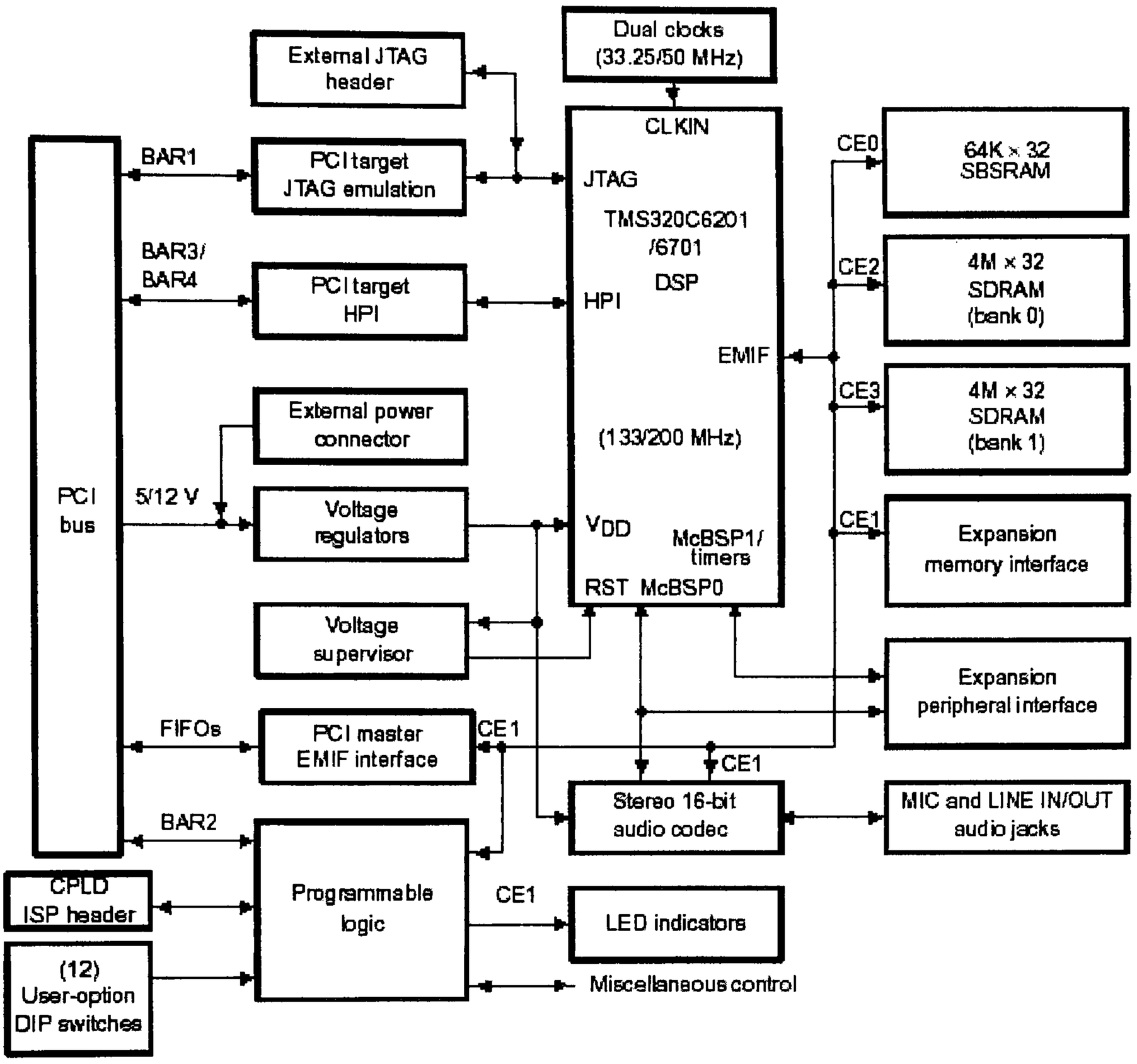

Figure 4.4. TMS320C6701 EVM Block Diagram

i. DSP TMS320C6701 Key Features [4.2]

- Launched at 167MHz; 1336 MIPS and 1 GFLOPS
- Executes up to 8 instructions in single cycle (6 float, 2 integer).
- 128K RAM on-chip (split 64K program / 64K data).
- Six ALUs
- Two 16-bit Multipliers (32 bit Result)
- Load Store Architecture with 32 32-Bit General Purpose Registers
- 32-Bit External Memory Interface to Synchronous/Asynchronous Memories
- Four Channel Boot loading Direct Memory Access Controller
- Thirty-two 32-bit registers
- 16-Bit Host Port Interface
- Two 32 bit General Purpose Timers
- All instructions may be conditional.

- Efficient compilation of C code.
- Data is byte-addressable. (It can be 8-bit, 16-bit or 32-bit).
- Single-cycle IEEE floating point (single precision)
- Efficient double precision

ii. DSP clocks

The EVM supports operation with two different onboard clock sources (OSC A at 25 MHz and OSC B at 33.25 MHz) and two clock modes (multiply-by-1 and multiply-by-4). As a result, the DSP can operate at four different clock rates, including OSC A, OSC A x 4, OSC B, or OSC B x 4 [4.2]. The clock rate used is OSC A x 4 at 100 MHz

iii. External memory

The EVM provides one bank of 64K, 133-MHz SBSRAM and two banks of 4M, 100-MHz SDRAM [4.3]. Additional asynchronous memory can be added with a daughterboard using the expansion memory interface. All external memory devices are byte addressable.

iv. Expansion interfaces

The EVM provides external memory interface and external peripheral interface connectors that enable the use of a custom or third-party daughterboard [4.4]. The memory interface supports asynchronous memory transfers, and the peripheral interface provides daughterboard use of the DSP internal peripherals.

v. DMA

Four DMA channels enable data to be transferred from memory-to-memory, and between memory and I/O devices, without CPU intervention [4.5]. This is particularly beneficial for handling I/O to and from the Multi Channel Serial Ports. Additionally, the DMA engines may support channel sorting for use with the Multi-Channel Serial Ports.

vi. PCI interface

The EVM includes a PCI Local Bus Revision 2.1-compliant interface that enables host access to the onboard JTAG controller, DSP host port interface (HPI), and board control/status registers [4.6]. The EVM's PCI interface allows source debugging with the 'C6x EVM without requiring an XDS510 emulator, as well as host software access to all of the DSP memory space via the PCI bus. The DSP can also master the PCI bus to transfer data to and from the host memory.

vii. JTAG emulation

The EVM provides embedded JTAG emulation, using an onboard test bus controller (TBC), as well as a header to support an XDS510 JTAG emulator [4.7]. This allows source debugging over the PCI bus without requiring an emulator or by using an XDS510 emulator when operating stand-alone on a desktop.

viii. Programmable logic

The EVM's CPLD provides the board's glue logic and control/status registers [4.1].

ix. Audio interface

The EVM includes a CD-quality, 16-bit audio interface with stereo microphone and line-level inputs and a stereo line-level output [4.1]. A multimedia audio codec is used that supports all popular sample rates from 5.5kHz to 48 kHz. The audio circuit includes an op-amp based microphone preamplifier. Three 3.5 mm audio jacks are located on the board's mounting bracket.

x. Power supplies

The EVM uses voltage regulators to provide 1.8 V for the DSP core, 3.3 V for the DSP I/O, memories, CPLD, and buffers, and 5 V for audio components. The PCI bus or external power connector's 5 V is used for all other digital components [4.8]. The PCI bus or external power connector's 12 V is used for the input to the 5 V regulator. Efficient switching regulators are used for the 1.8/2.5 V and 3.3 V, and a low-power linear regulator is used to generate the analog 5 V.

xi. Voltage supervision and reset control

The EVM uses a voltage supervisor to monitor the board's voltages and provide a board reset signal [4.1]. The CPLD also includes logic related to reset control with inputs from a manual reset pushbutton, the PCI controller, and software reset control signals.

xii. User options

The EVM supports user option control via 12 onboard DIP switches or with direct control by host software via the PCI bus. The user options include the boot mode, clock mode, clock select, JTAG select, and endian mode. Three user-defined options are also provided.

xiii. LED indicators

The EVM provides three LED indicators. A single green LED is illuminated whenever 5 V is applied to the board. Two red LEDs can be used for user-defined status, with one located on the board's mounting bracket and the other located at the top of the board.

Operating Scenarios

The EVM can operate in a computer motherboard's full-size PCI slot or stand alone on a desktop or lab bench. Because the 'C6701 EVM does not have onboard ROM, applications are loaded by host software using the board's embedded JTAG or DSP HPI interfaces over the PCI bus or by an XDS510 emulator connected to the board's 14-pin JTAG header. A daughterboard with nonvolatile memory can be designed to provide the 'C6701 EVM with a ROM boot capability that enables it to boot an application itself upon reset in both operating scenarios.

i. PCI operation.

When the EVM is installed in a PCI slot, host software can control and monitor it via memory-mapped registers. The host software can also access the onboard JTAG test bus controller (TBC) to download code and access the DSP, as well as transfer data to and from the DSP using the 'C6701 HPI. Code Composer uses the JTAG TBC to access the board, and the 'C6701 EVM COFF loader uses the HPI. An XDS510 can be used with the board in a PCI slot, but it is not needed because onboard emulation control is provided.

ii. Stand-alone operation.

When the EVM is operated in a stand-alone configuration, an XDS510 or XDS10WS emulator with the standard 'C6701 Code Composer (not the 'C6701 EVM debugger included in the kit) is typically used to load applications and control the board. In stand-alone operation, the PCI interface is disabled, so the onboard JTAG, TBC, and HPI interfaces are not available.

4.1.2 AED-106 Multi-Channel Parallel Daughterboard

The SIGNALWARE AED-106 Multi-Channel Parallel Analog Expansion Daughterboard (AED) for the Texas Instruments TMS320C6701 Evaluation Module provides a multiple sensor interface [4.9]. Figure (4.5) shows the AED. The daughterboard has four 4-channel A/D converters that can monitor a variety of sensor outputs where simultaneous sampling is required. In addition to the analog channels,

three groups of 8 buffered digital signals can be switched to either input or output. Breadboard space is provided for constructing signal conditioning and interface circuits.

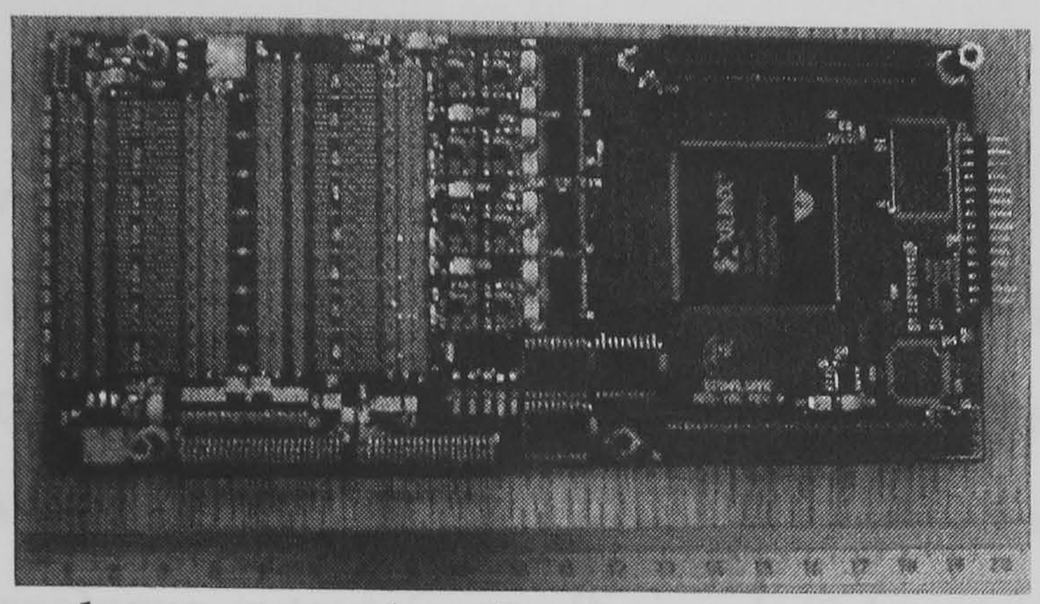

Figure 4.5. The analogue expansion daughter board (AED 106) used with the TMS320C6701

Each of the four A/D converters can sample up to 4 single-ended or 2 differential channels simultaneously, with 12-bit resolution and 1.25 MS/s on each channel. Single channels can be sampled up to 6 MS/s. The bias voltage of the A/D is 2.5 V.

The configuration also includes voltage reference, digital buffers, amplifiers, regulators, programmable logic interface, and 90 pins on I/O connectors for off-board connections. The AED-106 comes with a demonstration logic program and software for the DSP.

Preprocessing of the A/D samples and control of the converters with the Field Programmable Gate Array (FPGA) significantly reduces the load on the DSP, making more computation possible with a single C6701 DSP. The FPGA is a Xilinx Virtex™ XCV50-4 with 57,906 logic gates (2034 flip-flops, 57K RAM bits).

Digital I/O and External Synchronization:

- 24 - Buffered TTL Input/Outputs up to 100 MHz
- Switchable to input or output in groups of 8.

4.1.3 Anti-aliasing filters

The Nyquist theorem states that any signal can be reconstructed if it is sampled at greater than twice the frequency of the highest frequency component of that signal. All frequency components of a sampled signal greater than or equal to one half the sampling frequency will be folded back into the band between DC and half the sampling frequency. This means that all signals, including noise, need to be low pass filtered before they are sampled. This filter is called an anti-aliasing filter [4.10].

For designing an anti-aliasing filter, there are some parameters which define it [4.10], sampling frequency, highest frequency of interest, and desired signal to noise ratio. The

anti-aliasing filter used is a Sallen-Key 2nd order low pass filter, tuned for a 32 kHz corner frequency.

4.1.4 Current and voltage sensors

i. Current transducer

The LEM type LTA 100-P/SP1 is a transducer employing the Hall effect to measure DC and complex waveform AC currents in a non-invasive manner [4.11]. Figure (4.6) shows the current transducer used. Galvanic isolation is provided between the primary (measured) and the analogue output (control) signal. Table 4.1 indicates the nominal parameters of the transducer used.

Table 4.1. The current transducer nominal parameter values

Nominal current	100 (r.m.s.)	A
Current output	1	mA/Amp
Measuring range	0 to ± 160	A
Frequency range	DC to 100 (-1dB)	kHz
di/dt	>50	A/μs

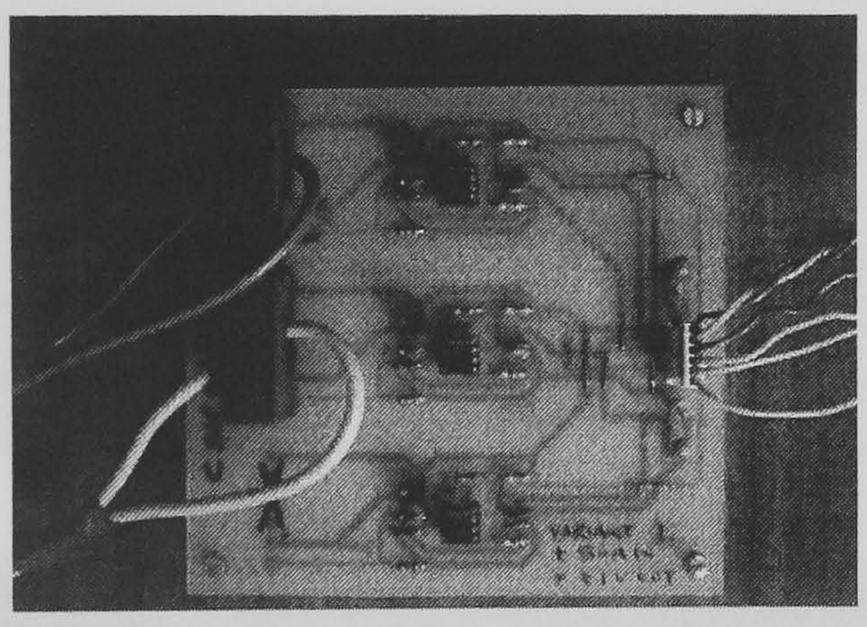

Figure 4.6. The current transducers

ii. Voltage transducer

The LEM voltage transducer LV 25-P uses the Hall effect to measure DC, AC, and pulsed voltage with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit) [4.12]. Figure (4.7) indicates the voltage transducer used while Table 4.2 indicates the nominal parameter value of the transducer used.

Table 4.2. The voltage transducer nominal values

Primary nominal current	10 (r.m.s.)	mA
Primary current (measuring range)	0… ± 14	mA
Primary nominal voltage	10... 500	V
Bandwidth	Drop resistor dependent	
Accuracy	± 0.8	%

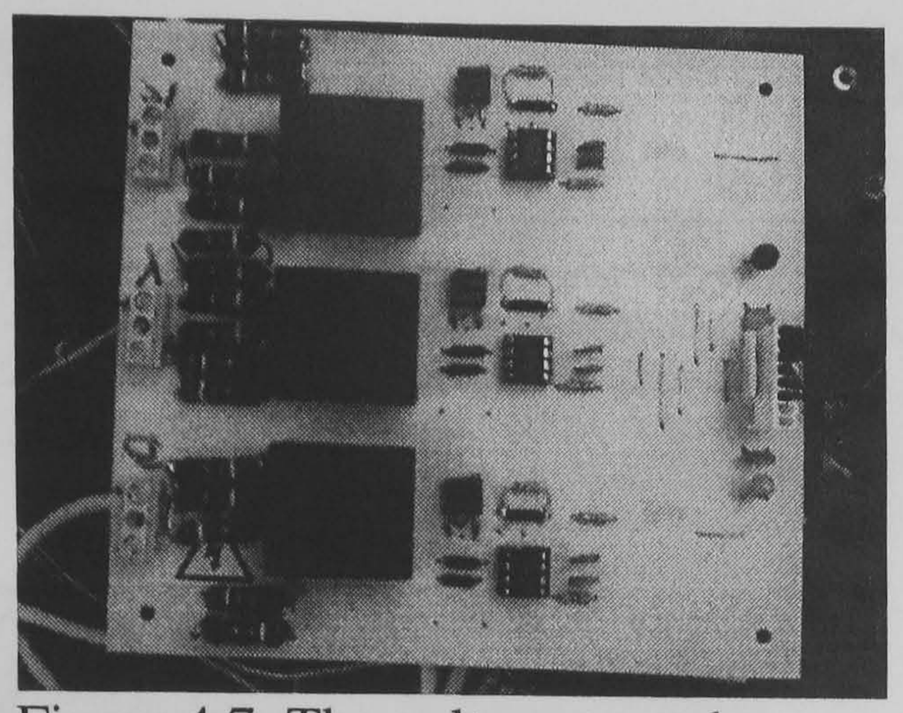

Figure 4.7. The voltage transducers

4.1.5 IGBT inverter and gate drive circuits

(a) Gate drive circuits

The gate drive circuit provides isolation between the control signal and the IGBT gate by means of two transformers. One transformer is for transmitting power from the low side circuit and the other is for transmitting the gate drive signal. Figure (4.8) indicates the gate drive used. Table 4.3 indicates the parameters of the gate drive

Table 4.3. The gate drive parameters

Supply voltage (max)	5.25	V
$t_{d\ on}$ (typ.)	60	ns
$t_{d\ off}$ (typ.)	60	ns
Drive signal frequency (max)	75	kHz
Output voltages	0, 15	V
Output current	$\pm$ 3	A

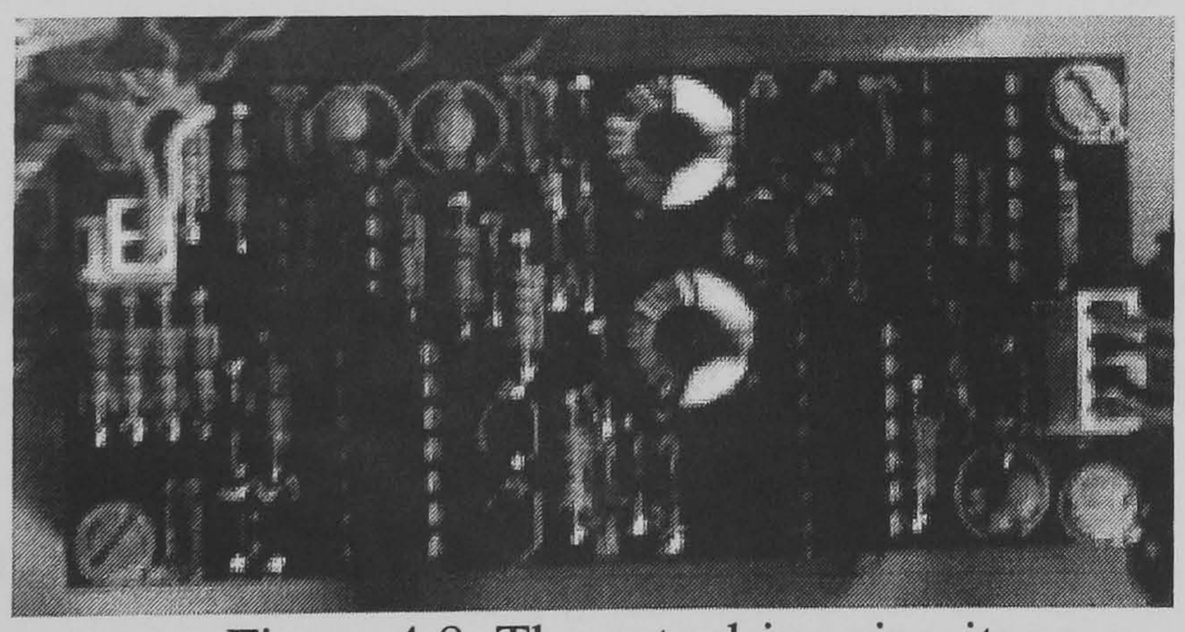

Figure 4.8. The gate drive circuit

(b) Inverter

A BSM 100 GD 120 DN2 solderable power module from Siemens, including a fast freewheeling diode, is used for the multilevel inverter operations. It is packaged with an insulated metal base as shown in figure (4.9), whilst Table 4.4 indicates its main parameters.

Table 4.4. The IGBT module BSM 100 GD 120 DN2

V_{CE}	1200	V
I_c (80 C^o)	100	A
$t_{d\ on}$ (max)	320	ns
t_r (max)	160	ns
$t_{d\ off}$ (max)	520	ns
t_f (max)	100	ns

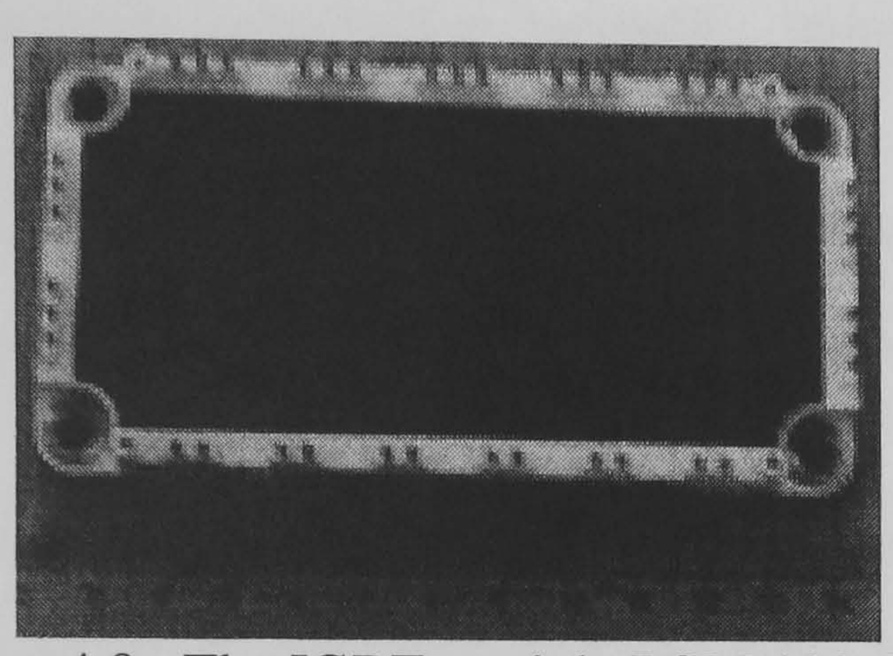

Figure 4.9. The IGBT module BSM 100 GD 120 DN2

BSM 35 GD 120 DN power module with parameters as in Table 4.5 is used for the two-level active power filter.

Table 4.5. The IGBT module BSM 35 GD 120 D2

V_{CE}	1200	V
I_c (80 C^o)	35	A
$t_{d\ on}$ (max)	120	ns
tr (max)	120	ns
$t_{d\ off}$ (max)	600	ns
t_f (max)	75	ns

4.2 Software

The software can be divided into two parts. The first part is used for simulation and modelling of the system and the second part, which is used in conjunction with the hardware for implementing the experimental prototype of the system.

4.2.1 TMS320C6x EVM Software Functional Overview

The EVM software consists of host support software and DSP support software. The host support software supplied includes the following Win32 host utilities and libraries. The host utilities and libraries run on an Intel-compatible PC under either Windows 98 or Windows NT 4.0.

i. Board configuration utility (evm6xrst.exe)

This utility is used to reset and configure the board.

ii. Code Composer

Code composer is the software debugger used to debug (compile, assemble, and link) 'C6701 software. The code composer runs on the host PC and is a fully integrated development environment (IDE). It has the following features.

- Contains a profiler, useful for debugging and determining timing of steps
- Project management, compilation, assembly, linking, loading [C complier, not C++]
- A development environment that integrates all tools into a single application
- Real-time analyses tools for monitoring program interactions without halting the processor
- Profile-Based Compiler for optimising code size and performance
- Visual Linker for graphically arranging program code and data in memory
- Data visualization for viewing signals in multiple graphical formats
- Real-time bi-directional application data visibility through Real Time Data exchange (RTDX) technology

iii. EVM confidence test utility (evm6xtst.exe).

This utility tests the basic operation of the board.

iv. COFF loader utility (evm6xldr.exe).

This utility is used to load and execute 'C6x software.

v. EVM Win32 DLL (evm6x.dll).

The Win32 host libraries consist of a Windows 98 and a Windows NT version of evm6x.dll, which provides user software access for control and communication with the EVM board.

4.2.2 FPGA (Xilinx Virtex XCV50)

Xilinx software "Foundation series 3.1i" is used. The schematic flow supports top-level schematic design with the Xilinx unified libraries components, LogiBLox symbols, CORE generated modules, and ABEL, HDL and/or state machine macros. The schematic design is used with CORE generated modules.

4.2.3 Simulation software

The software used for simulation is the MATLAB/SIMULINK 6.5 package from MathWorks [4.13].

i. MATLAB

MATLAB integrates mathematical computing, visualization, and a powerful language to provide a flexible environment for technical computing [4.14]. The open architecture makes it easy to use MATLAB and its companion products to explore data, create algorithms, and create custom tools that provide insight.

ii. Simulink

Simulink is an interactive tool for modelling, simulating, and analyzing dynamic, multidomain systems [4.15]. It allows accurate description, simulation, evaluation, and refinement of a system's behaviour through standard and custom block libraries. Simulink integrates seamlessly with MATLAB, providing immediate access to an extensive range of analysis and design tools. These benefits make Simulink a suitable tool for control system design, signal processing system design, communications system design, and other simulation applications.

4.3 Recording system

4.3.1 Tektronix TDS3032B Oscilloscope Measurements/Features

The digital phosphor oscilloscope [4.16] used is a TDS3032B from Tektronix, as shown in figure (4.10) and its characteristics are shown in Table 4.6.

Table 4.6. Tektronix TDS3032B Performance Characteristics

Bandwidth	300	MHz
Number of Channels	2	channels
Simultaneous Maximum Sampling Rate/ch	2.5	GSa/s
Max. Single Shot bandwidth	300	MHz
Min. Vertical Sensitivity	1	mV/div
Maximum Vertical Sensitivity	10	V/div
Number of Bits	9	Bits
Input Impedance	1	MOhm
Input Impedance (alternate)	50	Ohm
Input Coupling	AC,DC,GND	
Maximum Input Voltage	150	Vrms
Main time base – lowest	2	ns/div
Main time base – highest	10	s/div
Time base accuracy	0.002	%
Minimum Trigger Hold off	13.2	ns

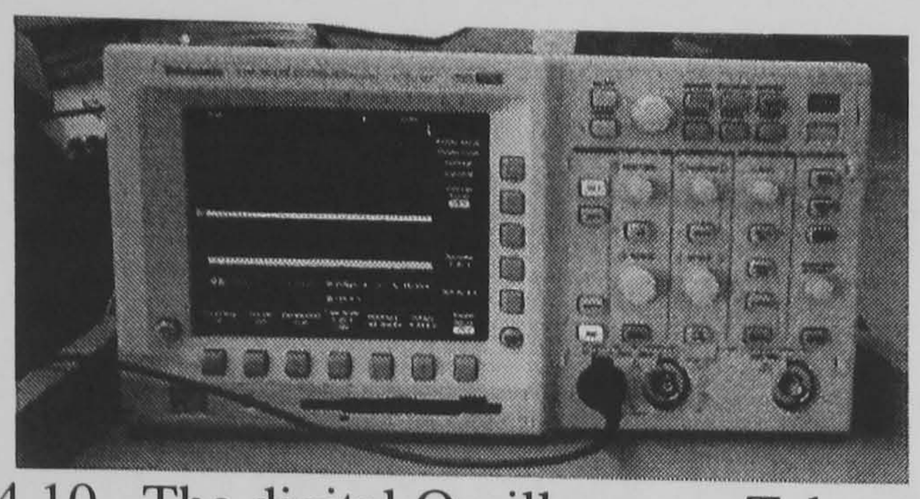

Figure 4.10. The digital Oscilloscope, Tektronix TDS3032B

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Chapter 5

Generalized Theory of Multilevel Space Vector Modulation

Although offering potential advantages, the application of space vector modulation (SVM) to multilevel inverters has been limited. This is due to the fact that the number of available switching states increases rapidly with the number of levels. In this chapter, an algorithm is proposed for multilevel space vector modulation, which is applicable to any number of levels. The algorithm is based on numerical analysis and gives a fast, fixed execution time when DSP implemented, irrespective of the number of levels. The algorithm reduces the complexity faced in multilevel SVM implementation. A visualization of the multilevel SVM analysis is detailed, without using any representative technique. Alternative paths can be readily utilized. The proposed algorithm caters for over modulation and minimum pulse, and is validated by Matlab/Simulink simulations and practical implementation. It will be shown that this algorithm is readily codable and time efficient.

5.1 Multilevel Space Vector Modulation

Multilevel inverters employ different modulation control techniques, as discussed in chapter two. Space vector modulation (SVM) for multilevel inverters is considered as an extension of space vector modulation for the two-level voltage source inverter. The SVM technique involves vectorially equating the volt-second integral between a desired reference voltage vector and the nearest three states in space which are realizable by the inverter. Compared to sinusoidal PWM techniques, SVM offers improved DC bus utilization, reduced commutation losses, and lower total harmonic distortion (THD). The SVM concept for the simple two level voltage source inverter has been discussed extensively [5.1]-[5.41]. SVM for multilevel inverters has been considered and part of the literature is devoted to SVM for three-level inverters [5.42]-[5.57], while [5.58]-[5.69] consider the generalization of multilevel SVM.

In [5.58], the algorithm uses 60^0 coordinates instead of cartesian coordinates. In [5.61], the algorithm is based on decision-based PWM developed by Holtz. The vector localization depends on iterative vertical and horizontal searching, starting from an initial condition. The algorithm in [5.62] is based on choosing an appropriate coordinate system. The algorithm in [5.65] determines the sector and times, based on classification techniques such as a neural network.The algorithm in [5.67] defines the line voltage in a three-dimensional Euclidean vector space, which adds complexity. No method gives a

systematic approach to the generation of multilevel SVM, considering DSP-implementation with a fast, fixed execution time, irrespective of the number of levels, with extension to over modulation and pulse deletion avoidance. This chapter presents such an algorithm.

The algorithm procedures can be summarized as follows:

i. Generating the states of the space vector for any number of levels because as the number of levels is increased, the number of states is greatly increased. Generally, the number of states is m^3 in an m-level inverter where m is the number of levels in the phase voltage. For example, there are 125 states for the 5-level inverter.
ii. Processing for the vector location in the vector space is increased with increased number of levels. Generally the number of different triangles is $6(m-1)^2$. For example, there are 96 triangles for the 5-level inverter.
iii. Distribution of the sampling time between the nearest three states.
iv. Determination of the sequence of the nearest three states.
v. Making use of the alternative state sequences. Generally there are $3m(m-1)+1$ vectors and m^3 states. For example, for 5-levels there are 61 vectors (a zero vector, 6 vectors in the first hexagon, 12 vectors in the second hexagon, 18 vectors in the third hexagon, and 24 vectors in the fourth hexagon) and 125 states.

The proposed generalized algorithm for multilevel space vector modulation to overcome these difficulties, is shown in the flow chart in figure (5.1). The following sub-sections clarify each step of the algorithm.

5.1.1 State matrix generation

The states are represented in $m-1$ two-dimensional matrices and a zero state vector. These matrices can be generalized for any number of levels. Figure (5.2) represents the space vectors for two, three, and five levels. From these figure parts, the state vector matrices can be represented as follows.

i. The zero state vector

$$X(1,1,k) = [000 \quad 111 \quad 222 \quad 333 \quad \ldots\ldots\ldots \quad (m-1)(m-1)(m-1)] \tag{5.1}$$

where the dimensions of the zero state matrix are $1 \times m$. A `0′ represents the minimum voltage obtainable from the multilevel inverter and $m-1$ represents the maximum value. For example, in a two-level inverter, `0′ is equivalent to 0 V and `1′ is equivalent to $E_T$ Volts, where $E_T$ is the inverter DC link voltage. In a 3-level inverter `0′ is equivalent to -E_T Volts,`1′ is equivalent to 0 V, and `2′ is equivalent to E_T Volts where E_T is the per

unit cell voltage of the multilevel inverter. The symbol k represents the number of alternative states.

ii. The n-hexagon state matrices

The n-hexagon state matrices are generally represented as follows:

$$X(n+1,j,k)=\begin{bmatrix}
n00 & (n+1)11 & \ldots\ldots & (m-1)(m-n-1)(m-n-1) \\
n10 & (n+1)21 & \ldots\ldots & (m-1)(m-n)(m-n-1) \\
\vdots & \vdots & \ldots\ldots & \vdots \\
n(n-1)0 & (n+1)n1 & \ldots\ldots & (m-1)(m-2)(m-n-1) \\
 & & & \\
nn0 & (n+1)(n+1)1 & \ldots\ldots & (m-1)(m-1)(m-n-1) \\
(n-1)n0 & n(n+1)1 & \ldots\ldots & (m-2)(m-1)(m-n-1) \\
\vdots & \vdots & \ldots\ldots & \vdots \\
1n0 & 2(n+1)1 & \ldots\ldots & (m-n)(m-1)(m-n-1) \\
 & & & \\
0n0 & 1(n+1)1 & \ldots\ldots & (m-n-1)(m-1)(m-n-1) \\
0n1 & 1(n+1)2 & \ldots\ldots & (m-n-1)(m-1)(m-n) \\
\vdots & \vdots & \ldots\ldots & \vdots \\
0n(n-1) & 1(n+1)n & \ldots\ldots & (m-n-1)(m-1)(m-2) \\
 & & & \\
0nn & 1(n+1)(n+1) & \ldots\ldots & (m-n-1)(m-1)(m-1) \\
0(n-1)n & 1n(n+1) & \ldots\ldots & (m-n-1)(m-2)(m-1) \\
\vdots & \vdots & \ldots\ldots & \vdots \\
01n & 12(n+1) & \ldots\ldots & (m-n-1)(m-n)(m-1) \\
 & & & \\
00n & 11(n+1) & \ldots\ldots & (m-n-1)(m-n-1)(m-1) \\
10n & 21(n+1) & \ldots\ldots & (m-n)(m-n-1)(m-1) \\
\vdots & \vdots & \ldots\ldots & \vdots \\
(n-1)0n & n1(n+1) & \ldots\ldots & (m-2)(m-n-1)(m-1) \\
 & & & \\
n0n & (n+1)1(n+1) & \ldots\ldots & (m-1)(m-n-1)(m-1) \\
n0(n-1) & (n+1)1n & \ldots\ldots & (m-1)(m-n-1)(m-2) \\
\vdots & \vdots & \ldots\ldots & \vdots \\
n01 & (n+1)12 & \ldots\ldots & (m-1)(m-n-1)(m-n)
\end{bmatrix}$$

sector1 (rows 1–4); sector2 (rows 5–8); sector3 (rows 9–12); sector4 (rows 13–16); sector5 (rows 17–20); sector6 (rows 21–24) (5.2)

where n represents the hexagon order in which the state lies. The dimensions of the n-hexagon matrix is $6n\times(m\text{-}n)$. It is divided into 6 sub-matrices, each with dimensions of $n\times(m\text{-}n)$ corresponding to each sector. The symbol j represents the non-alternative states which lie in the hexagon and is the number of rows in the state matrix.

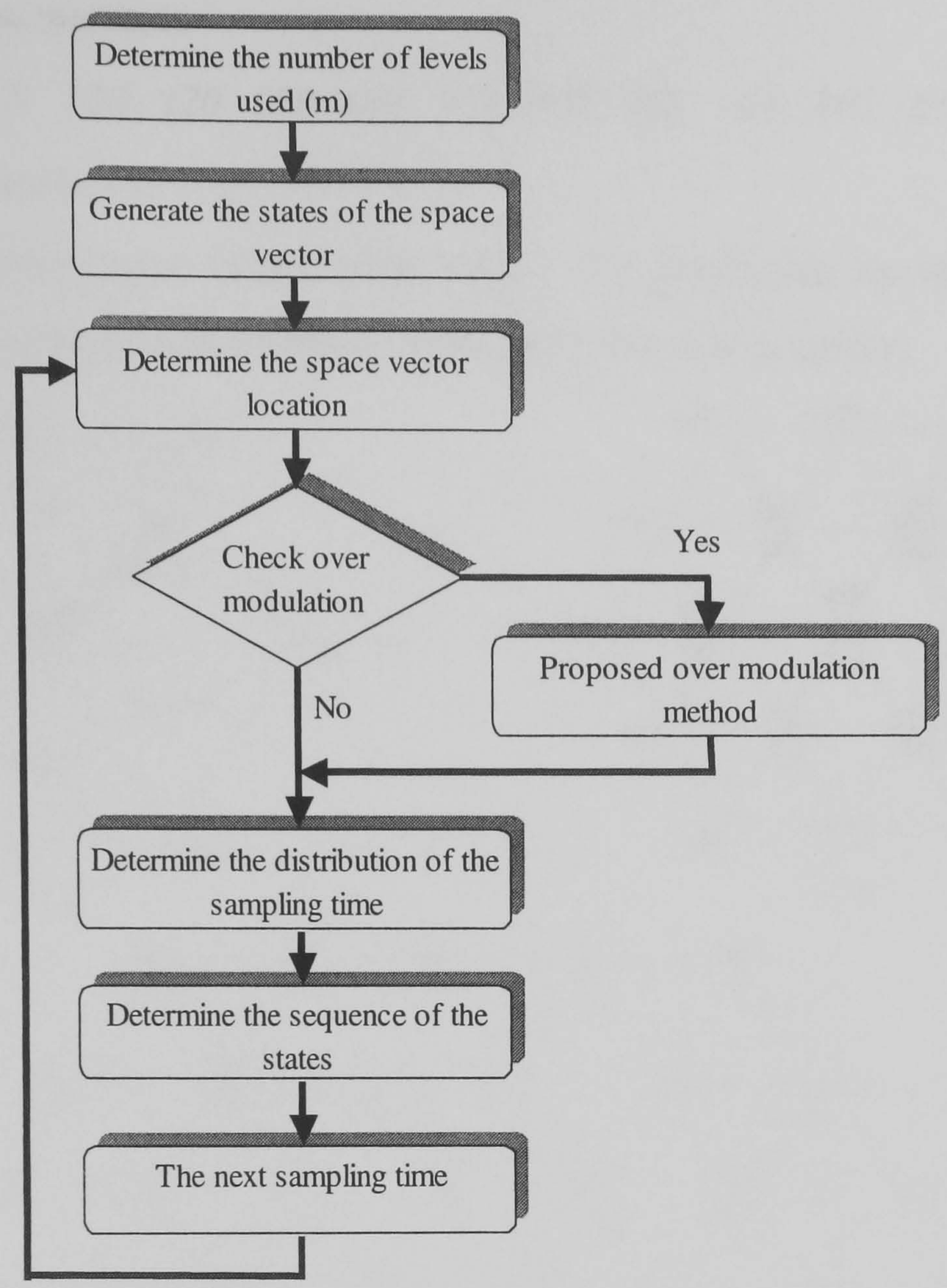


Figure 5.1. Flow chart of the proposed algorithm

The two-level inverter

There are two two-dimensional matrices. The zero state matrix is

$$X(1,1,k) = [000 \quad 111] \tag{5.3}$$

where $k = 1$ or 2, and $j = 1$.

The first and only hexagon is shown in figure (5.2a).

$$X'(2,j,1) = [100 \quad 110 \quad 010 \quad 011 \quad 001 \quad 101] \tag{5.4}$$

where $1 \leq j \leq 6$ is the number of rows and $k = 1$.

The three-level inverter

The zero state matrix is

$$X(1,1,k) = [000 \quad 111 \quad 222] \tag{5.5}$$

where $1 \leq k \leq 3$ and $j = 1$.

The first hexagon matrix is

$$X'(2,j,k) = \begin{bmatrix} 100 & 110 & 010 & 011 & 001 & 101 \\ 211 & 221 & 121 & 122 & 112 & 212 \end{bmatrix} \tag{5.6}$$

where $1 \leq j \leq 6$ and $1 \leq k \leq 2$.

The second hexagon matrix is

$$X'(3,j,1)=[200 \quad 210 \quad 220 \quad 120 \quad 020 \quad 021 \quad 022 \quad 012 \quad 002 \quad 102 \quad 202 \quad 201] \qquad (5.7)$$

where $1 \le j \le 12$ and $k = 1$.

This situation is shown figure (5.2b), while Figure (5.2c) indicates the states of the five level space vector which can be found from the previous state matrices.

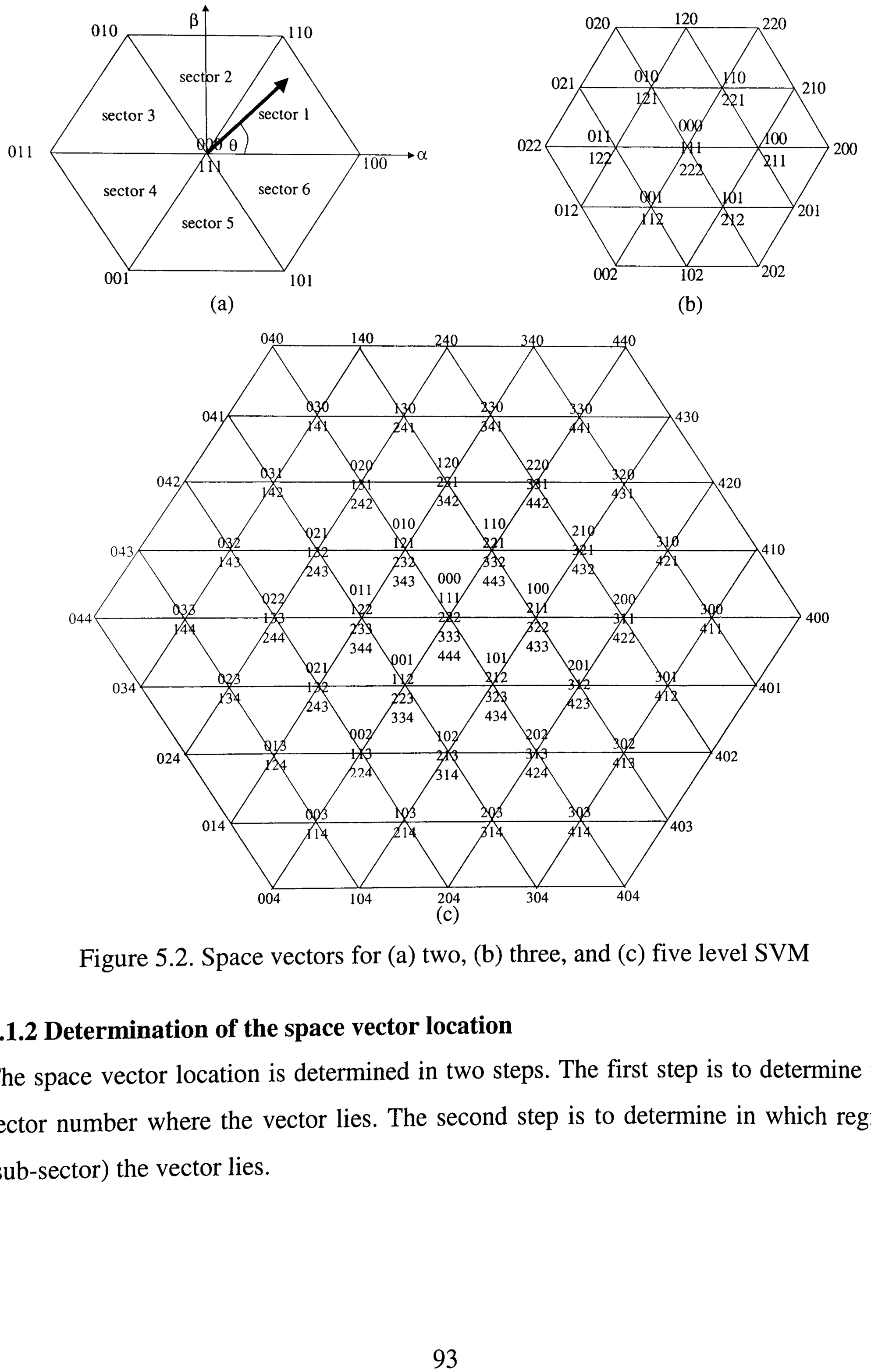


Figure 5.2. Space vectors for (a) two, (b) three, and (c) five level SVM

5.1.2 Determination of the space vector location

The space vector location is determined in two steps. The first step is to determine the sector number where the vector lies. The second step is to determine in which region (sub-sector) the vector lies.

Step 1: *The sector number (s)*

The voltage magnitude V_m is obtained from transforming the *a-b-c* frame to the α-β frame using Park's transformation, namely

$$\begin{pmatrix} V_\alpha \\ \\ V_\beta \end{pmatrix} = \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \tag{5.8}$$

Then the vector magnitude V_m and the vector angle θ can be determined from:

$$V_m = \sqrt{V_\alpha^2 + V_\beta^2} \tag{5.9}$$

$$\theta = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \tag{5.10}$$

Consequently the sector number *s* is given by

$$\mathrm{s} = \mathbf{floor}\left(\frac{\theta}{\pi/3}\right) + 1 \tag{5.11}$$

where **floor** is the function which corrects any real number to the nearest, but lower, integer number (e.g. **floor**(3.9) = 3).

Step 2: *The region number (reg)*

Three parameters identify the vector location hence determine the region number. The first parameter `h´ divides the sector horizontally as shown in figure (5.3). The second parameter `a´ divides the sector with 60-degree inclined lines. The third parameter `b´ divides the sector with 120-degree inclined lines. The maximum value that *a, b* or *h* can obtain for *m*-levels is *m-1*. Using numerical analysis, the region number can be expressed as a function of the three parameters as follows:

$$reg = -a + \left(b^2 - b + 1\right) + h \tag{5.12}$$

The three parameters can be determined as follows:

$$\mathrm{a} = \mathbf{floor}\left(\frac{\mathrm{V_m}\cos\left(\theta + \frac{\pi}{6}\right)}{E\cos\left(\frac{\pi}{6}\right)}\right) + 1 = \mathbf{floor}\left(m_a(m-1)\cos\left(\theta + \frac{\pi}{6}\right)\right) + 1 \tag{5.13}$$

$$\mathrm{b} = \mathbf{floor}\left(\frac{\mathrm{V_m}\cos\left(\frac{\pi}{6} - \theta\right)}{E\cos\left(\frac{\pi}{6}\right)}\right) + 1 = \mathbf{floor}\left(m_a(m-1)\cos\left(\frac{\pi}{6} - \theta\right)\right) + 1 \tag{5.14}$$

$$\mathrm{h} = \mathbf{floor}\left(\frac{\mathrm{V_m}\sin(\theta)}{E\cos\left(\frac{\pi}{6}\right)}\right) + 1 = \mathbf{floor}\left(m_a(m-1)\sin(\theta)\right) + 1 \tag{5.15}$$

where $0 \le \theta \le \pi/3$.

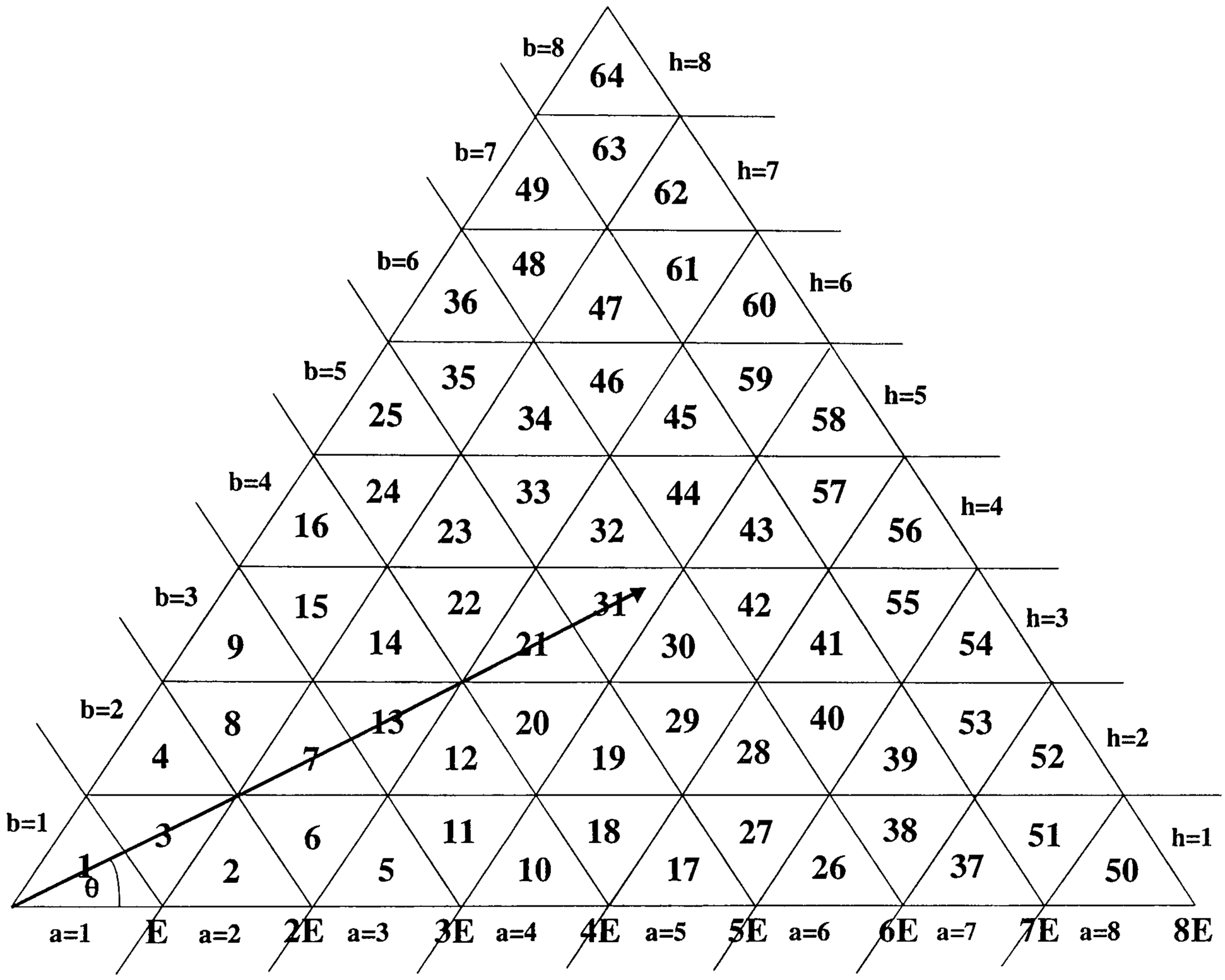


Figure 5.3. The region numbers according to the three parameters a, b, and h

where the modulation index for the multilevel inverter configurations shown in figure (5.4) can be generalized as

$$m_a = \frac{V_m}{(m-1)E\cos\left(\frac{\pi}{6}\right)} \tag{5.16}$$

where E is the cell voltage as shown in figures (5.3) and (5.4), and m is the number of levels per phase voltage.

Figure (5.5) indicates the axis a, b, and h where the value of `a´ is the projection of vector V_m on to the a-axis. Similarly for b and h. For example, for the vector shown in figure (5.3), the three parameters values a = 3, b = 6, and h = 3, substituted into the region equation, gives region 31.

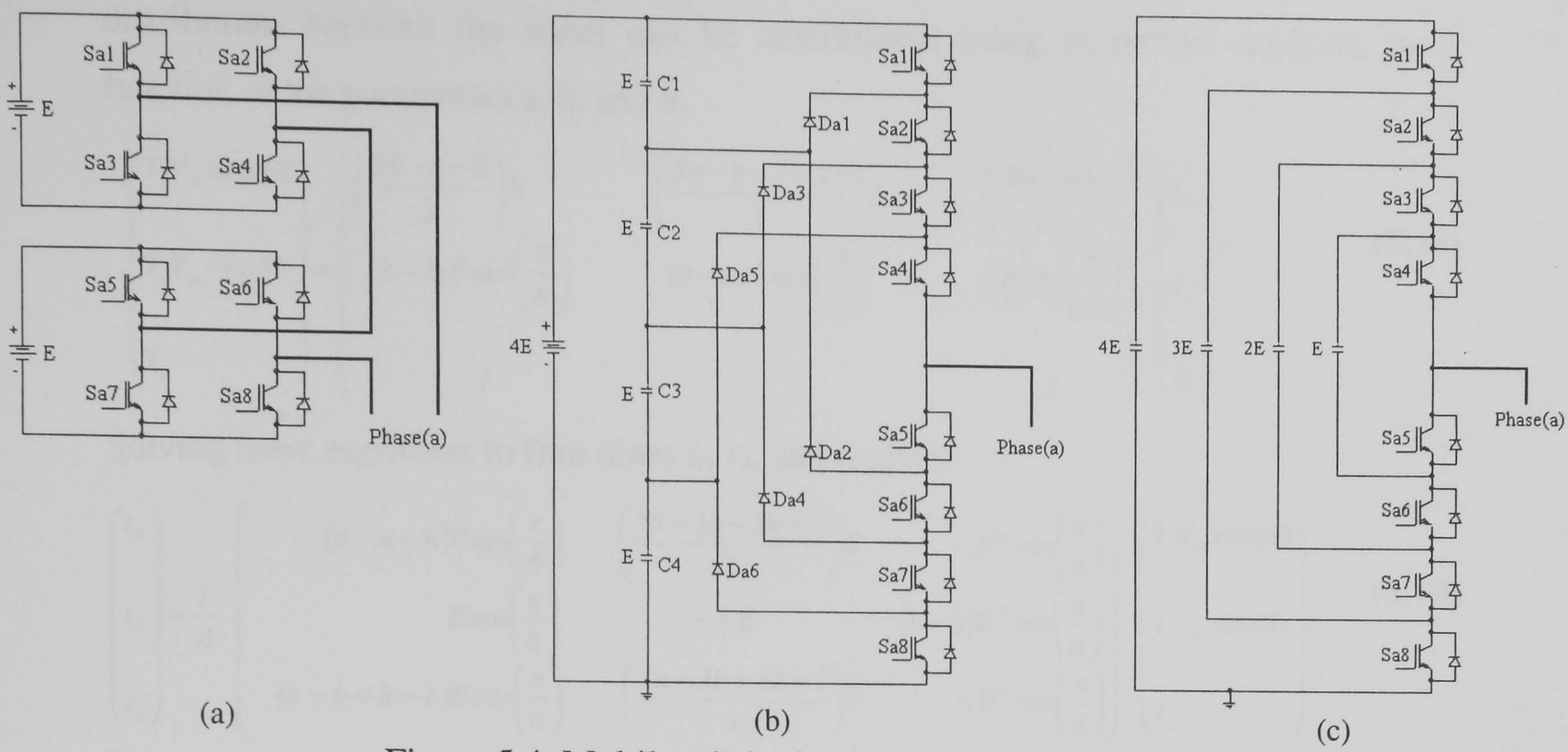


Figure 5.4. Multilevel single-phase configuration of:
(a) Cascaded type, (b) Neutral point clamped type, and (c) Flying capacitor type

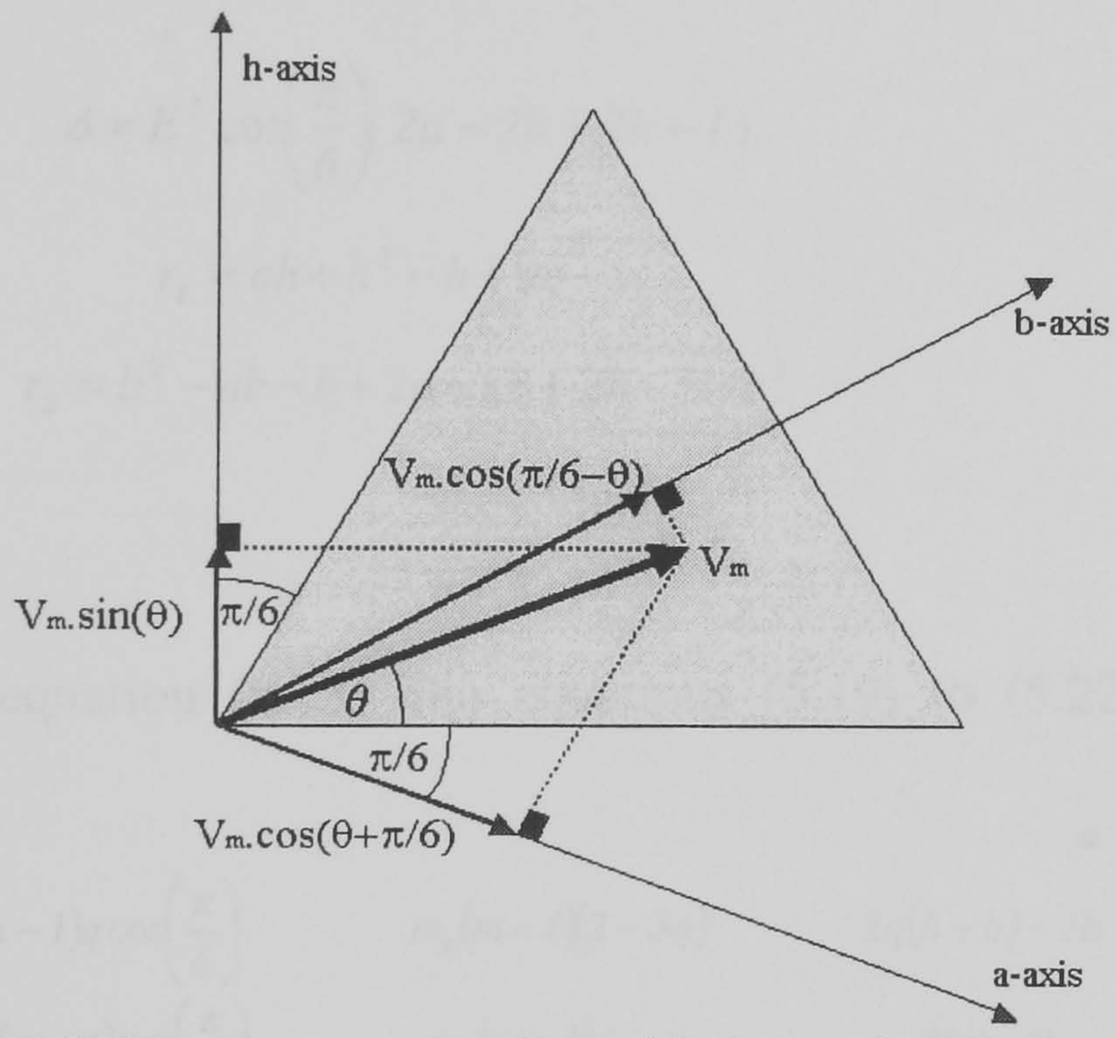


Figure 5.5. The three axes a, b, and h for region determination

5.1.3 Distributing the sampling time

The sampling time is distributed between the three nearest states based on equating the volt-second integral principle. The following equation complies with this principle

$$\overline{V_m}T_s = \overline{V_{0-}}\frac{t_0}{2} + \overline{V_1}t_1 + \overline{V_2}t_2 + \overline{V_{0+}}\frac{t_0}{2} \qquad (5.17)$$

where T_s is the sampling time, and V_{0-}, V_1, V_2, and V_{0+} are the voltage vectors corresponding to the first, second, third, and the alternative state of the first state respectively (on the condition that the minimum number of switchings per sampling time is maintained). The rotation sequence between the three states for the first sector is indicated in figure (5.6). This rotation sequence can be applied for odd sector numbers, while the direction is reversed in even sectors. Generalized equations for the time

distribution between the states can be determined, using numerical analysis, as a function of the parameters a, b, and h.

$$\begin{pmatrix} T_s V_m \cos(\theta) \\ T_s V_m \sin(\theta) \\ T_s \end{pmatrix} = \begin{pmatrix} \left(\frac{2b-1-h}{2}\right)E & \left(\frac{3a-b-2+2h}{2}\right)E & \left(\frac{2b-h}{2}\right)E \\ (h-1)E\cos\left(\frac{\pi}{6}\right) & (b-a)E\cos\left(\frac{\pi}{6}\right) & hE\cos\left(\frac{\pi}{6}\right) \\ 1 & 1 & 1 \end{pmatrix} \begin{pmatrix} t_0 \\ t_1 \\ t_2 \end{pmatrix} \tag{5.18}$$

Solving these equations to find times t_0, t_1, and t_2 gives

$$\begin{pmatrix} t_0 \\ t_1 \\ t_2 \end{pmatrix} = \frac{1}{\Delta} \begin{pmatrix} (b-a-h)E\cos\left(\frac{\pi}{6}\right) & \left(\frac{3b-3a-3h+2}{2}\right)E & r_1E^2\cos\left(\frac{\pi}{6}\right) \\ E\cos\left(\frac{\pi}{6}\right) & -\frac{1}{2}E & (h-b)E^2\cos\left(\frac{\pi}{6}\right) \\ (a-b+h-1)E\cos\left(\frac{\pi}{6}\right) & \left(\frac{3a-3b+3h-1}{2}\right)E & r_2E^2\cos\left(\frac{\pi}{6}\right) \end{pmatrix} \begin{pmatrix} T_s V_m \cos(\theta) \\ T_s V_m \sin(\theta) \\ T_s \end{pmatrix} \tag{5.19}$$

where

$$\Delta = E^2\cos\left(\frac{\pi}{6}\right)(2a-2b+2h-1) \tag{5.20}$$

$$r_1 = ah+h^2-h+ab-b^2 \tag{5.21}$$

$$r_2 = b^2-ab-b+2a-ah+2h-1-h^2 \tag{5.22}$$

Let

$$q = a-b+h \tag{5.23}$$

Then substituting equation (5.23) into equations (5.19) to (5.22), reduces the time equations to:

$$\begin{pmatrix} t_0 \\ t_1 \\ t_2 \end{pmatrix} = \frac{1}{\Delta_1} \begin{pmatrix} -2m_a(m-1)q\cos\left(\frac{\pi}{6}\right) & m_a(m-1)(2-3q) & 2q(h+b)-2h \\ 2m_a(m-1)\cos\left(\frac{\pi}{6}\right) & -m_a(m-1) & 2(q-a) \\ 2m_a(m-1)(q-1)\cos\left(\frac{\pi}{6}\right) & m_a(m-1)(3q-1) & -2q(h+b-2)+2b-2 \end{pmatrix} \begin{pmatrix} T_s\cos(\theta) \\ T_s\sin(\theta) \\ T_s \end{pmatrix} \tag{5.24}$$

where

$$\Delta_1 = 2(2q-1) \tag{5.25}$$

To reduce DSP execution time, t_1 and t_2 are calculated from equation (5.24) while t_0 is calculated from

$$t_0 = T_S - t_1 - t_2 \tag{5.26}$$

5.1.4 Selecting the states

When a vector lies in a particular region, the movement between the nearest three states is chosen in the sequence mentioned in section (5.1.3) and shown in figure (5.6). The states selected must be such that they minimize transitions during the sampling period. For example, in a five-level inverter, when the vector lies in region `7′, the sequence of rotation between the states is shown in figure (5.7). There are 3 alternative sequences, (100 200 210 211), (211 311 321 322), and (322 422 432 433) for the first half of the switching cycle which satisfy the condition for minimum switching. In the second half of the switching cycle the same sequence is used but reversed, as shown in figure (5.8).

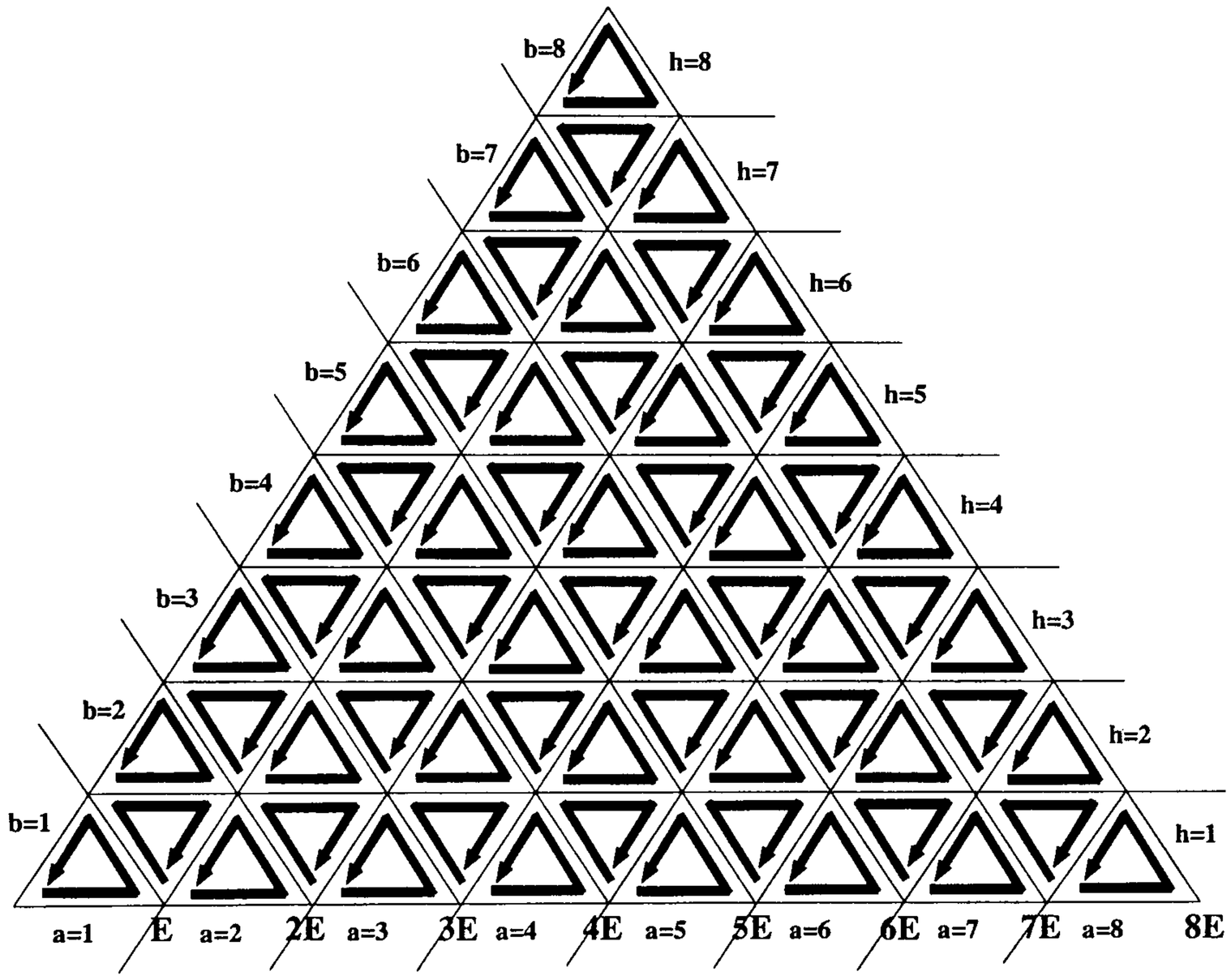


Figure 5.6. The sequence of the rotation between the states

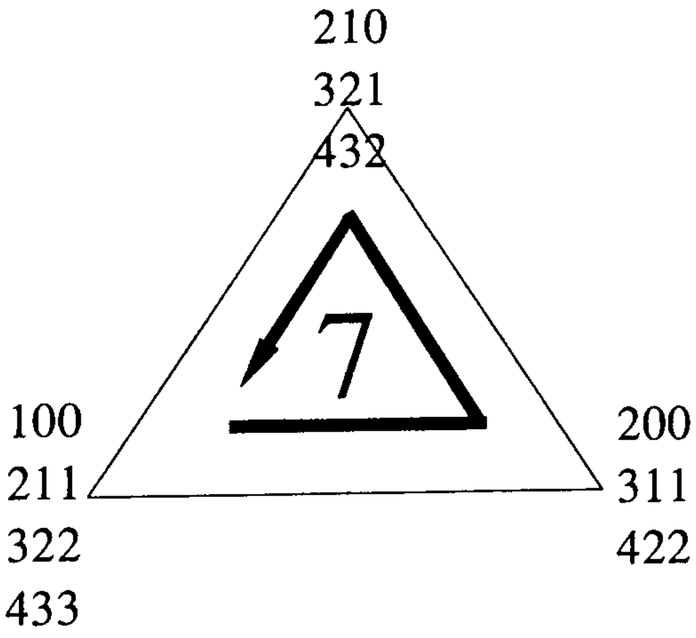


Figure 5.7. The region `7′ for a five-level inverter

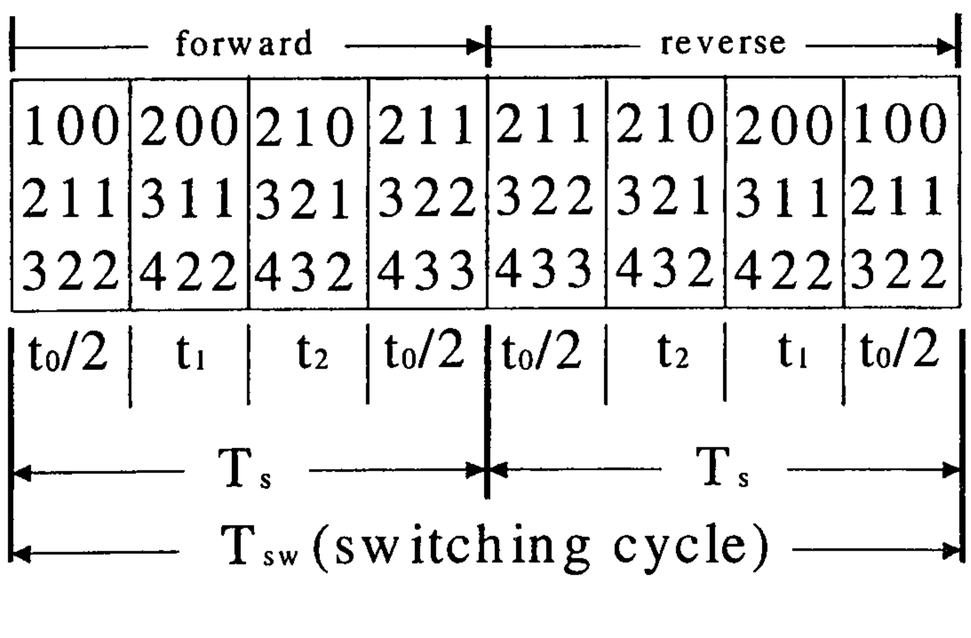


Figure 5.8. The distribution of states during the sampling time

i. Generalized procedure

To generalize the process of finding the rotation sequence between the states in any region where the vector lies, the general states in Table 5.1 are determined from the state matrices.

Table 5.1. The state sequence definition over a sampling time

State	Definition
$X(g_1,g_2,g_3)$	The first state of the sequence movement
$X(g_4,g_5,g_6)$	The second state of the sequence movement
$X(g_7,g_8,g_9)$	The third state of the sequence movement
$X(g_{10},g_{11},g_{12})$	The alternative state for the first state maintaining the minimum number of switchings per sampling time

The parameters g_1, g_4, g_7, and g_{10} determine the order of the state matrix. Parameters g_2, g_5, g_8, and g_{11} determine the sequence of the states. Parameters g_3, g_6, g_9, and g_{12} determine which sequence of the alternative paths is selected. Using numerical analysis, the parameters g_1 to g_{12} can be expressed in terms of s, b, reg, and λ as in Table 5.2, where λ represents the number of possible sequences in a given region (the detailed numerical proof is not within the length restriction of the thesis (see Appendix I)).

Table 5.2. The state parameter definitions

Parameter	Equations
g_1	$g_1 = b$
g_2	$g_2 = c_1 - 6(b\text{-}1)\mathbf{floor}\left(\frac{c_1 - 1}{6(b\text{-}1)}\right)$
g_3	$g_3 = \lambda$
g_4	$g_4 = b + 1 - c_2$
g_5	$g_5 = c_3 - 6b\mathbf{floor}\left(\frac{c_3 - 1}{6b}\right)$
g_6	$g_6 = \lambda$
g_7	$g_7 = b + 1 - \mathbf{even}(s).c_4$
g_8	$g_8 = 1 + c_1 + (s-1).\mathbf{odd}(s) + c_5 - c_6$
g_9	$g_9 = \lambda + c_4.\mathbf{even}(s)$
g_{10}	$g_{10} = g_1$
g_{11}	$g_{11} = g_2$
g_{12}	$g_{12} = \lambda + 1$

Function **even** gives an output of `1′ for an even number otherwise `0′, and **odd** is the complement of function **even.** Note that $1 \le \lambda \le m-b$ can be chosen to make use of the alternative paths. The parameters c_1 to c_7 referred to in Table 5.2 are defined in Table 5.3.

Table 5.3. Detailed expressions for parameters (c_1:c_7) in Table 5.2

Parameter	Equations
c_1	$c_1 = \mathbf{floor}\left(\frac{reg - b(b-2)}{2}\right) + (s-1)(b\text{-}1)$
c_2	$c_2 = \mathbf{odd}(s.b).\mathbf{even}(reg) + \mathbf{odd}(s.reg).\mathbf{even}(b)$
c_3	$c_3 = \mathbf{floor}\left(\frac{reg + 1 - b(b-2)}{2}\right) + b(s-1) + c_7.\mathbf{even}(s) - c_2.(s\text{-}1)$
c_4	$c_4 = \mathbf{odd}(reg).\mathbf{even}(b) + \mathbf{even}(reg).\mathbf{odd}(b)$
c_5	$c_5 = c_7.(s-2).\mathbf{even}(b)$
c_6	$c_6 = 6(b-1).c_4.\mathbf{floor}\left(\frac{reg}{b^2-1}\right).\mathbf{floor}\left(\frac{s}{6}\right)$
c_7	$c_7 = \mathbf{even}(reg).\mathbf{even}(b) + \mathbf{odd}(reg).\mathbf{odd}(b)$

An important feature of these equations is that they involve unsigned short integer numbers which reduces DSP computational burden. Therefore localizing the vector by determining the sector number s and parameters a, b, and h, (therefore the region number 'reg') automatically gives the state sequence, by direct substitution in Tables 5.2 and 5.3, whatever the number of levels. Choosing λ makes use of the alternative path sequences and will be considered later in a three-level SVM case study.

5.2 Over modulation and pulse dropping

In multilevel space vector modulation, the outermost hexagon is the boundary between linear modulation (inside) and over modulation (outside). For an over modulated voltage vector, the solution of time equations is negative for at least one of the three times (t_0, t_1, and t_2 in equation (5.24)). To overcome this problem, the outermost hexagon is considered as the locus for the over modulated voltage vector. However, if the voltage vector lies on this locus, one of the nearest three states is dropped and this leads to increased current ripple. A defined inward shift of this locus avoids dropping one of the nearest three states (pulse dropping). Also this shift prevents incorrect or invalid determination of the region number. Pulse dropping occurs when the modulation index lies on any of the internal region boundaries as well as the outermost hexagon

boundary. This is avoided by imposing a minimum time constraint on t_0, t_1, and t_2 which will impose some non-linearity into the inverter transfer function. The following section explains the proposed method for dealing with over modulation and pulse deletion.

5.2.1 Proposed over modulation method

For over modulation, the voltage space vector exceeds the boundary of the outermost hexagon. To deal with over modulation in multilevel SVM, if the voltage space vector V_m (line OA in figure(5.9a)) exceeds the outermost hexagon, the voltage space vector is reduced to V_m' (line OA$'$ in figure (5.9a)). The point A$'$ is the intersection of the voltage space vector OA and the line BC (OA and BC can never be parallel). The line BC represents the locus for the over modulated voltage space vector in this sector. Generally, the outermost hexagon will represent the locus for the over modulated voltage space vector in all the sectors. Although figure (5.9a) represents one sector for 3-level space vector modulation, generally for *m*-level SVM, point B equals *(m-1)E* and point D equals *(m-1)E/2*. For *m*-level SVM, the equation of line BC is:

$$y = \cos\left(\frac{\pi}{6}\right)\left(2E(m-1)-2x\right) \tag{5.27}$$

The equation of line OB is:

$$y = x\tan(\theta) \tag{5.28}$$

Solving equations (5.27) and (5.28) gives:

$$x = \frac{2E(m-1)\cos\left(\frac{\pi}{6}\right)}{\tan(\theta)+2\cos\left(\frac{\pi}{6}\right)} \tag{5.29}$$

The limited voltage space vector V_m' can be expressed as a function of x

$$V_m' = \frac{x}{\cos(\theta)} \tag{5.30}$$

From equations (5.29) and (5.30), V_m' becomes

$$V_m' = \frac{E(m-1)\cos\left(\frac{\pi}{6}\right)}{\sin\left(\theta+\frac{\pi}{3}\right)} \tag{5.31}$$

So, if the voltage space vector exceeds V_m' , the voltage space vector is over modulated and is reduced to V_m'.

5.2.2 Pulse dropping avoidance on outer hexagon

To avoid losing one of the nearest three states (pulse dropping), BC (figure (5.9a)) is shifted inwards by δ percent as shown in figure (5.9b), where δ is related to the minimum t_0 (t_{0min}).

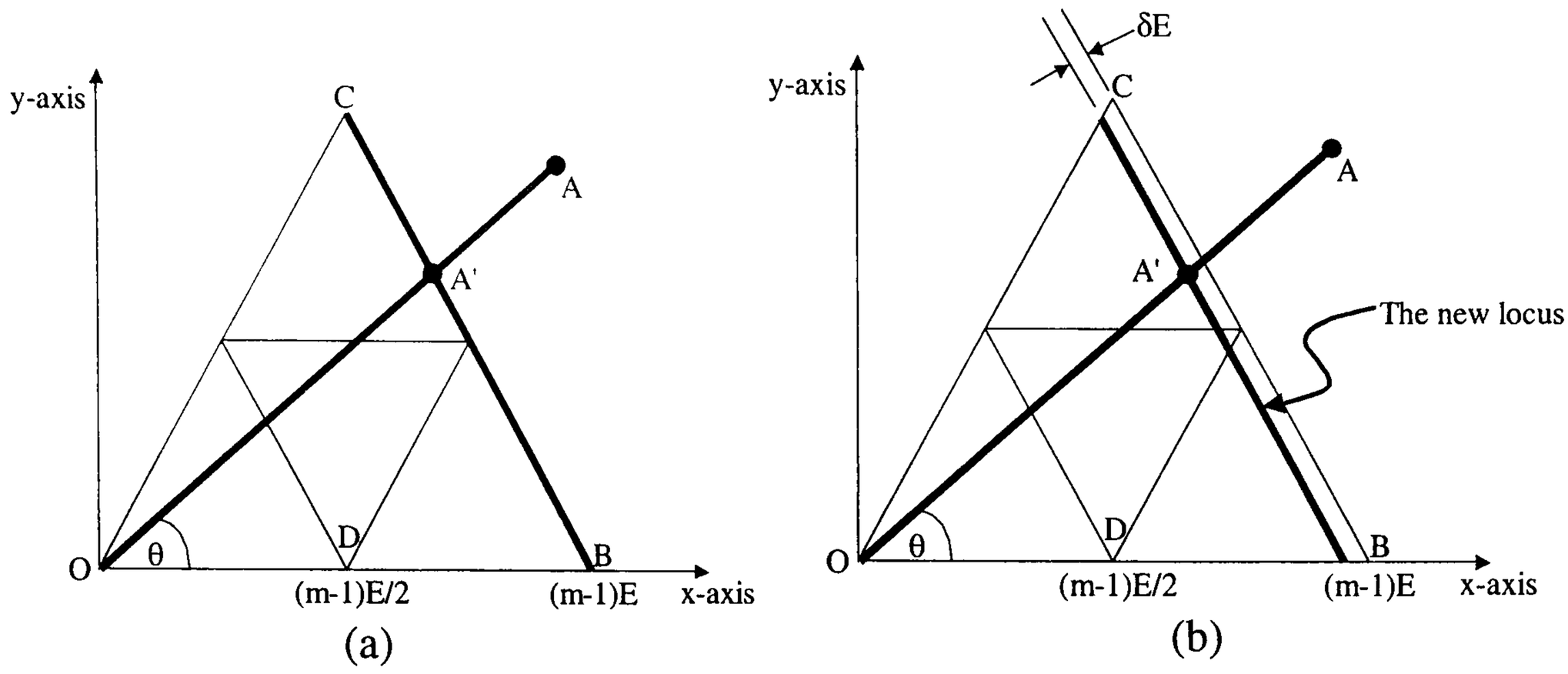


Figure 5.9. Over modulation: (a) The locus of the over modulated voltage space vector and (b) The new locus of the over modulated voltage space vector

The shift of V_m' by δE towards the centre, to V_m'', is incorporated into equation (5.31) as in equation (5.32):

$$V_m'' = \frac{E(m-1)\cos\left(\frac{\pi}{6}\right)}{\sin\left(\theta+\frac{\pi}{3}\right)} - \delta.E \tag{5.32}$$

where

$$\delta = \delta_1.(m-1)\cos\left(\frac{\pi}{6}\right) \tag{5.33}$$

Substituting for the modulation index, m_a from equation (5.12) into equation (5.32) gives

$$m_a = \frac{1}{\sin\left(\theta+\frac{\pi}{3}\right)} - \delta_1 \tag{5.34}$$

From equation (5.24), t_0 is defined as

$$t_0 = \frac{T_s}{2(2q-1)}\left[\begin{array}{r} -2m_a(m-1)q\cos\left(\frac{\pi}{6}\right)\cos(\theta) \\ +m_a(m-1)(2-3q)\sin(\theta) \\ +\left[2q(h+b)-2h\right] \end{array}\right] \tag{5.35}$$

If the voltage vector is on the outer hexagon, the vector is moved to lie inside the shaded area shown in figure (5.10). If the voltage vector lies in a shaded area, then (b = m - *1)* and (a + h = m). If figure (5.10) represents one sector for the 9-level inverter (m = 9) and the vectors in the shaded area, b = 8 and a + h = *9*. From equation (5.23), q = 1.

Therefore, equation (5.35) can be reduced to

$$\frac{t_0}{T_s} = (m-1)\left[1 - m_a \sin\left(\theta + \frac{\pi}{3}\right)\right] \tag{5.36}$$

Substituting m_a from equation (5.34) into (5.36) yields

$$\frac{t_0}{T_s} = (m-1).\delta_1.\sin\left(\theta + \frac{\pi}{3}\right) \tag{5.37}$$

Thus δ_1 can be expressed as

$$\delta_1 = \frac{1}{(m-1).\sin\left(\theta + \frac{\pi}{3}\right)}.\left(\frac{t_0}{T_s}\right) \tag{5.38}$$

In equation (5.38), δ_1 is maximized with respect to θ to minimize t_0 in equation (5.36). Note that the minimum time t_0 ($\breve{t}_0$) must be greater than the summation of both the minimum on-time and the underlap time of the switch, in order to avoid losing one of the three states in over modulation. For $\hat{\delta}_1$, θ = 0 or π/3 $\quad (0 \le \theta \le \pi/3)$.

$$\hat{\delta}_1 = \frac{1}{(m-1).\sin\left(\frac{\pi}{3}\right)}.\left(\frac{t_0}{T_s}\right) \tag{5.40}$$

Substituting equation (5.40) into equation (5.32) yields

$$V_m^{//} = \frac{E(m-1)\cos\left(\frac{\pi}{6}\right)}{\sin\left(\theta + \frac{\pi}{3}\right)} - \frac{t_0}{T_s}E \tag{5.41}$$

so that δ is defined as

$$\delta = \frac{t_0}{T_s} \tag{5.42}$$

If the switch minimum on-time (the typical values for turn-on delay time, rise time, turn-off delay time, and fall time) is $t_{on} = 710\ ns$, the underlap time for a switch is $t_d = 640\ ns$, and the switching cycle (T_{sw}) is $327.7\ \mu s$ (the sampling time is 327.7 / 2 μs), then $\breve{t}_0 = 2(t_{on} + t_d) = 2(710 + 640) = 2700\ ns$ (because t_0 is divided equally so that $t_0/2 = 1.35\ \mu s$), such that from equation (5.42), $\delta = 0.822\ \%$.

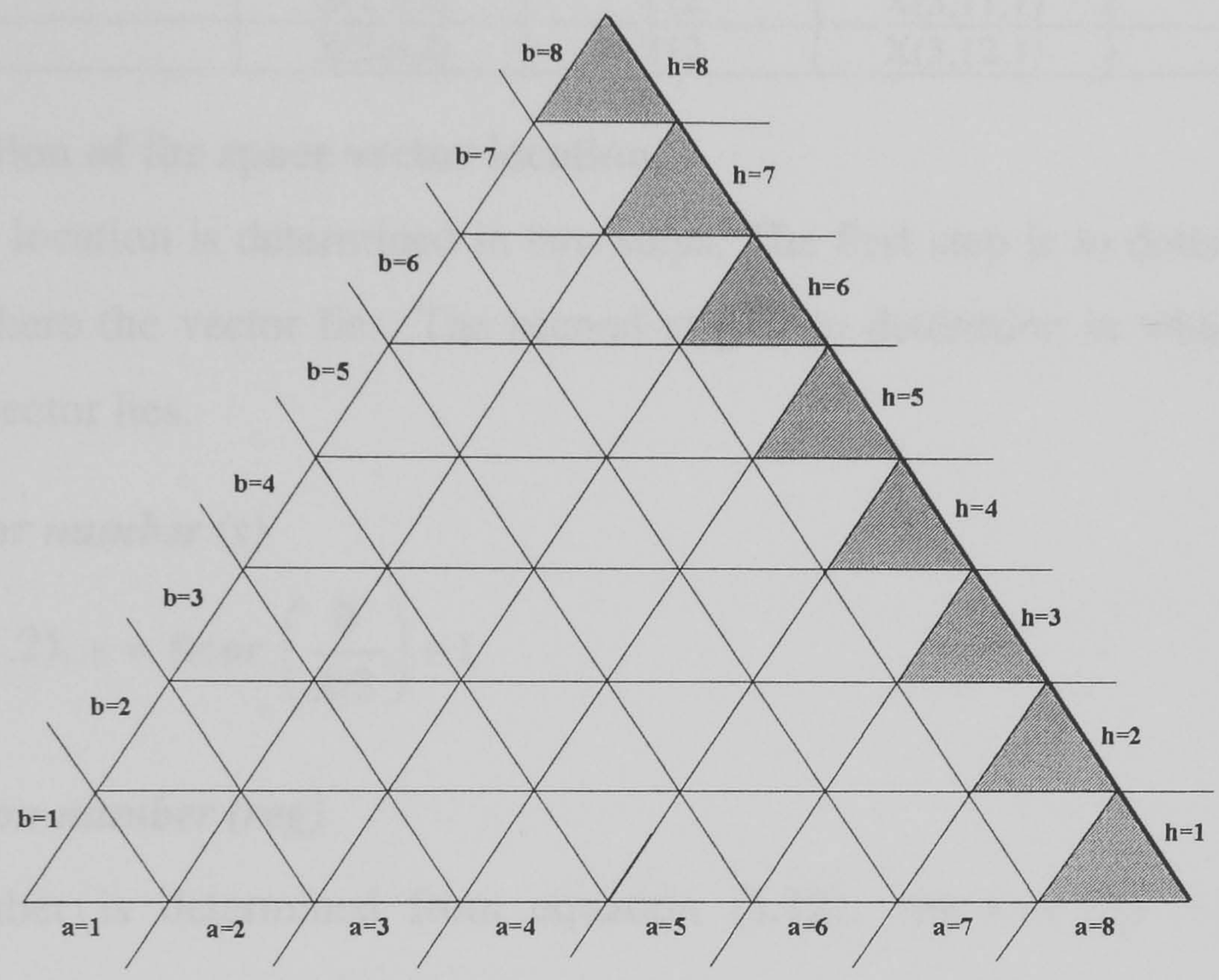


Figure 5.10. The shaded area represents the location of the over modulated voltage vector

5.2.3 Pulse dropping avoidance on inner triangle boundaries

To avoid pulse dropping when the vector lies on the boundary of any triangle, a minimum time for $t_0/2$, t_1, and t_2 is assumed. According to section 5.2, taking into consideration the minimum on-time and the underlap time, a 1.35 μs minimum time is assumed.

5.3 Three-level SVM example

The following sub-sections outline each step of the proposed generalized algorithm when applied to three-level SVM.

5.3.1 The three-level inverter space vector states

The 27 states are defined in section (5.1.1) equations (5.5) to (5.7) and are shown in Table 5.4.

Table 5.4. The three-level space vector states

Zero state		First hexagon		Second hexagon	
X(1,1,1)	000	X(2,1,1)	100	X(3,1,1)	200
X(1,1,2)	111	X(2,2,1)	110	X(3,2,1)	210
X(1,1,3)	222	X(2,3,1)	010	X(3,3,1)	220
		X(2,4,1)	011	X(3,4,1)	120
		X(2,5,1)	001	X(3,5,1)	020
		X(2,6,1)	101	X(3,6,1)	021
		X(2,1,2)	211	X(3,7,1)	022
		X(2,2,2)	221	X(3,8,1)	012
		X(2,3,2)	121	X(3,9,1)	002
		X(2,4,2)	122	X(3,10,1)	102
		X(2,5,2)	112	X(3,11,1)	202
		X(2,6,2)	212	X(3,12,1)	201

5.3.2 Determination of the space vector location

The space vector location is determined in two steps. The first step is to determine the sector number where the vector lies. The second step is to determine in which region (sub-sector) the vector lies.

Step 1. The sector number (s)

As in section (5.1.2), $s = \mathbf{floor}\left(\frac{\theta}{\pi/3}\right)+1$

Step 2. The region number (reg)

The region number is determined from equation (5.12), $reg = -a+\left(b^2-b+1\right)+h$

where a, b, and h are determined as follows:

$$a = \mathbf{floor}\left(2m_a \cos\left(\theta+\frac{\pi}{6}\right)\right)+1 \tag{5.43}$$

$$b = \mathbf{floor}\left(2m_a \cos\left(\frac{\pi}{6}-\theta\right)\right)+1 \tag{5.44}$$

$$h = \mathbf{floor}\left(2m_a \sin(\theta)\right)+1 \tag{5.45}$$

where m_a is defined from equation (5.16) for three-level SVM, m=3, as

$$m_a = \frac{V_m}{2E\cos\left(\frac{\pi}{6}\right)} \tag{5.43}$$

5.3.3 Distribution of the sampling time

For three-level SVM, the sampling time is distributed according equation (5.24):

$$\begin{pmatrix} t_0 \\ t_1 \\ t_2 \end{pmatrix} = \frac{1}{\Delta_1} \begin{pmatrix} -4m_a q\cos\left(\frac{\pi}{6}\right) & 2m_a(2-3q) & 2q(h+b)-2h \\ 4m_a\cos\left(\frac{\pi}{6}\right) & -2m_a & 2(q-a) \\ 4m_a(q-1)\cos\left(\frac{\pi}{6}\right) & 2m_a(3q-1) & -2q(h+b-2)+2b-2 \end{pmatrix} \begin{pmatrix} T_s\cos(\theta) \\ T_s\sin(\theta) \\ T_s \end{pmatrix} \quad (5.47)$$

where

$$\Delta_1 = 2(2q-1) \quad (5.48)$$

and

$$q = a - b + h \quad (5.49)$$

To reduce DSP execution time, t_1 and t_2 are calculated from (5.47) while t_0 is calculated from

$$t_0 = T_S - t_1 - t_2 \quad (5.50)$$

For the three-level inverter and in the four different regions, the time equations are defined from equation (5.47), as shown in Table 5.5.

Table 5.5 The time equations for the four regions

a	*b*	*h*	*reg*	*Time equations*
1	1	1	**1**	$t_1 = 2m_aT_s.\sin\left(\frac{\pi}{3}-\theta\right)$ $t_2 = 2m_aT_s.\sin(\theta)$
2	2	1	**2**	$t_1 = T_s\left(2m_a.\sin\left(\frac{\pi}{3}-\theta\right)-1\right)$ $t_2 = 2m_aT_s.\sin(\theta)$
1	2	1	**3**	$t_1 = T_s\left(1-2m_a.\sin\left(\frac{\pi}{3}-\theta\right)\right)$ $t_2 = T_s\left(2m_a.\sin\left(\frac{\pi}{3}+\theta\right)-1\right)$
1	2	2	**4**	$t_1 = 2m_aT_s.\sin\left(\frac{\pi}{3}-\theta\right)$ $t_2 = T_s(2m_a.\sin(\theta)-1)$

5.3.4 Choosing the states

The chosen states must minimize transitions during the sampling period. The state sequences in the four regions are shown in figure (5.11). The state transition for three-level SVM is based on the following steps.

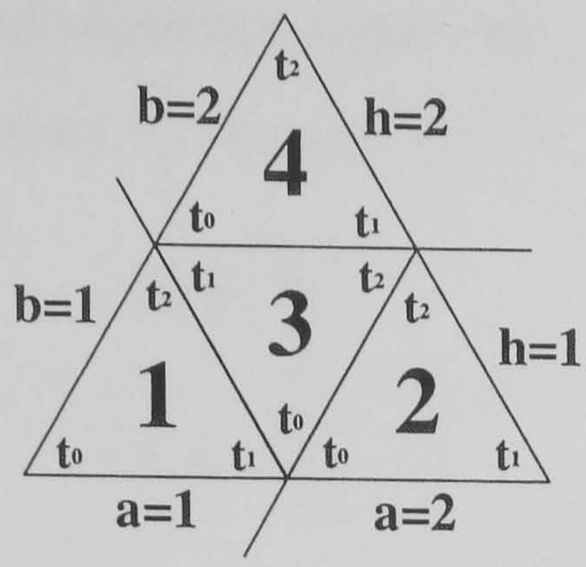


Figure 5.11. The region numbers according to the three parameters a, b, and h

i. Generalized procedure

For the three-level inverter, using Tables 5.2 and 5.3, the state sequences in all regions in the three-level space, are shown in Table 5.6.

Table 5.6. The sequence of the states in three-level space
(grey rows indicate the alternative path sequences)

s	b	reg	λ	t_0 state $X(g_1, g_2, g_3)$	t_1 state $X(g_4, g_5, g_6)$	t_2 state $X(g_7, g_8, g_9)$	t_7 state $X(g_{10}, g_{11}, g_{12})$
1	1	1	1	000	100	110	111
			2	111	211	221	222
	2	2	1	100	200	210	211
		3		100	110	210	211
		4		110	210	220	221
2	1	1	1	000	010	110	111
		1	2	111	121	221	222
	2	2	1	110	120	220	221
		3		110	120	121	221
		4		010	020	120	121
3	1	1	1	000	010	011	111
			2	111	121	122	222
	2	2	1	010	020	021	121
		3		010	011	012	121
		4		011	021	022	122
4	1	1	1	000	001	011	111
			2	111	112	122	222
	2	2	1	011	012	022	122
		3		011	012	112	122
		4		001	002	102	112
5	1	1	1	000	001	101	111
			2	111	112	121	222
	2	2	1	001	002	102	112
		3		001	101	102	112
		4		101	102	202	212
6	1	1	1	000	100	101	111
			2	111	211	212	222
	2	2	1	101	201	202	212
		3		101	201	211	212
		4		100	200	201	211

5.3.5 Over modulation and minimum pulse width

For over modulation, the vector V_m' is expressed as

$$V_m'' = \frac{2E\cos\left(\frac{\pi}{6}\right)}{\sin\left(\theta+\frac{\pi}{3}\right)} - \frac{t_0}{T_s}E \tag{5.51}$$

If the voltage space vector exceeds V_m'', the voltage space vector is either over modulated or may result in pulse dropping, so it is reduced to V_m'', (OA'') as shown in figure (5.12).

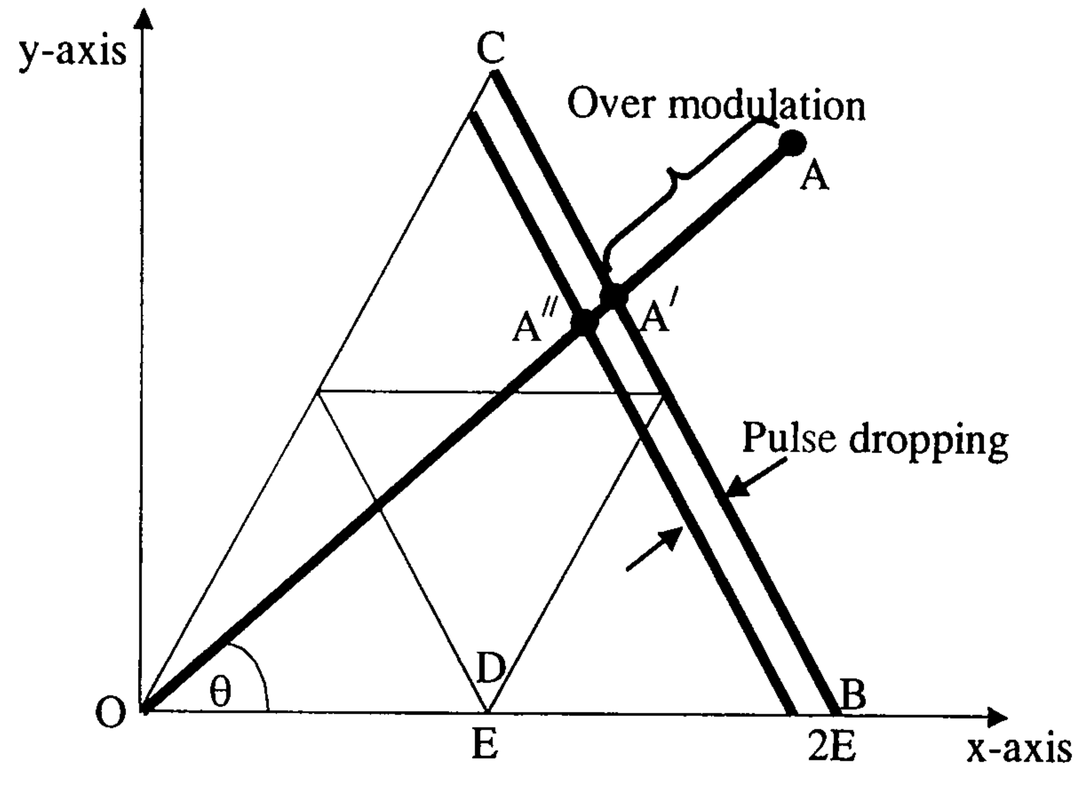


Figure 5.12. The locus of the over modulated voltage space vector

5.4 Simulation results

5.4.1 Linear modulation

Using Matlab/Simulink, the proposed generalized algorithm for multilevel SVM can be validated (see Appendix A). Parts a to f of figure (5.13) present the line voltage for two, three, five, seven, nine, and eleven level inverters. The modulation index is 0.9 and the sampling frequency is 3 kHz, with an output frequency of 50 Hz.

Figure (5.14a) shows the line voltage total harmonic distortion (THD) for three, five, seven, and nine level SVM. As expected, as the number of levels increases, THD decreases for a given modulation index. Figure (5.14b) presents the corresponding line voltage distortion factors (DF). Figure (5.14c) presents the fundamental component of the line voltage. The results are as would be expected.

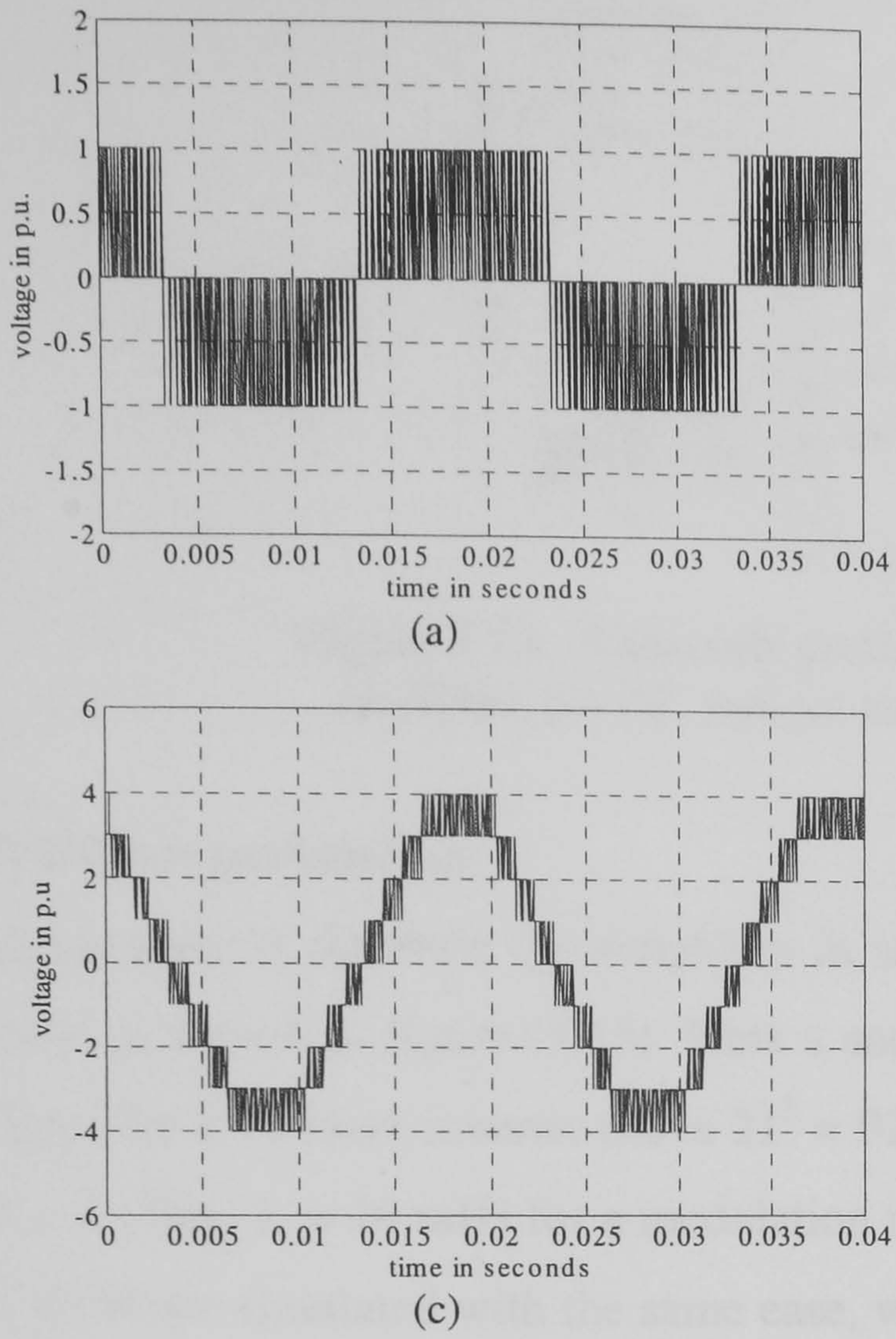
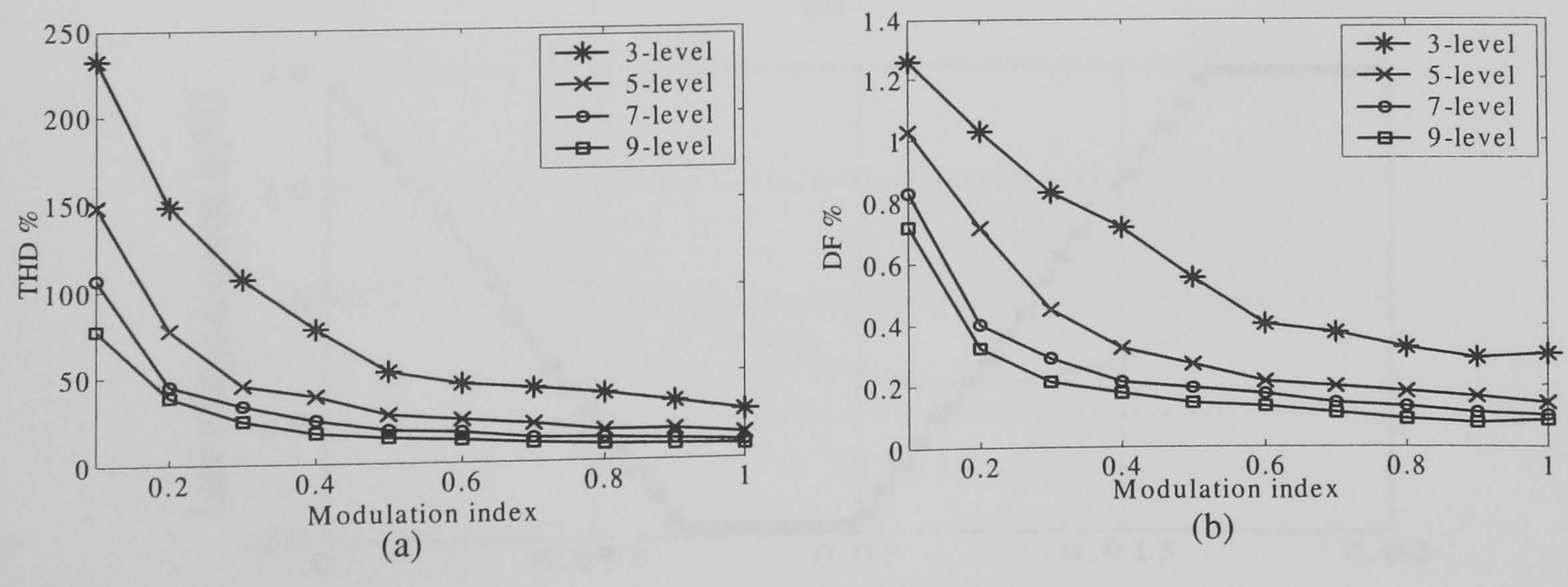
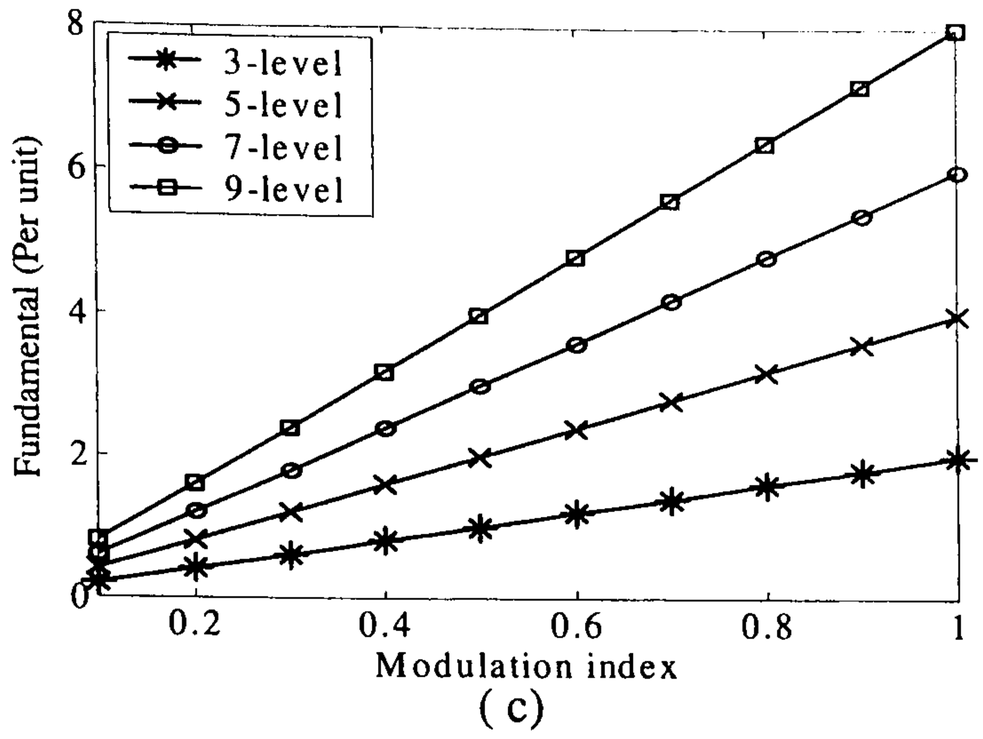


Figure 5.13. Line voltage for:
(a) 2-level, (b) 3-level, (c) 5-level, (d) 7-level, (e) 9-level, and (f) 11-level inverters



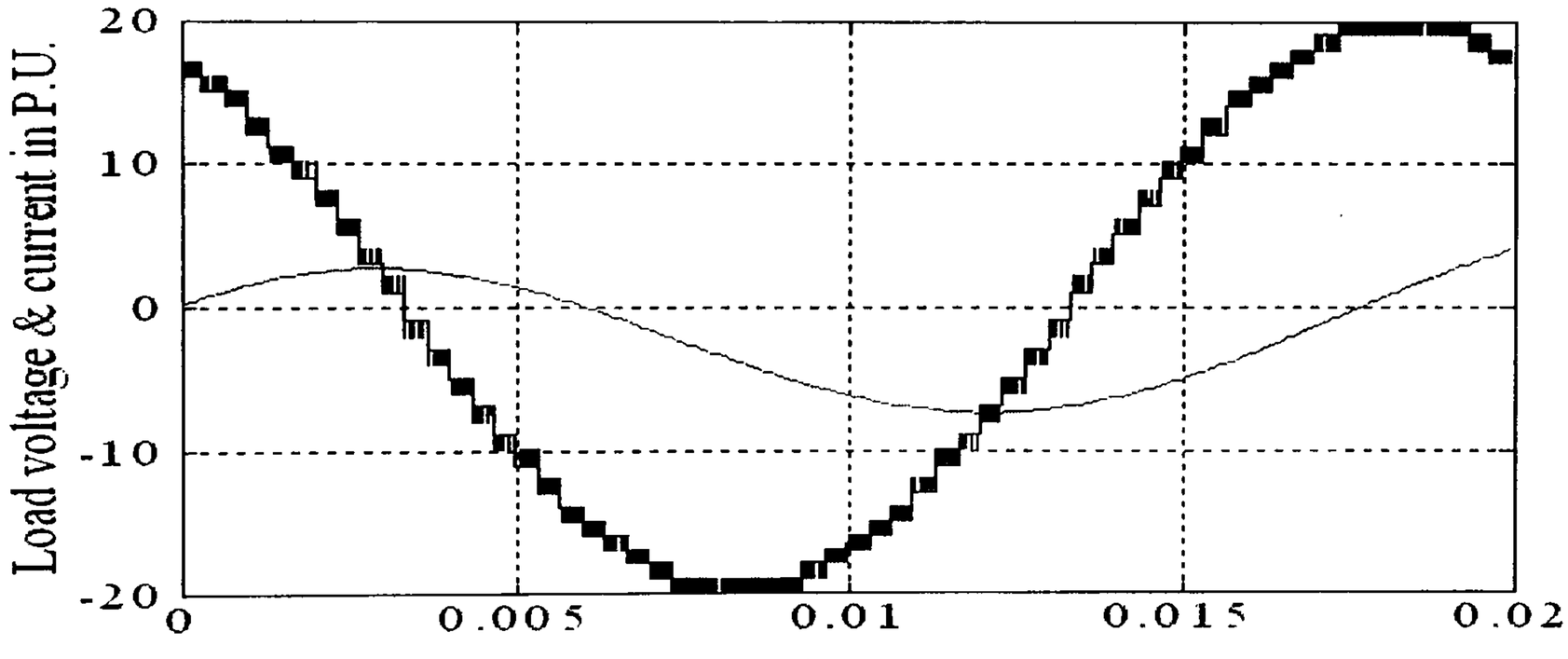


(c)

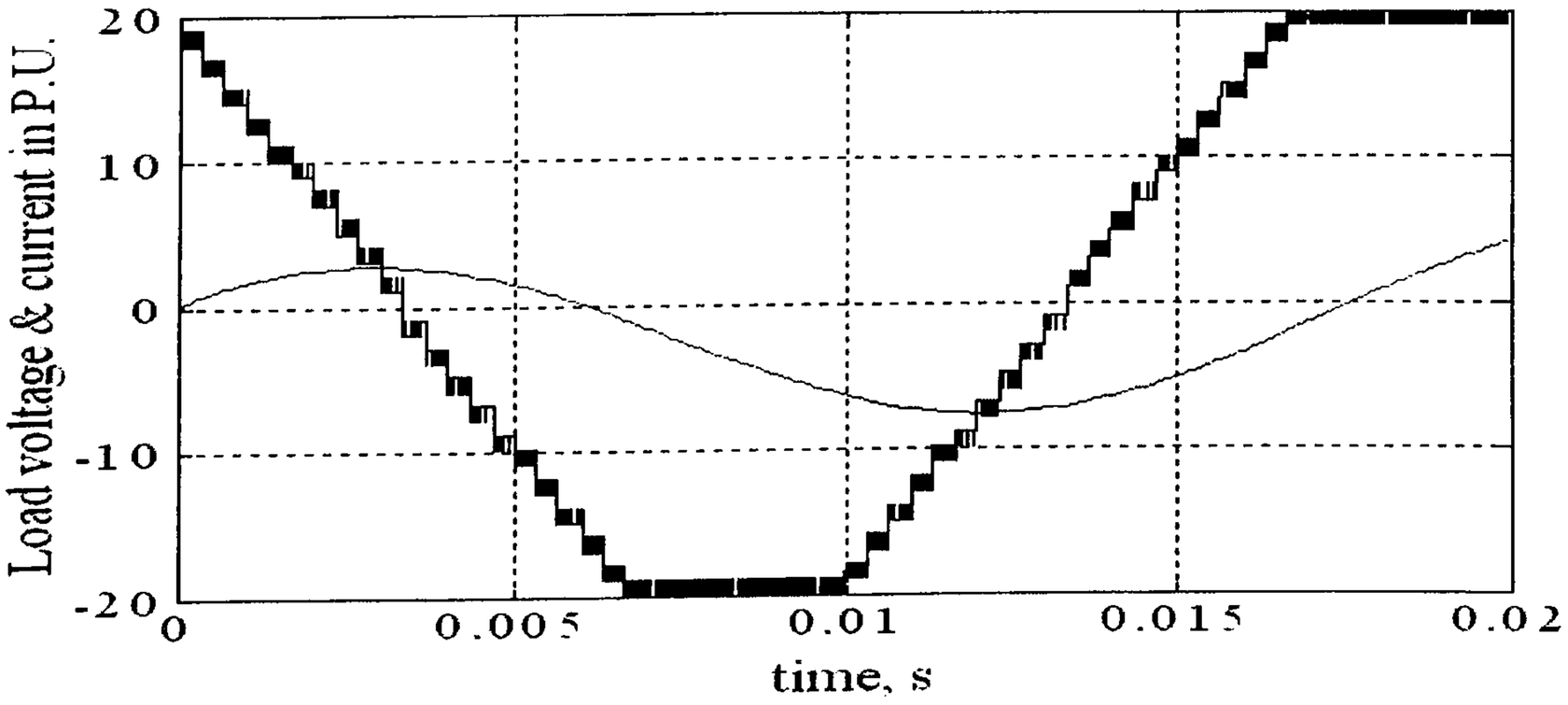
Figure 5.14. Harmonic performance of multilevel SVM:
(a) THD, (b) DF, and (c) the fundamental component

5.4.2 Over modulation

An example to illustrate the simplicity in simulating the algorithm for any number of levels, is shown in figure (5.15). Parts a and b of this figure represent the line voltage output for a 21-level inverter (have $21^3 = 9261$ states) feeding a three-phase static load (R = 1 Ohm, L = 10 mH) for a modulation index of 1 and 2 respectively. Higher levels of SVM are simulated with the same ease, with a 21-level example presented to clearly indicate the number of levels (41 levels / line voltage).



(a)



(b)

Figure 5.15. 21-level SVM for modulation index of (a) 1 and (b) 2

5.4.3 Alternative paths

To demonstrate the use of the alternative paths, a state space model of the three-level neutral point clamped inverter (NPC) is simulated and three-level SVM is applied for a modulation index of 0.3 (to assure that the reference vector is inside the inner hexagon). The capacitor voltage is controlled using the parameter λ (path redundancy) starting at t = *0.1 s*. Parts a to c of figure (5.16) indicate the capacitor voltages, the load current, and the parameter λ, respectively. When λ = 1, the lower capacitor will be loaded (discharge) and all the DC voltage will be impressed on the upper capacitor. Also, the load current converges to zero since the output voltage converges to zero. At $t = 0.1\ s$, λ is controlled and the capacitor voltages reach balance after half a cycle.

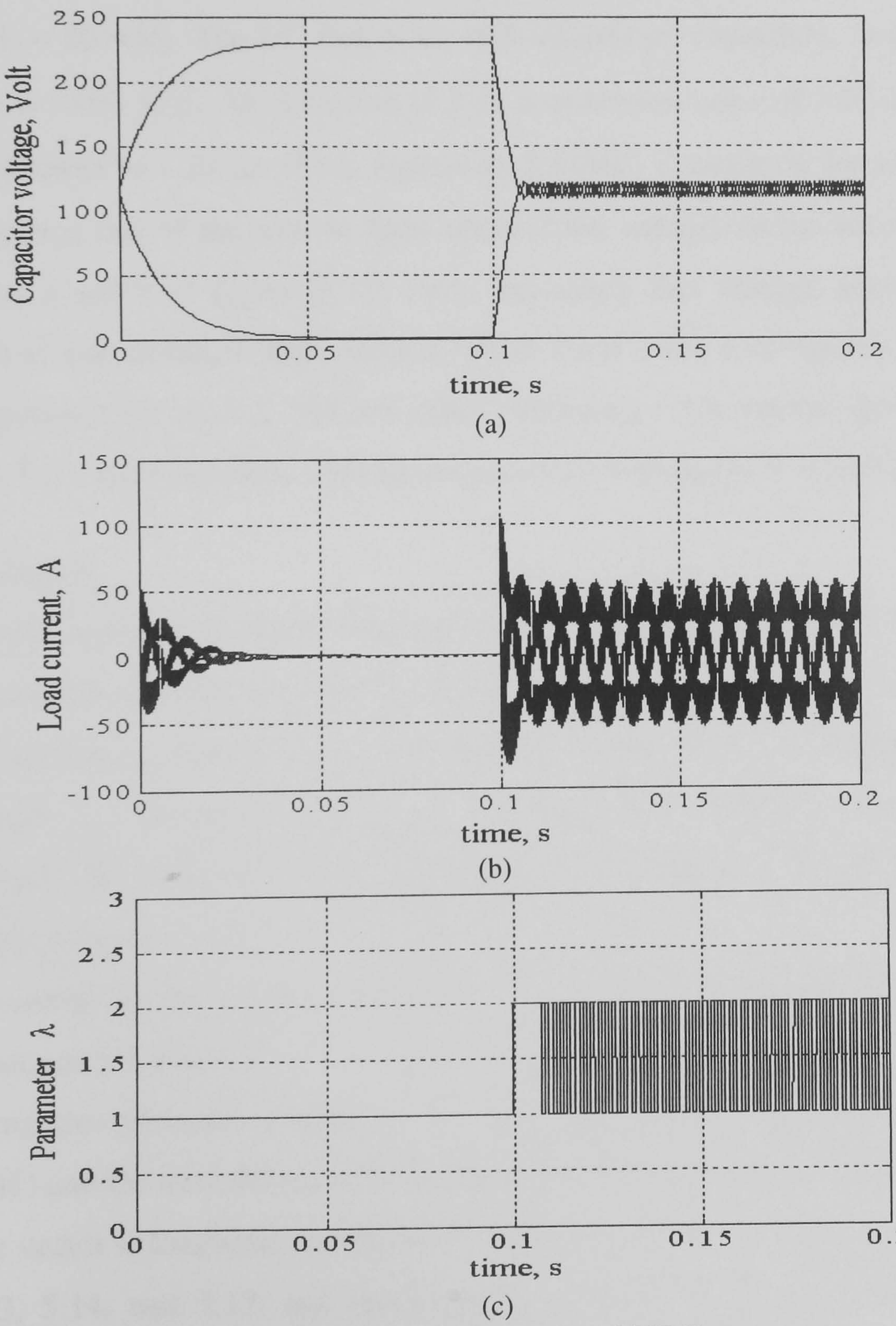


Figure 5.16. Three-level NPC
(a) capacitor voltages, (b) load currents, and (c) parameter λ

5.5 Practical results

The proposed algorithm is implemented using DSP software (Code Composer (see Appendix B)) and the DSP output to the AED-106 is the timing distribution of the states (t_0, t_1, t_2) and the corresponding states. The code execution time of 44 μs allows a switching frequency of up to 22 kHz, independent of the number of levels. PWM generation and the underlap time for the switches (640 ns) are implemented in the Xilinx chip. The **d**igital **i**ncrement **r**eference **p**eriod (DIRP) is 640 ns and this means the underlap time is 1 DIRP. The TTL PWM outputs from the AED-106 digital I/O pins, feed the gate drives of the inverter switches.

The inverter is a 3-phase 5-level cascaded type (H-bridge) with a 3-phase R-L load (R = 17 Ohm, L = 20 mH). The DC link is six 450 V/2200 μF capacitors, and the switching frequency is 3.051 kHz. As in section (5.3.3), a minimum value of 1.28 μs (1.35 μs can be approximated to 1.28 μs which represents 2 DIRP) is assumed for $t_0/2$, t_1, and t_2 to avoid dropping one of the nearest three states if the voltage vector lies on any triangle edge. Parts a and b of figure (5.17) show the output line voltage, phase current, and spectrums at a modulation index (m_a) of 0.866. Parts c and d of figure (5.17) show the same outputs but for $m_a = 2$. The low order harmonics in the current spectrum in part d of figure (5.17) are minimized with the proposed over modulation technique.

5.6 Conclusion

A systematic numerical analysis-based generalized algorithm, with fast DSP execution time, for multilevel SVM has been presented in this chapter. Practical execution time is fixed for a given number of levels, thus ensuring that the system switching frequency is not limited by computation time. Over modulation without pulse dropping is incorporated. The alternative path sequences can be utilized. The algorithm sequence can be summarized as follows:

i. According to the number of inverter levels, the state matrix is generated from equations 5.1 and 5.2;
ii. Using the reference voltage vector, over modulation is checked using equation (5.41) and the modulation index is calculated from equation (5.16);
iii. The vector is localized, by determining the parameters a, b, and h using equations 5.13, 5.14, and 5.15, and equations 5.11 and 5.12 give the sector and region numbers, respectively;
iv. The sampling time is distributed for the nearest three vectors using equation (5.24); and

v. The sequence of the states is determined from look-up tables 5.2 and 5.3. Alternative path sequences can be utilized by using parameter λ.

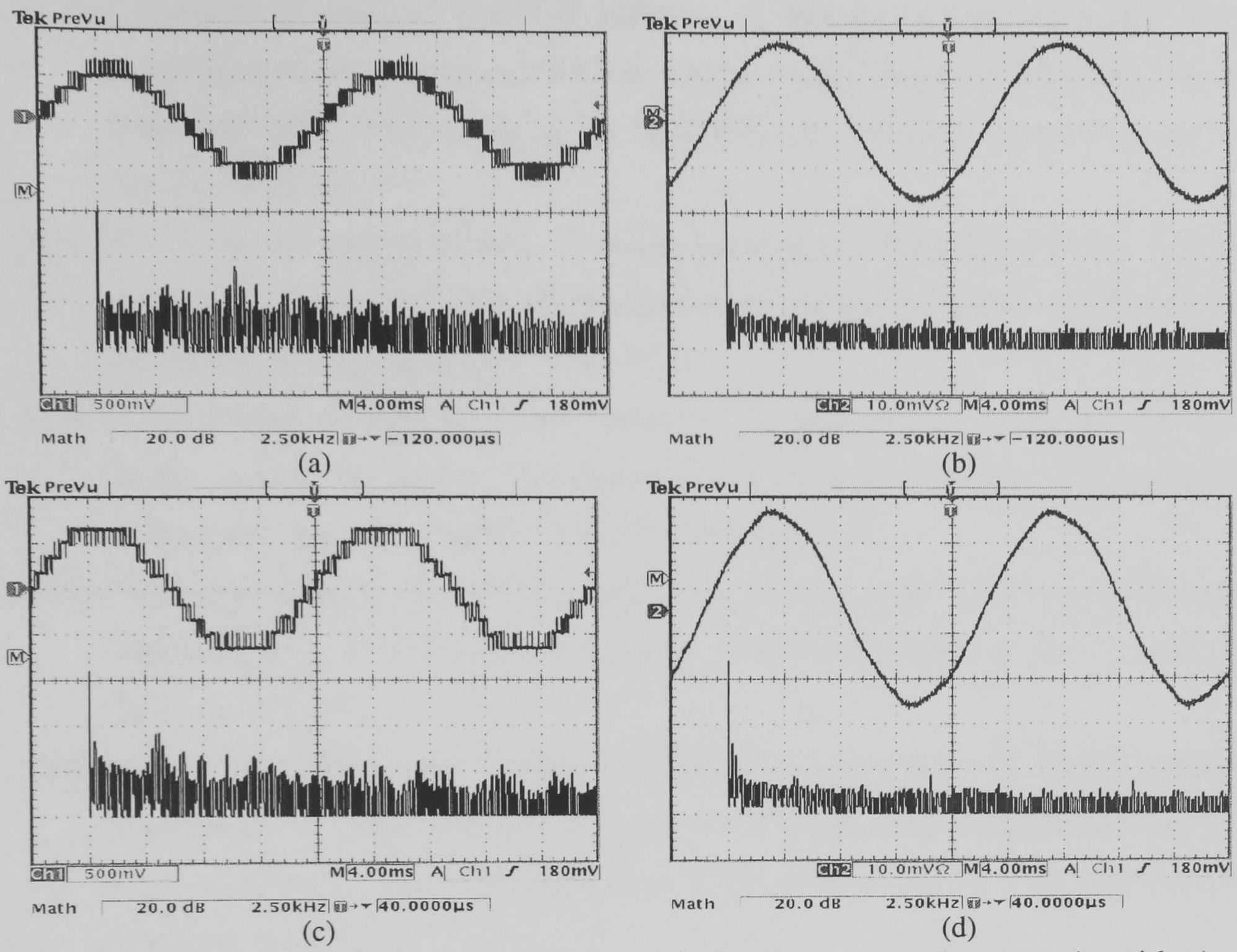


Figure 5.16. The output line voltage and phase current and spectra (semi log):
(a) and (b) for modulation index (m_a) = 0.866
(c) and (d) for modulation index (m_a) = 2
(power factor 0.938 lag) (100V/div & 2A/div)

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Chapter 6

New Multilevel SVM techniques

In this chapter four new multilevel SVM techniques, (phase shifted SVM (PS-SVM), hybrid SVM (H-SVM), mapped phase shifted SVM (MPS-SVM), and mapped hybrid SVM (MH-SVM)), are investigated. The proposed techniques are validated by simulation using Matlab/Simulink and confirmed practically.

6.1 Two-level SVM

The two-level SVM technique involves vectorially equating the volt-second integral of a desired reference voltage vector to the nearest three states in space which are realizable by the inverter.

For the two-level inverter shown in figure (6.1), a transformation from three to two phases is performed to obtain the reference vector magnitude:

$$\begin{pmatrix} v_\alpha^* \\ \\ v_\beta^* \end{pmatrix} = \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} v_a^* \\ v_b^* \\ v_c^* \end{pmatrix} \tag{6.1}$$

The reference voltage vector magnitude is expressed as:

$$V_{ref}^* = \sqrt{\left(v_\alpha^*\right)^2 + \left(v_\beta^*\right)^2} \tag{6.2}$$

hence the modulation index m_a is defined as:

$$m_a = \frac{V_{ref}^*}{E.\cos\left(\frac{\pi}{3}\right)} \tag{6.3}$$

Also, the vector angle is

$$\theta = \tan^{-1} \frac{v_\beta^*}{v_\alpha^*} \tag{6.4}$$

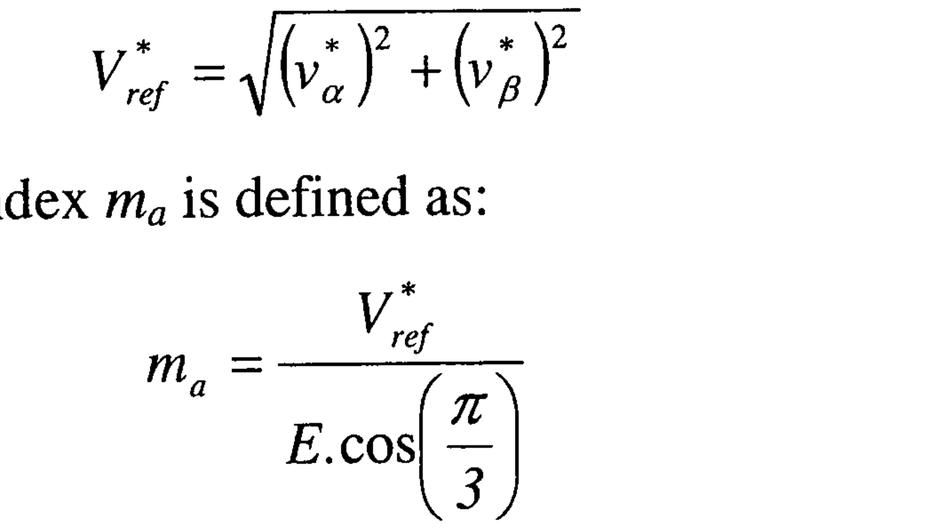


Figure 6.1. The two-level inverter

Figure (6.2) represents the space vector states for the two-level inverter. The vertices of the hexagon represent the six active states of the inverter while the hexagon centre represents the 2 zero output states. For these states, '1' means that the upper switch of the inverter phase leg, shown in figure (6.1), is 'on' and the lower switch is 'off', and '0' means that the lower switch is 'on' and the upper switch is 'off'. Equating the volt-second integral over a sampling period (T_s) of the reference voltage vector and the nearest three states gives:

$$\overline{V_{ref}^{*}}.T_s = \overline{V_1}.t_1 + \overline{V_2}.t_2 + \overline{V_0}.t_0 + \overline{V_7}.t_7 \tag{6.5}$$

where

$$T_s = t_1 + t_2 + t_0 + t_7 \tag{6.6}$$

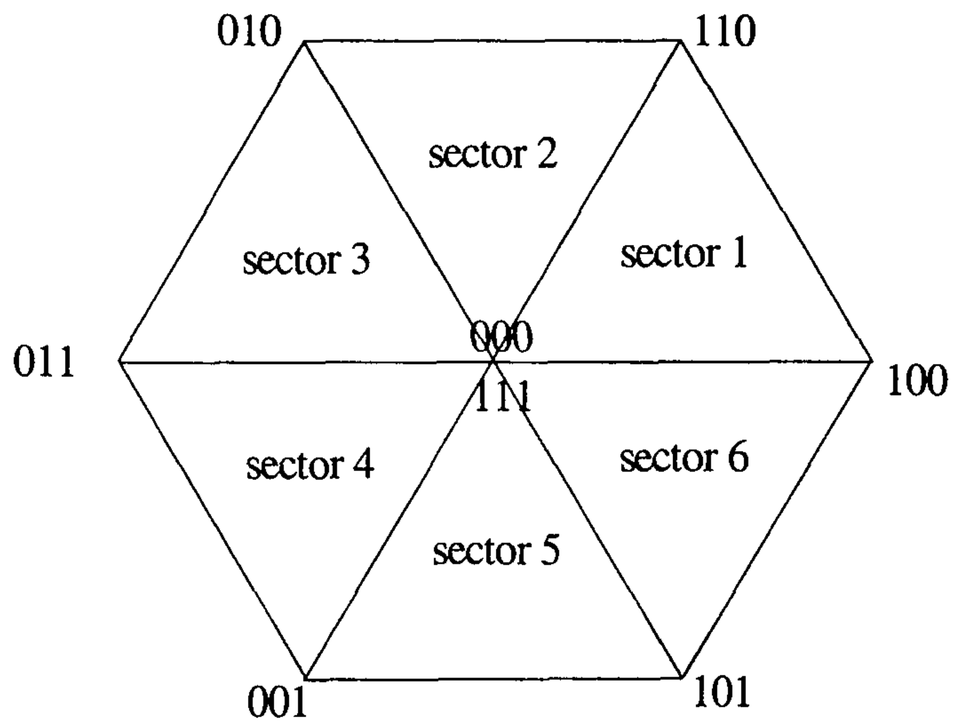


Figure 6.2. Space vector states

The voltage vector states V_1 and V_2 for all the six sectors are shown in Table 6.1, while the vectors V_0 and V_7 are the 000 and 111 states, respectively. The corresponding time periods t_0, t_1, t_2, and t_7 are calculated from equations (6.5) and (6.6).

$$t_1 = m_a T_s \sin\left(\frac{\pi}{3} - \theta\right) \tag{6.7}$$

$$t_2 = m_a T_s \sin(\theta) \tag{6.8}$$

Table 6.1. The states V_1 and V_2 in each sector

Sector \ States	V_1	V_2
1	100	110
2	010	110
3	010	011
4	001	011
5	001	101
6	100	101

From equation (6.6):

$$t_0 + t_7 = T_s - t_1 - t_2 \tag{6.9}$$

It is assumed that t_0 and t_7 are equally distributed so that:

$$t_0 = t_7 = \tfrac{1}{2}(T_s - t_1 - t_2) \tag{6.10}$$

6.2 Phase shifted SVM

A new SVM approach is proposed which overcomes the complexity of specifying normal multilevel space vector modulation. The method reduces DSP execution time, particularly as the number of levels increases. Superposition theory is applied to the multilevel inverter semiconductor switches. Conventional two-level SVM is applied to each three semiconductor switch group of the three-phases and their complementary groups in the multilevel inverter. A pre-calculated shift in time is introduced into the up-down counters of each switch group, then the output is summed and the required output voltage is obtained.

The phase shift depends on the number of levels. The most important advantage of this approach is the simplicity in dealing with the multilevel inverter states which in turn reduces DSP execution time. But the advantage of redundant sequence paths is lost.

6.2.1 Phase-shifted SVM (PS-SVM) implementation

For the five-level cascaded multilevel inverter shown in figure (6.3), the 24 switches are divided into four-groups (each group represents a leg of one cell). These groups can be defined as follows:

- (S_{a1}, S_{b1}, S_{c1}) and their complementary
- (S_{a4}, S_{b4}, S_{c4}) and their complementary
- (S_{a5}, S_{b5}, S_{c5}) and their complementary
- (S_{a8}, S_{b8}, S_{c8}) and their complementary

Two-level SVM is used for each group but the up-down counters are shifted in time as in the phase shift carrier based PWM control technique in [6.1],[6.2].

This time shift (t_{ps}) depends on the number of levels, m, and the sampling time, T_s,

$$t_{ps} = \frac{T_s}{m-1} \tag{6.11}$$

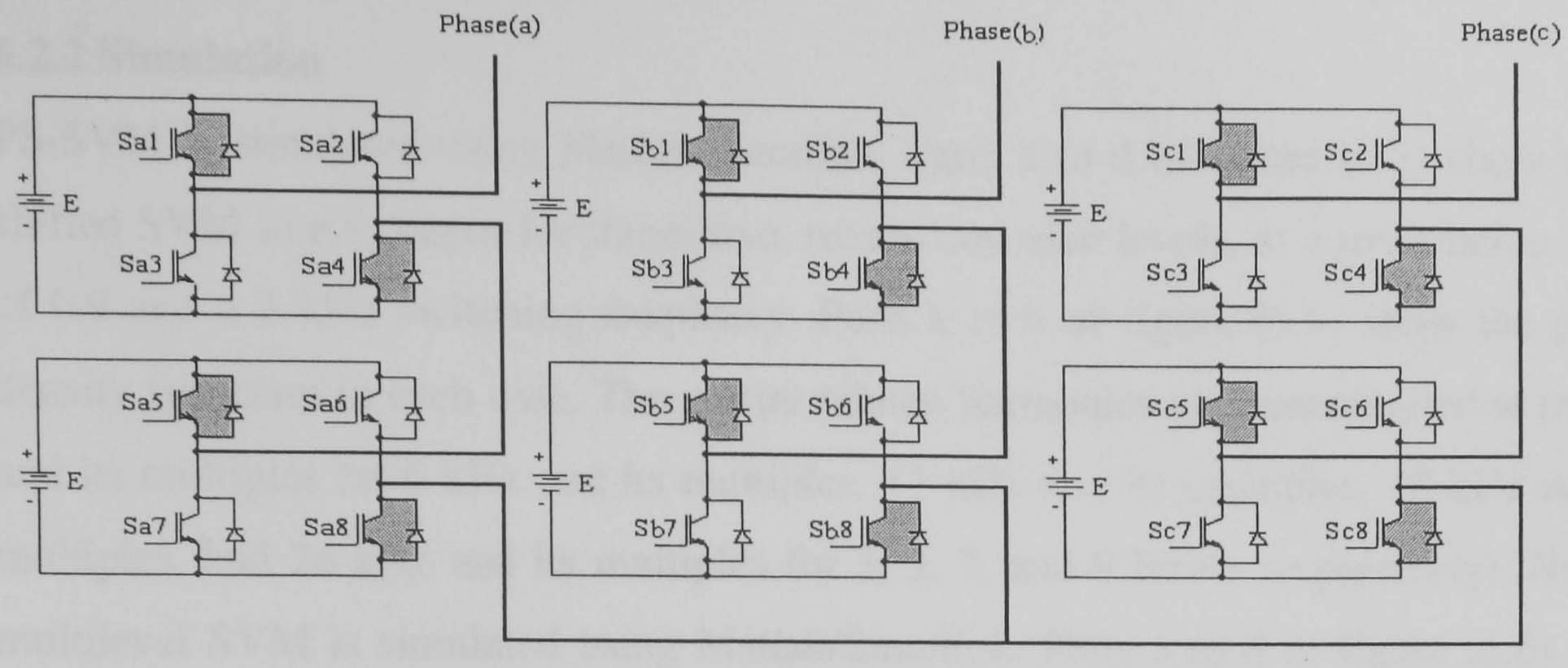


Figure 6.3. Three-phase, five-level cascaded multilevel inverter.

The up-down counter used for the 3-level inverter is shown in figure (6.4a). The three-level inverter is divided into two groups, so there are two up-down counters shifted by $T_s/2$. The up-down counts used for the five-level inverter are shown in figure (6.4b), where the up-down counters are shifted by $T_s/4$. The times (t_0, t_1, t_2, and t_7) are calculated using equations (6.7, 6.8, and 6.10) and then compared with the shifted up-down counters to obtain the required output. The modulation index for m-levels is defined as

$$m_a = \frac{V_{ref}^*}{(m-1).E.\cos\left(\frac{\pi}{6}\right)} \tag{6.12}$$

where E is the voltage per unit cell. With this method, the switching losses are increased by $(m-1)$ times that of normal multilevel SVM. But the carrier harmonics are shifted to $(m-1)f_s$ instead of f_s, as with normal multilevel SVM, where $f_s = 1/T_s$. Also the complexity of the states in normal multilevel SVM, is avoided with PS-SVM.

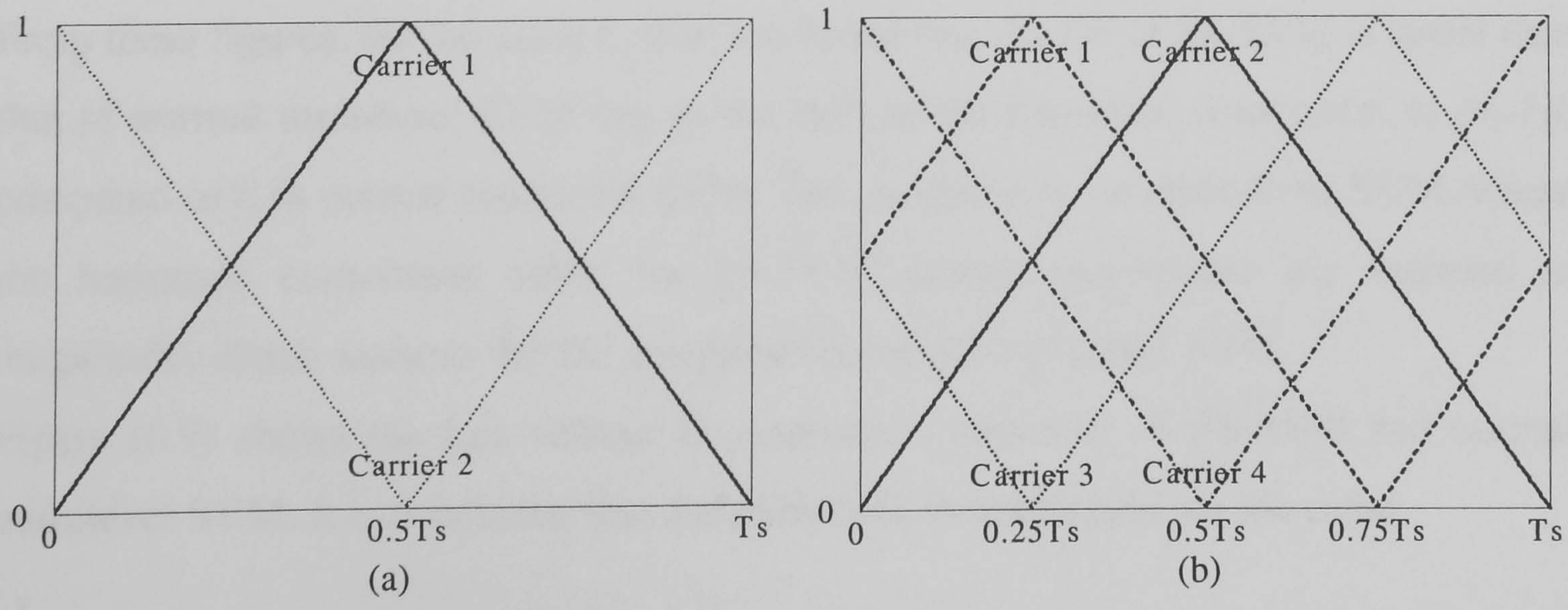


Figure 6.4. The up-down counters used for: (a) 3-level and (b) 5-level inverter

6.2.2 Simulation

PS-SVM is simulated using Matlab/Simulink. Parts a to d of figure (6.5) show phase shifted SVM line voltages for three, five, seven, and nine levels, at a modulation index of 0.9 and a 3 kHz switching frequency. Parts e to h of figure (6.5) show the power density spectrum in each case. The carrier related harmonics are concentrated at $(m-1)f_s$ and its multiples (at 6 kHz and its multiples, 12 kHz and its multiples, 18 kHz and its multiples, and 24 kHz and its multiples for 3, 5, 7, and 9 levels respectively). Normal multilevel SVM is simulated using Matlab/Simulink. Parts a to d of figure (6.6) show normal multilevel SVM line voltage for three, five, seven, and nine levels, at a modulation index of 0.9 and a 3 kHz switching frequency.

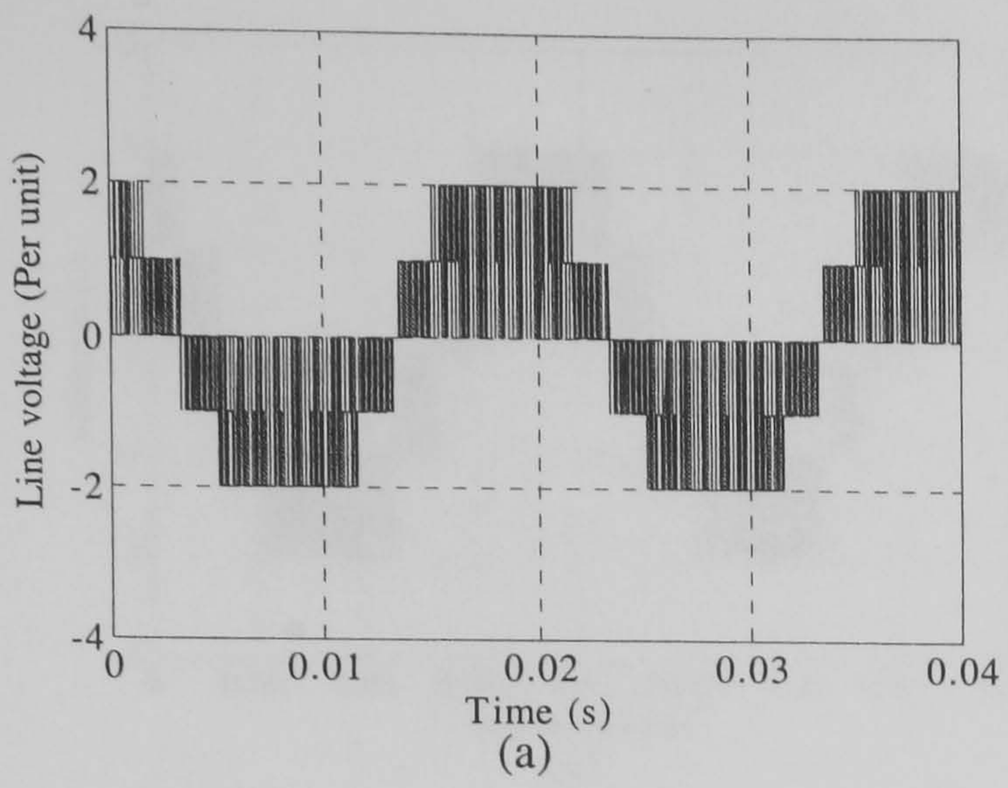
Parts e to h of figure (6.6) show the corresponding power spectrum densities. The harmonics are concentrated at f_s and its multiples (at 3 kHz and its multiples for three, five, seven, and nine levels).

Comparing the spectra of phase-shifted SVM (parts e to h of figure (6.5)) with normal multilevel SVM (parts e to h of figure (6.6)), the harmonic magnitudes of normal multilevel SVM are smaller relative to the corresponding phase-shifted SVM harmonics. Also the harmonics are concentrated around f_s and its multiples in normal multilevel SVM while they are around $(m-1)f_s$ and its multiples in phase-shifted SVM.

Parts a to d of figure (6.7) show the line voltage total harmonic distortion (THD) of PS-SVM and normal multilevel SVM for the four different levels respectively. From these figures, it is concluded that the THD of normal multilevel SVM is better than that of PS-SVM, for all modulation indices.

Parts a to d of figure (6.8) compare the line voltage distortion factor (DF), of PS-SVM, normal multilevel SVM, and normal SVM with the same switching frequency per switch as in PS-SVM ($2f_s$, $4f_s$, $6f_s$, and $8f_s$ for the four different levels respectively). From these figures, for the same f_s, it is concluded that the DF of PS-SVM is better than that of normal multilevel SVM due to the shift in the harmonic component to $(m-1)f_s$ compared to f_s in normal multilevel SVM. The exception is for three-level SVM, where the harmonic component shifts for PS-SVM cannot compensate the increase in magnitude, which worsens the DF compared to normal multilevel SVM.

Figure (6.9) shows the line voltage fundamental component of PS-SVM and normal multilevel SVM. It is concluded that the gains of both techniques are the same.



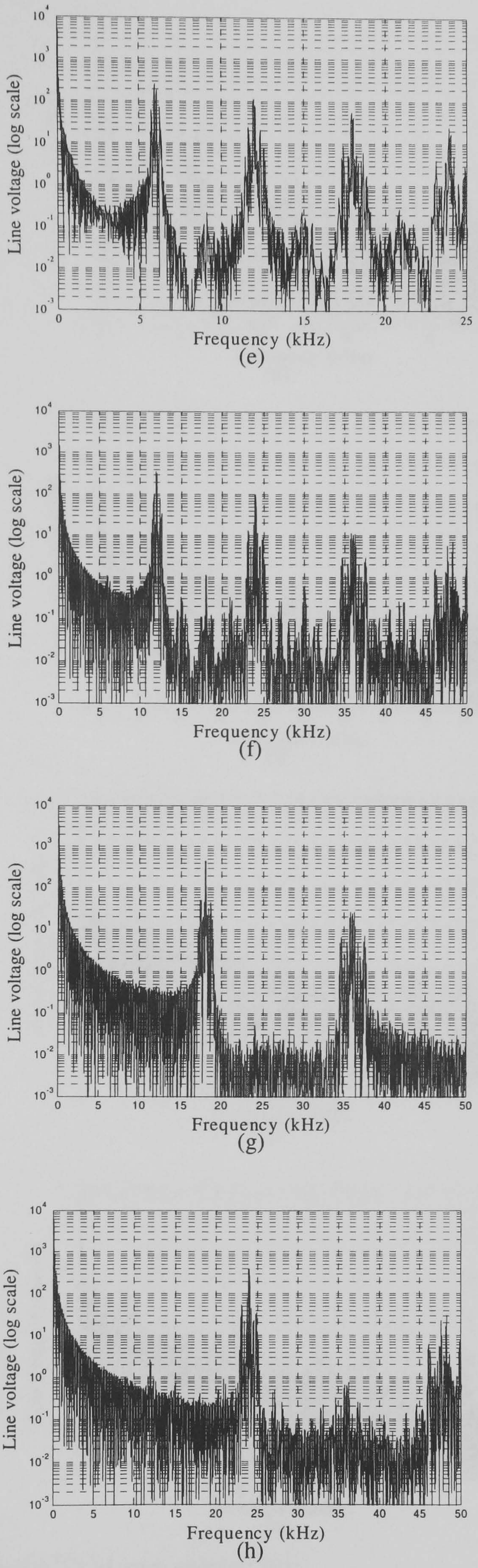
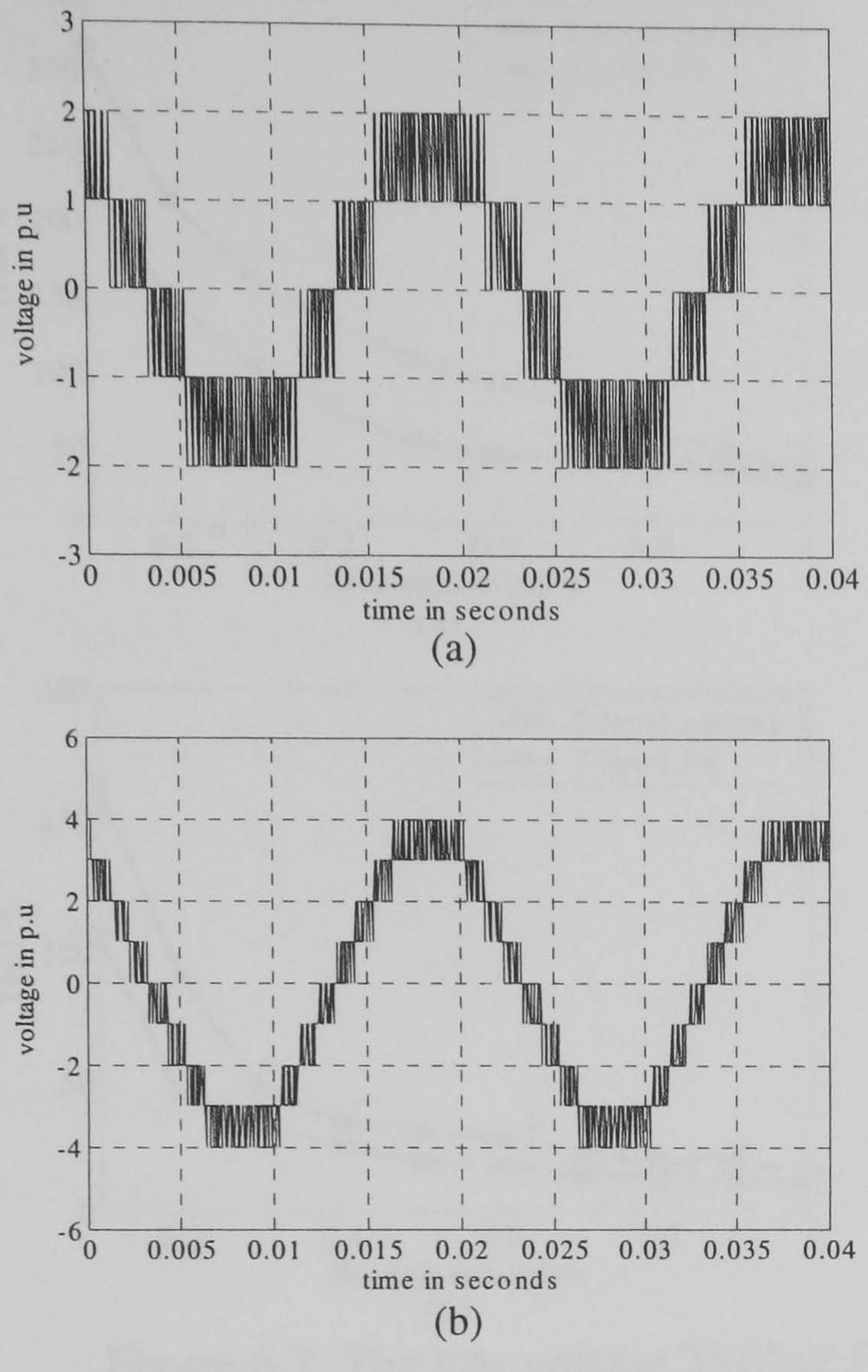
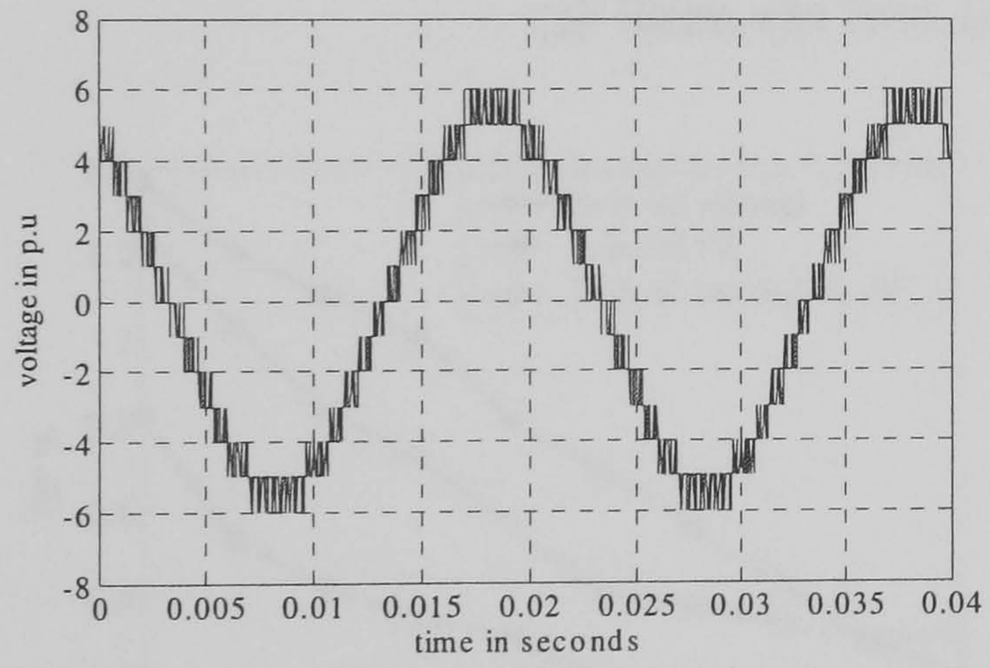


Figure 6.5. The line voltage using PS-SVM for:
(a) three, (b) five, (c) seven, and (d) nine levels and their respective power density spectrum (e), (f), (g), and (h) at $m_a = 0.9$ and $f_s = 3$ kHz

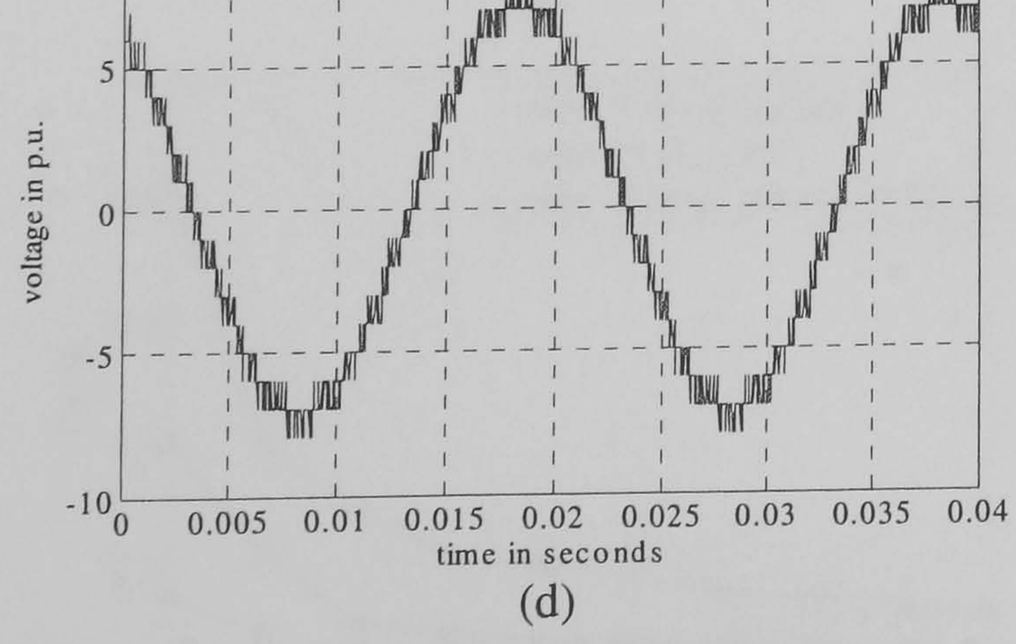


(a)

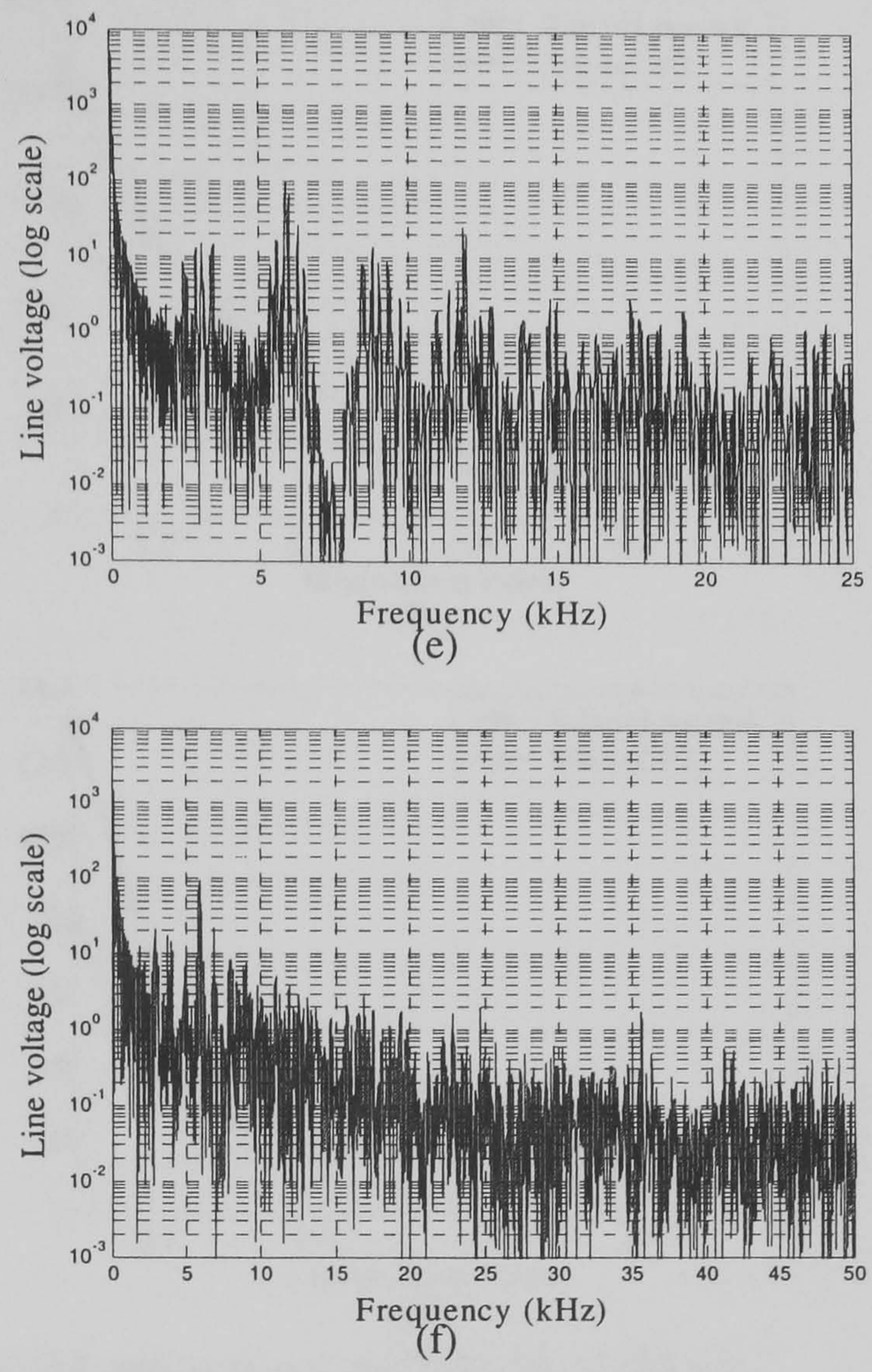
(b)



(c)

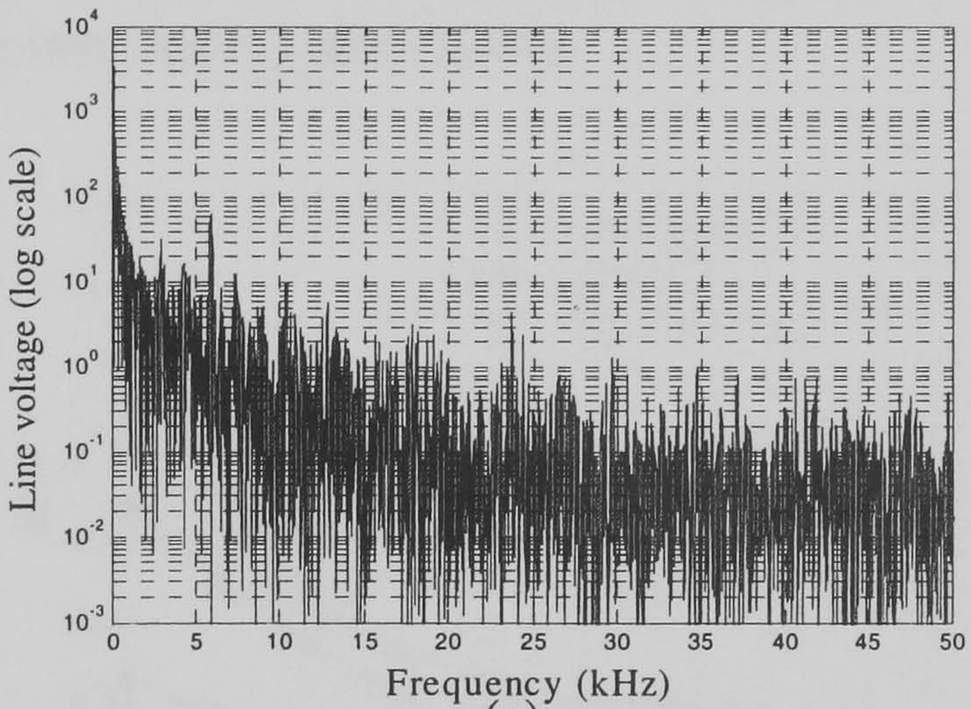


(d)

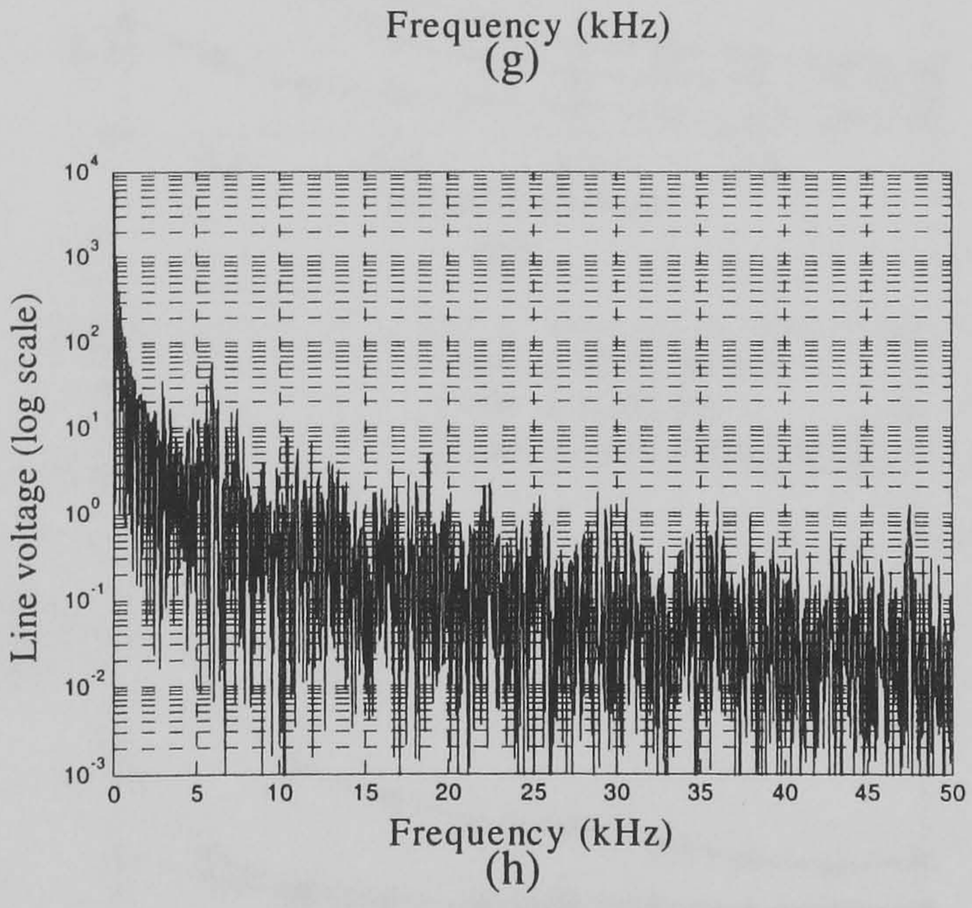


(e)

(f)

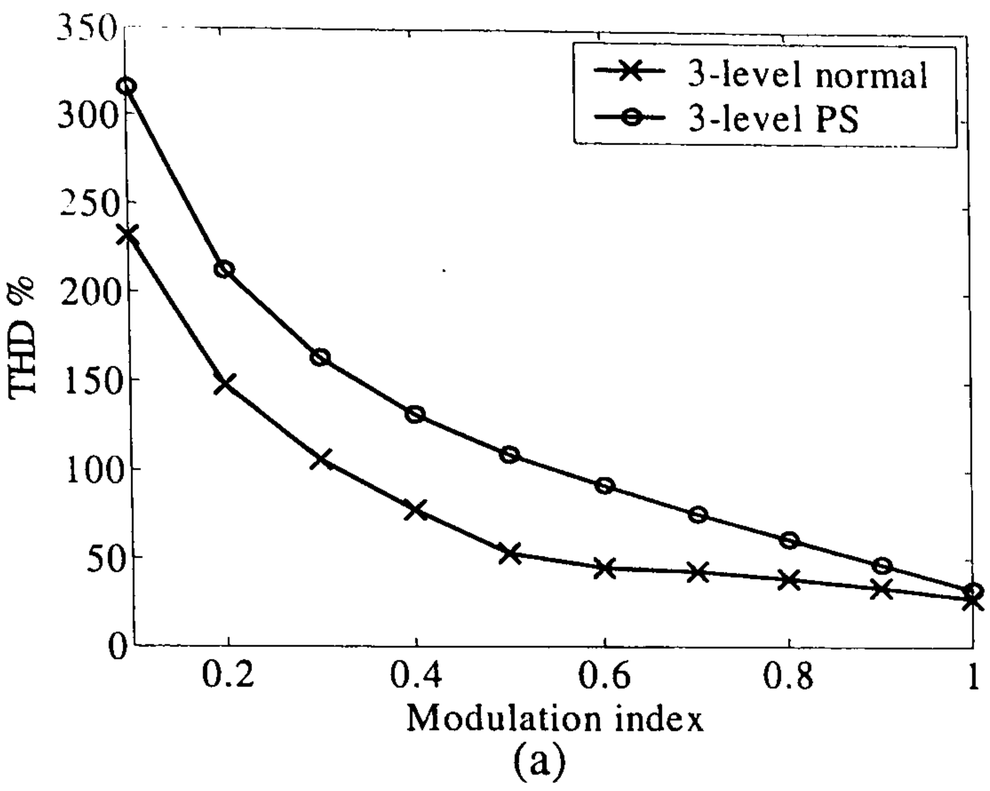


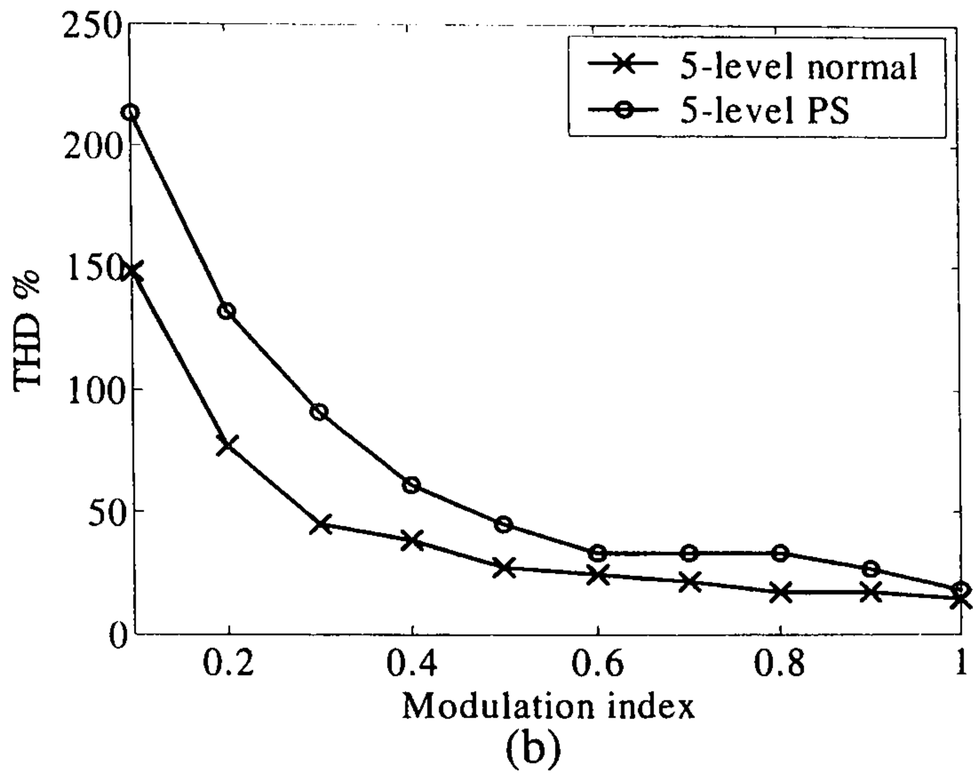
(g)

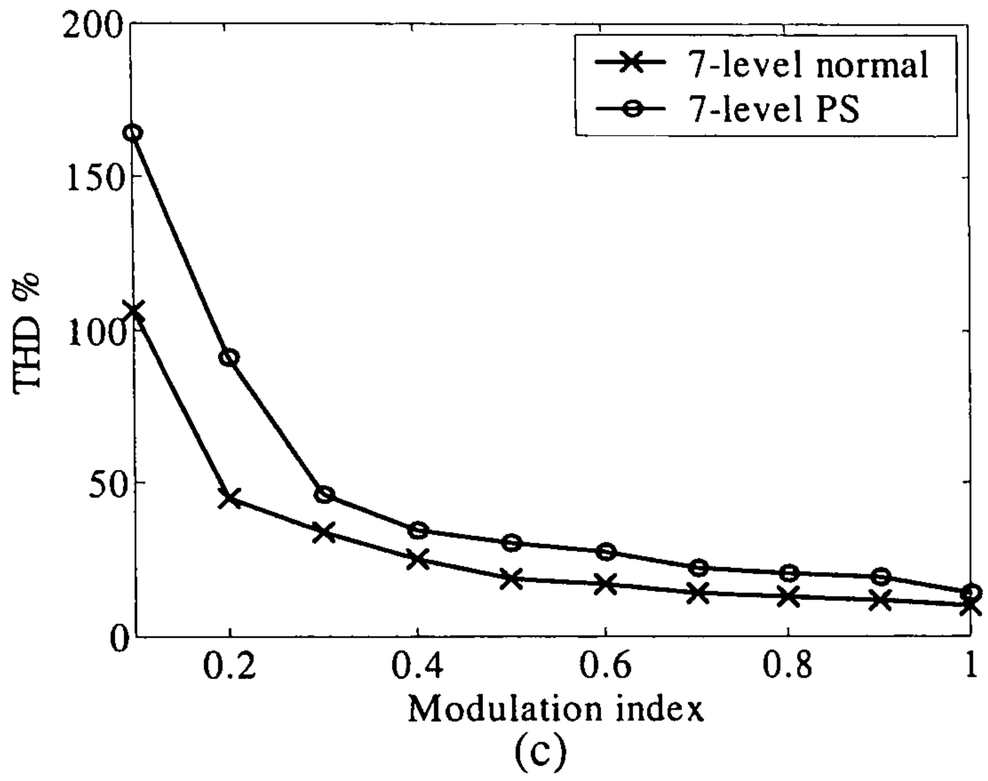


(h)

Figure 6.6. Normal multilevel SVM line voltage for:
(a) three, (b) five, (c) seven, and (d) nine levels and their respective power density spectrum (e), (f), (g), and (h) at $m_a = 0.9$, $f_s = 3$ kHz







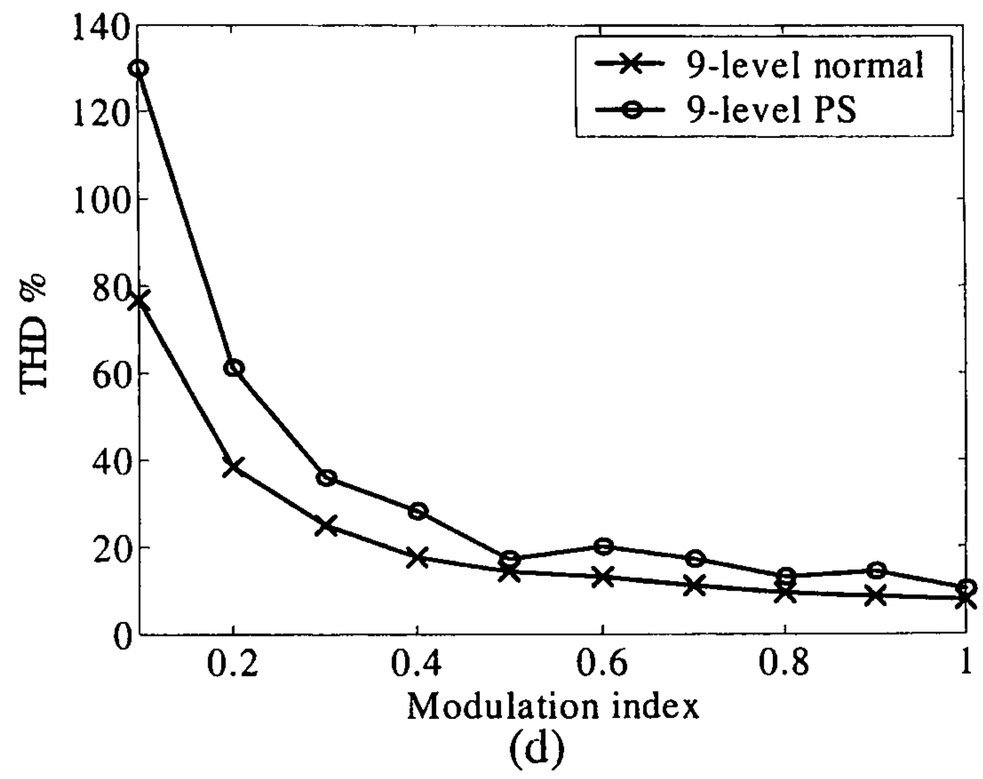
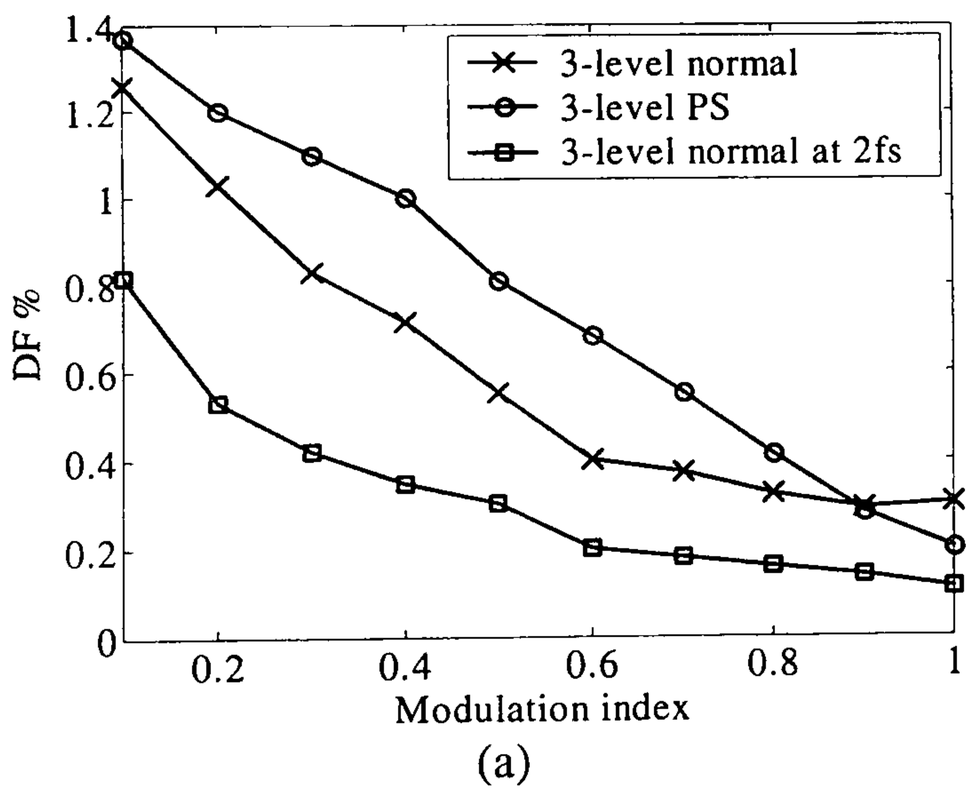
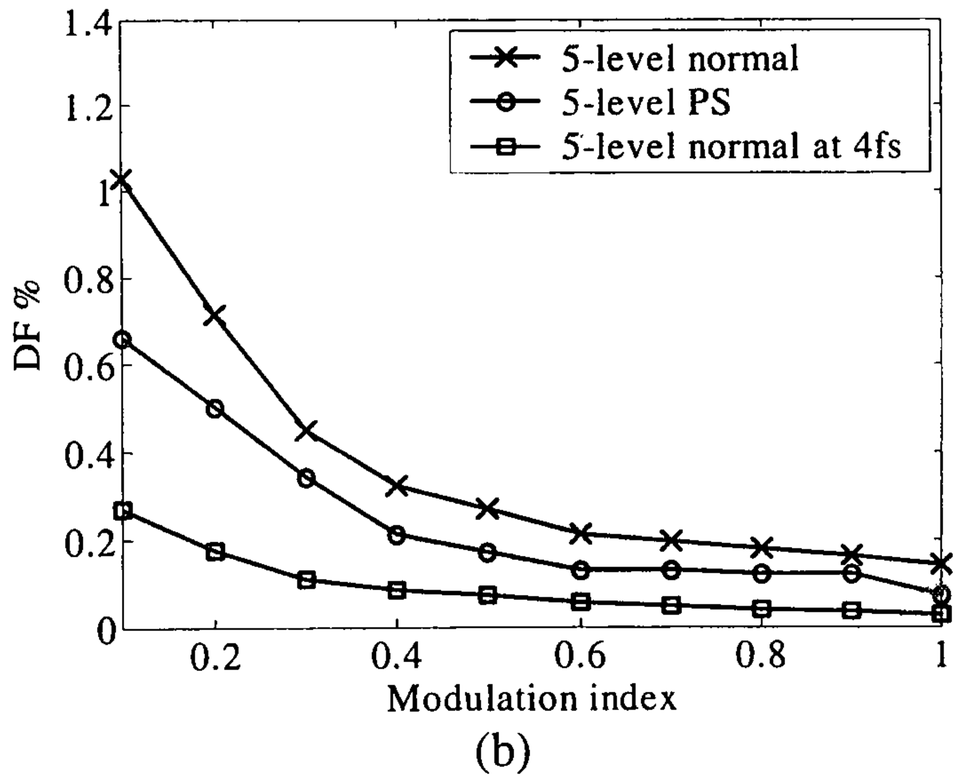
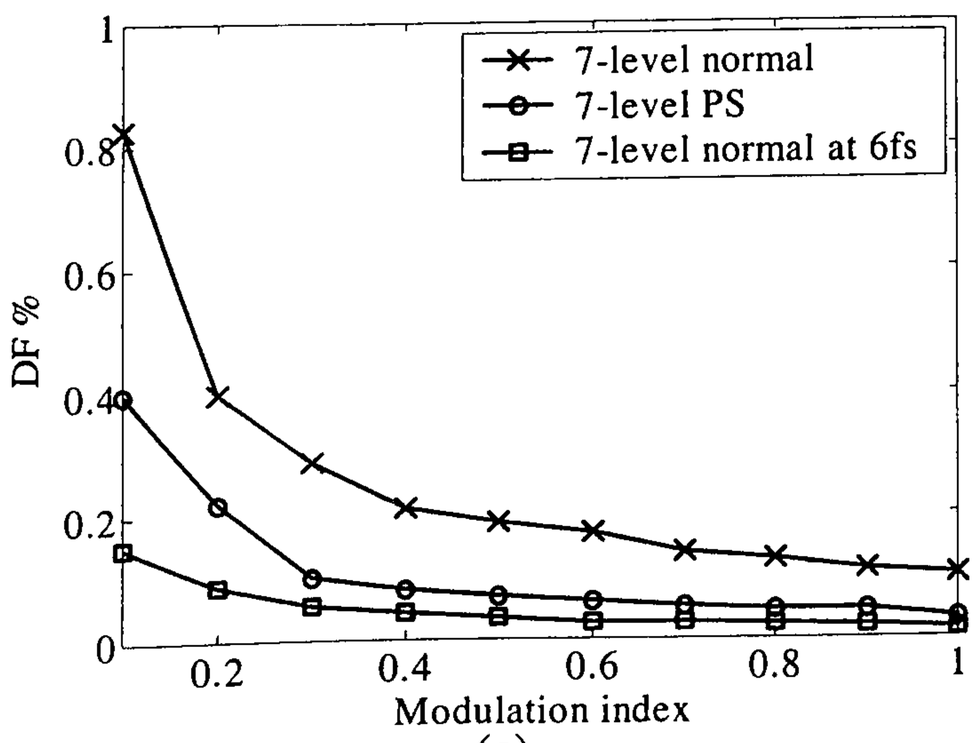


Figure 6.7. The line voltage THD of PS-SVM and normal multilevel SVM for: (a) three, (b) five, (c) seven, and (d) nine levels







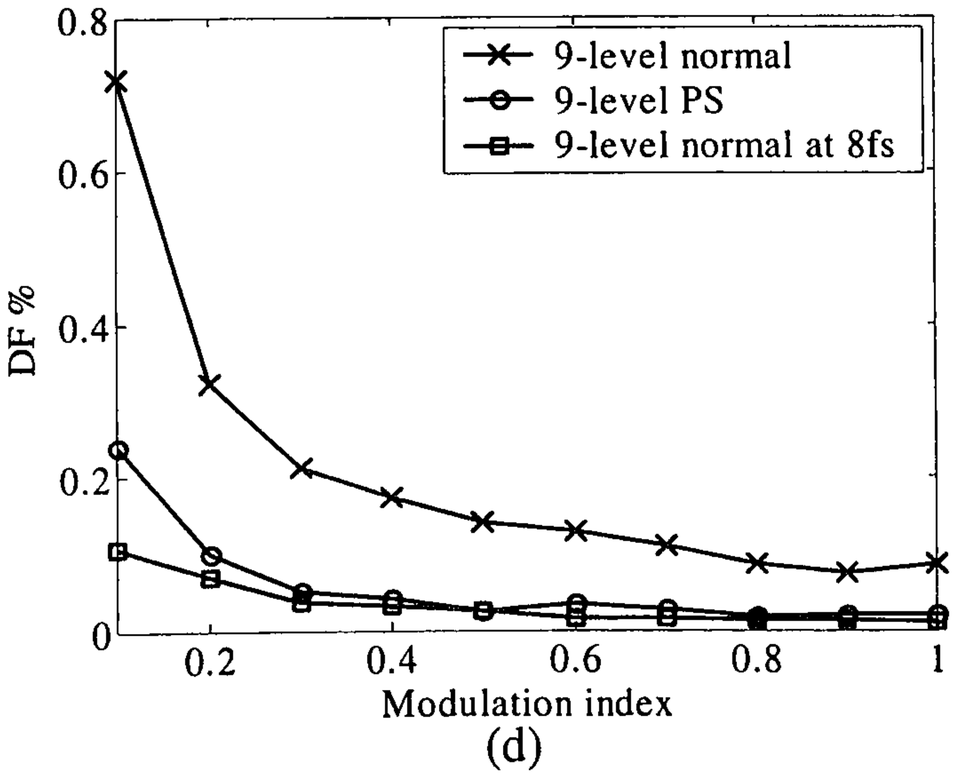


Figure 6.8. The line voltage DF of PS-SVM and normal multilevel SVM for: (a) three, (b) five, (c) seven, and (d) nine levels

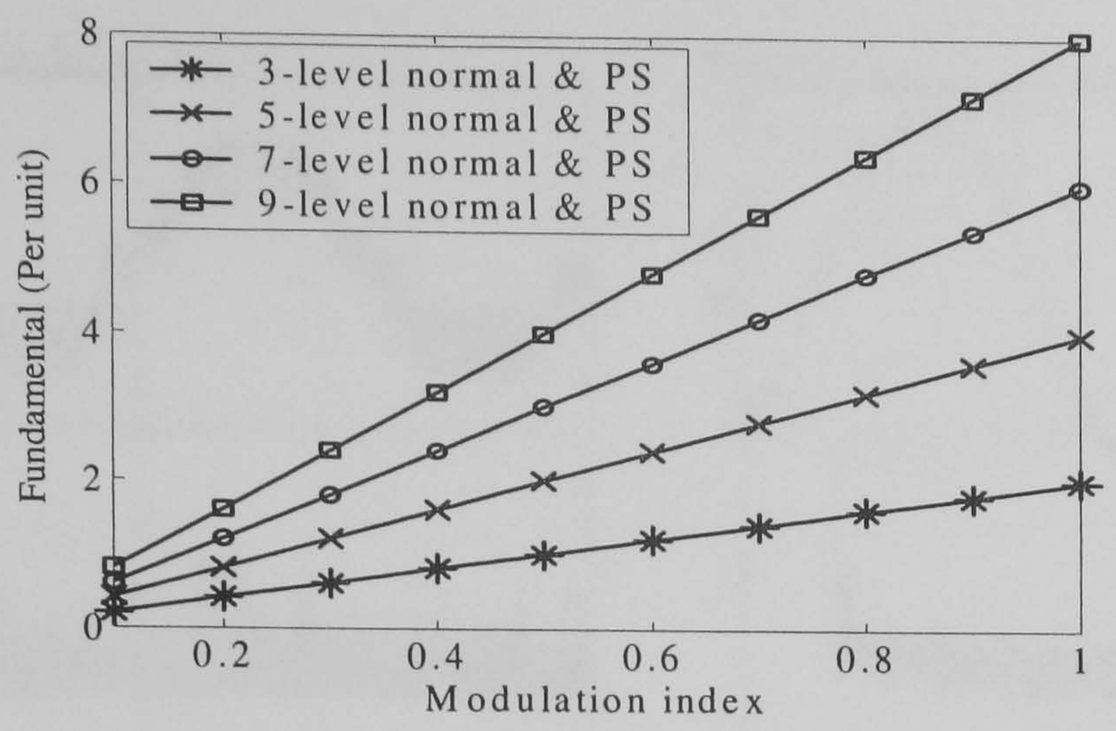
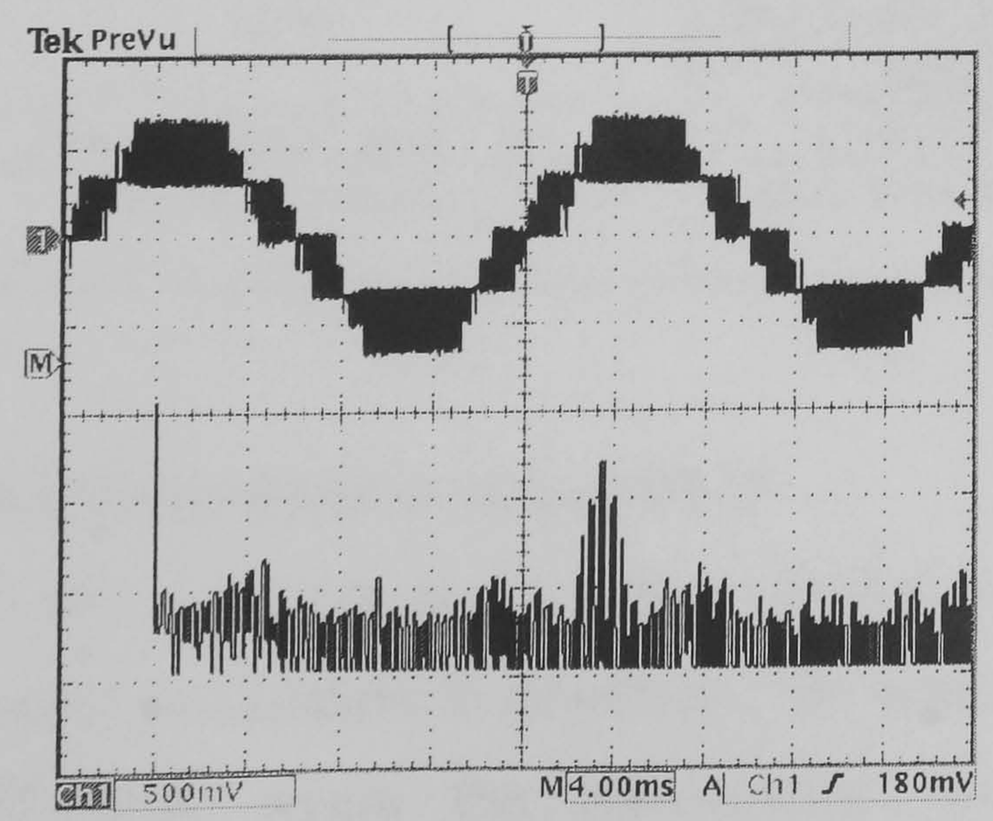


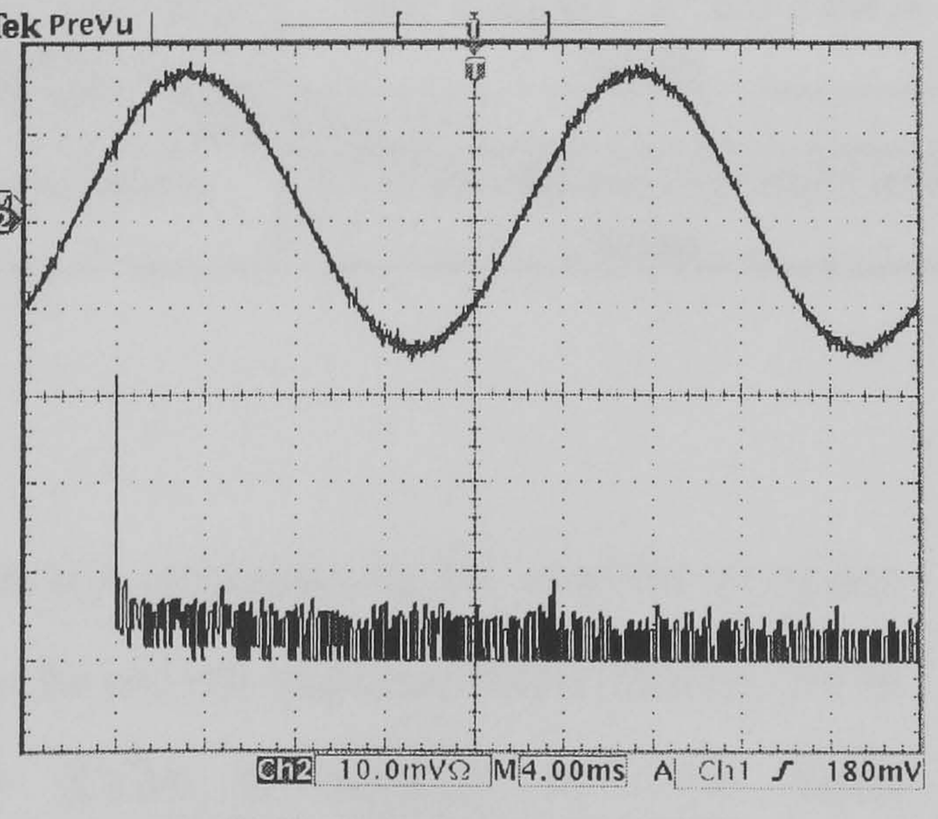
Figure 6.9. Line voltage fundamental component of PS-SVM and normal multilevel SVM

6.2.3 Practical results

The proposed algorithm is implemented using DSP software (Code Composer(see Appendix C.1)) and feeds the timing distribution of the states (t_0, t_1, t_2) and the corresponding states to the AED106. The execution time of the program is 18 μs, independent of the number of levels while the execution time of a generalized algorithm for normal multilevel SVM is 44 μs. PWM generation and the underlap time for the switches (640 ns) are implemented in the Xilinx FPGA. To obtain the required shifted up-down counters, presettable up-down counters are configured in the FPGA. The inverter is a 3-phase 5-level cascaded type (H-bridge) with a 3-phase R-L load (R = 17 Ohm, L = 20 mH). The DC link capacitors are six 450 V/2200 μF, and the switching frequency is 3.051 kHz. These parameters are used in all the schemes in this chapter. Parts a and b of figure (6.10) show the output line voltage, the phase current, and spectrums for phase-shifted SVM at a modulation index (m_a) of 0.866. Parts c and d of figure (6.10) show the same outputs but for m_a = 2. The low order harmonics in the current spectrum in figure (6.10d) are minimized with the proposed over modulation technique.



(a)



(b)

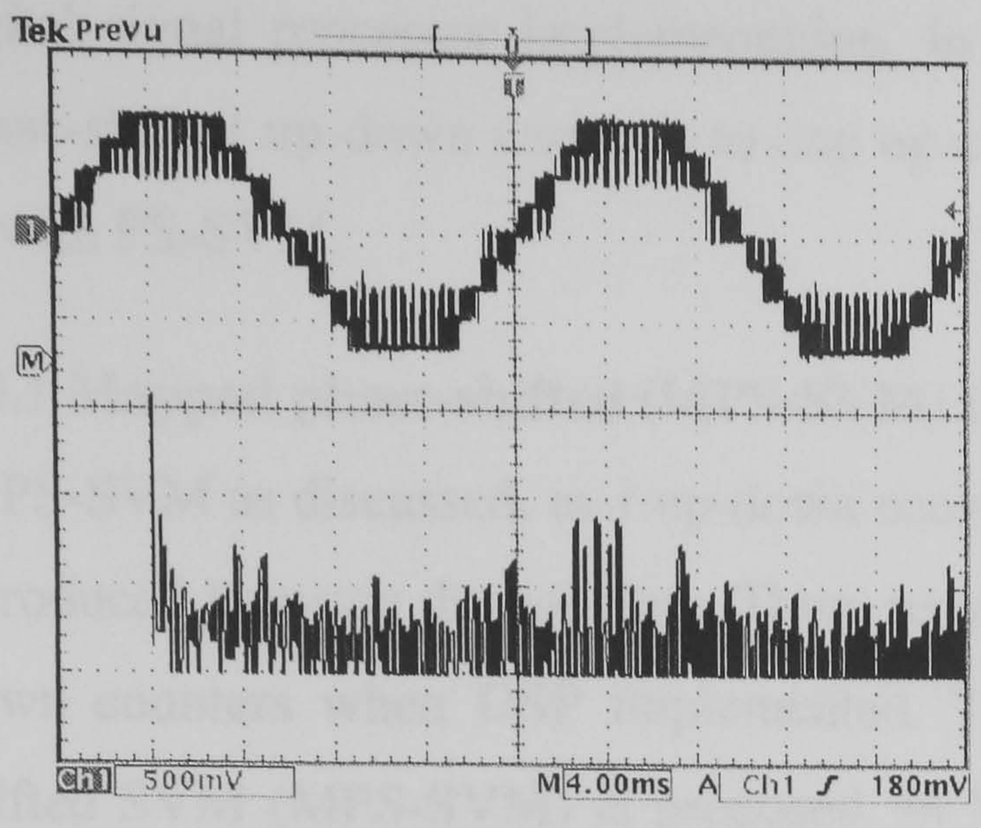


Figure 6.10. The output line voltage and phase current and spectrums (semi log) for phase-shifted SVM (a) and (b) for modulation index (m_a) = 0.866 (c) and (d) for modulation index (m_a) = 2 (power factor of 0.938 lag) (100V/div & 2A/div)

The simulation results (harmonic position and switching frequency) for PS-SVM are validated by the practical results in figure (6.10). Table 6.2 summarizes a comparison between PS-SVM and normal multilevel SVM characteristics.

Table 6.2. Comparison between PS-SVM and normal multilevel SVM.

	Phase shifted SVM	Normal SVM
Counter	*(m-1)* counters shifted from each other by $T_s/(m-1)$	Single counter
Total number of switchings per fundamental cycle	Higher, ((*m-1*) times that of generalized SVM)	Lower
Line voltage THD	Worse	Better
Line voltage DF	Better	Worse
Harmonic spectrum	Shifted to $(m-1)f_s$	Shifted to f_s
Execution time	18 µs	44 µs
Redundant sequence of paths	No	Yes
Complexity	The well-known 2-level SVM	More complex
dv/dt	A transition of more than one level may be in the line voltage	Lower
States	The 8-states of the well-known 2-level SVM are used	More complex (m^3 states for *m*-levels)
Line voltage fundamental	The same	
Number of levels	Used for odd number of levels	Used for odd and even number of levels

6.3 Mapped phase-shifted SVM

A new approach, mapped phase-shifted space vector modulation, for multilevel space vector modulation is presented. The approach is based on superposition theory, as in PS-SVM, where the conventional two-level SVM is applied to each three semiconductor switch group of the three phases and their complementary groups in multilevel inverter. For PS-SVM, shifted up-down counters used cause a bottleneck for

digital signal processor implementation. In the proposed approach, a mapping of the phase-shifted up-down counters to one up-counter is proposed, giving the same output as with PS-SVM.

6.3.1 Mapped phase-shifted (MPS-SVM) implementation

In PS-SVM as discussed, *m-1* up-down counters are used with a phase shift of $T_{sw}/(m-1)$ introduced between the counters. There remains a problem with using phase shifted up-down counters when DSP implemented. To overcome this problem, mapped phase-shifted SVM (MPS-SVM) is proposed. In MPS-SVM, the effect of the phase shifting the up-down counters is mapped into the sampling time distribution among the nearest three states thereby using only one up counter, yet producing the same output as in phase shifted SVM. In the following sub-sections, MPS-SVM is explained for the three, five, and seven levels.

i. Three-level mapped phase shifted SVM

In PS-SVM for the three-level cascaded type inverter shown in figure (6.11), there are two groups of semiconductor switches. The first group is S_{a1}, S_{b1}, and S_{c1} and their complementary S_{a3}, S_{b3}, and S_{c3}. The second group is S_{a4}, S_{b4}, and S_{c4} and their complementary S_{a2}, S_{b2}, and S_{c2}. Note that the main switches of each group are in grey. These two groups can be treated as if they are separate two two-level inverters controlled by the conventional two-level SVM but with two up-down counters shifted by $T_{sw}/2$, as shown in figure (6.12). Figure (6.13) indicates one switching cycle in sector 1, for the two shifted up-down counters associated with the main switches of each group.

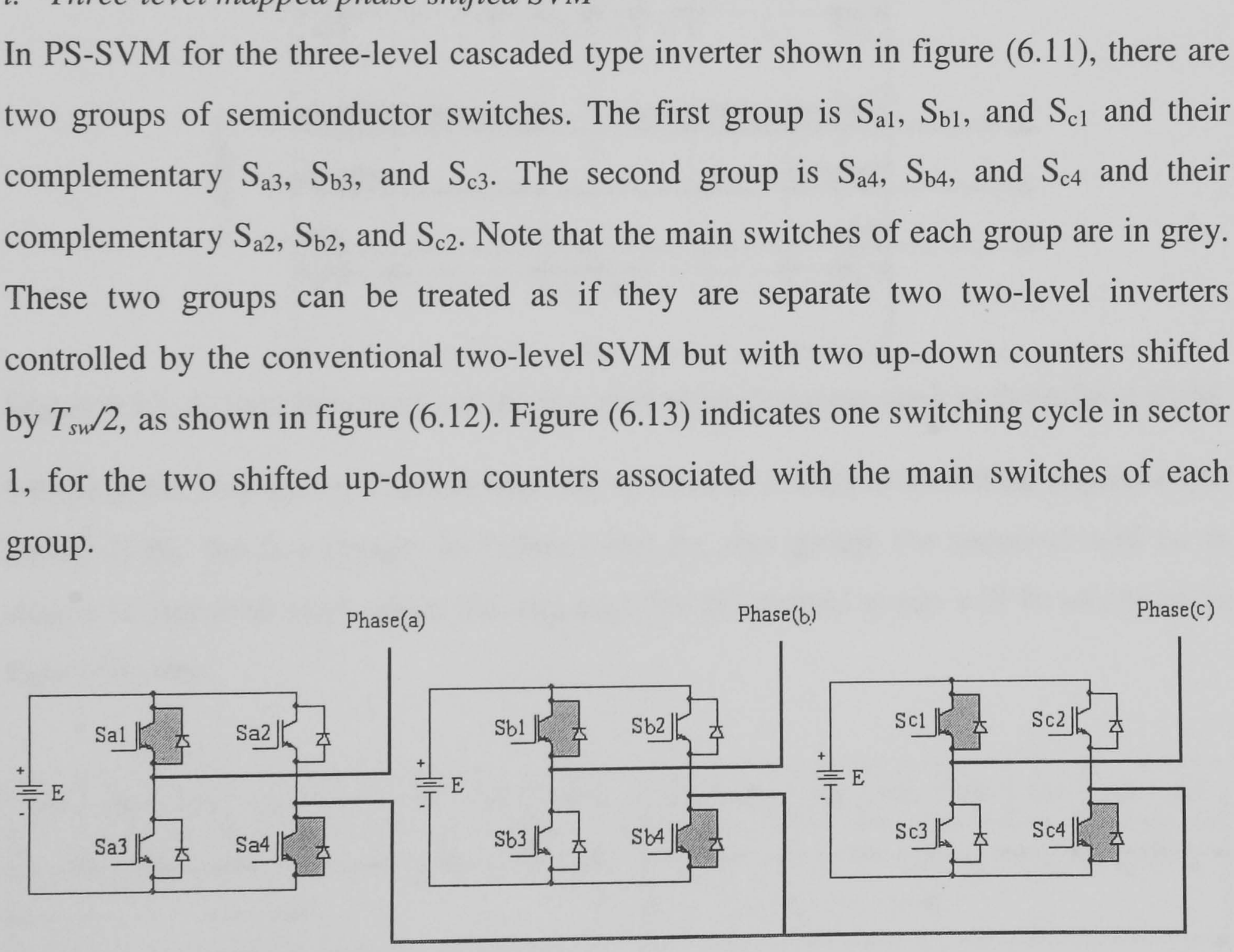


Figure 6.11. Three-level cascaded inverter

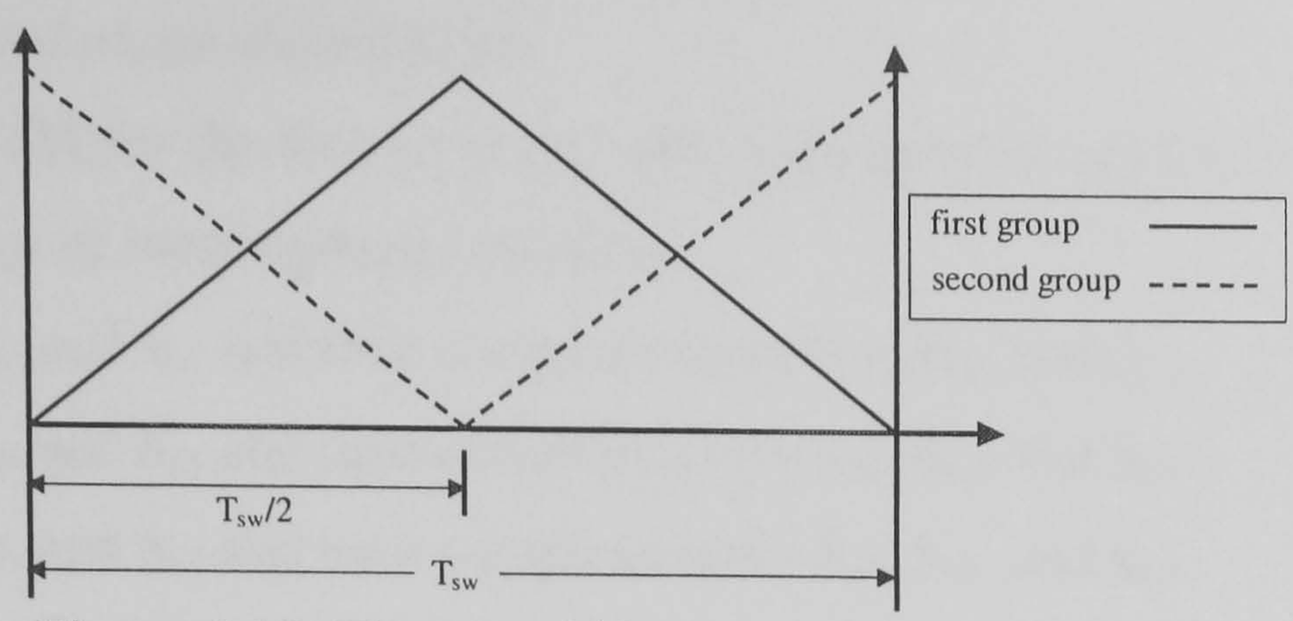


Figure 6.12. The two shifted up-down counters

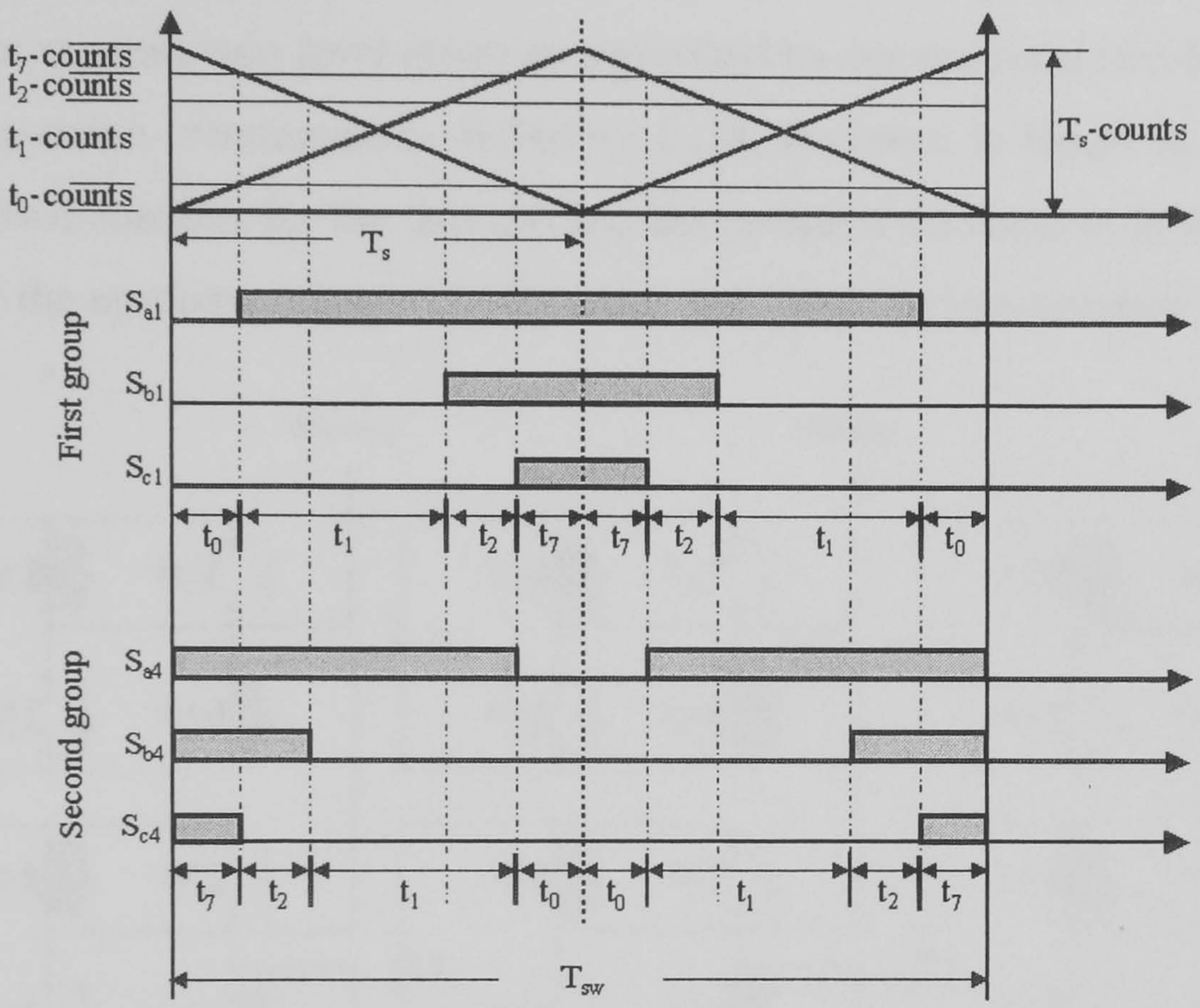


Figure 6.13. A switching cycle of the two shifted up-down counters in three-level SVM.

Mapping the 2 up-down counters into one up counter results in a rotating sequence (for sector 1) for the two groups as follows. For the first group, the sequence will be as shown in figure (6.14a), while the sequence for the second group will be as shown in figure (6.14b).

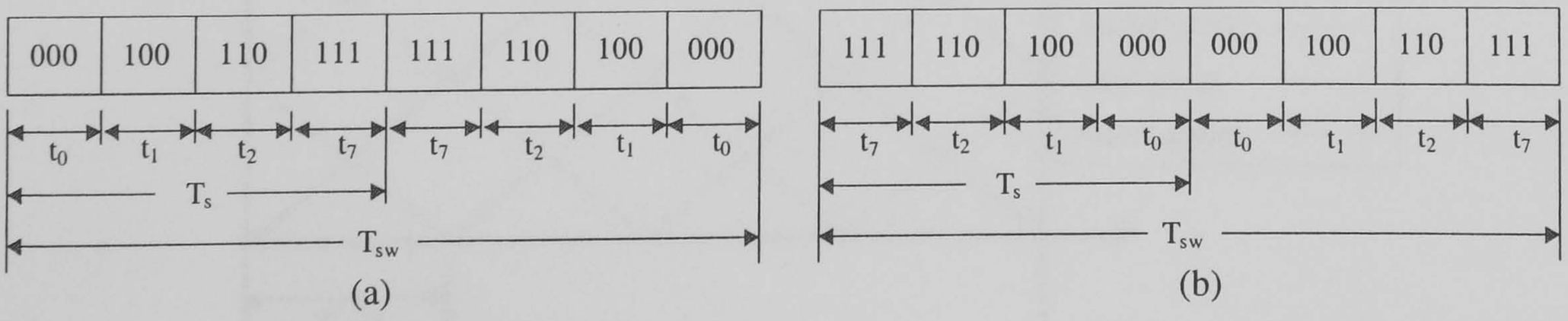


Figure 6.14. The sequence of states for the two groups in three-level inverter: (a) the first group and (b) the second group

ii. Five-level mapped phase-shifted SVM

In phase shifted SVM for the five-level cascaded type inverter shown in figure (6.15), there are four groups of semiconductor switches.

Group 1: is S_{a1}, S_{b1}, and S_{c1} and their complementary S_{a3}, S_{b3}, and S_{c3}.

Group 2: is S_{a4}, S_{b4}, and S_{c4} and their complementary S_{a2}, S_{b2}, and S_{c2}.

Group 3: is S_{a5}, S_{b5}, and S_{c5} and their complementary S_{a7}, S_{b7}, and S_{c7}.

Group 4: is S_{a8}, S_{b8}, and S_{c8} and their complementary S_{a6}, S_{b6}, and S_{c6}.

The main switches of each group are shown in grey. The four groups can be treated as if they are four separate two-level inverters controlled by conventional two-level SVM but with four up-down counters each shifted by $T_{sw}/4$, as shown in figure (6.16). Mapping of the up-down counters for the first and second groups is the same as in section (6.3.1*i*) Mapping of the up-down counters for the third and fourth groups involves two cases.

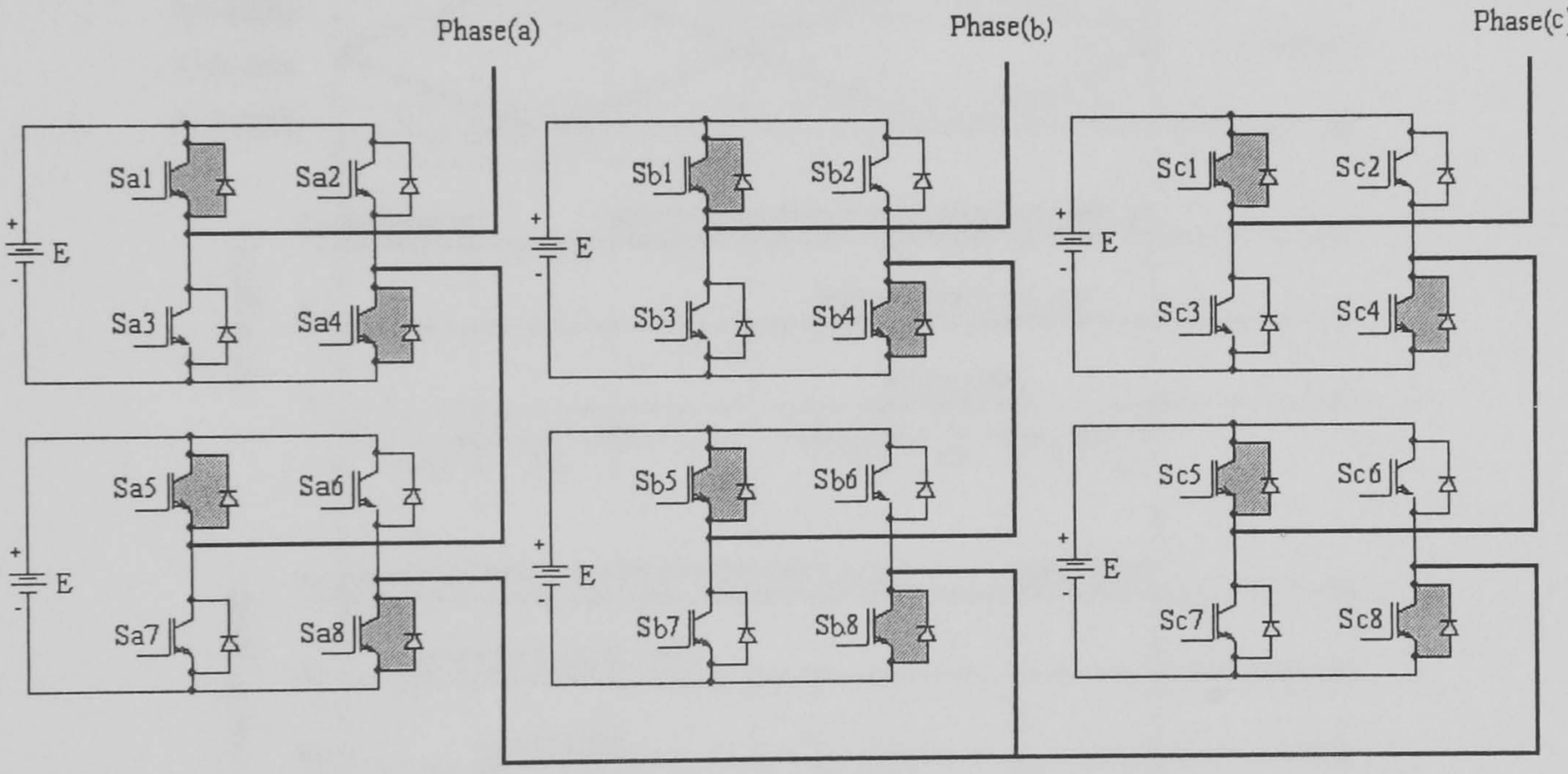


Figure 6.15. Five-level cascaded inverter

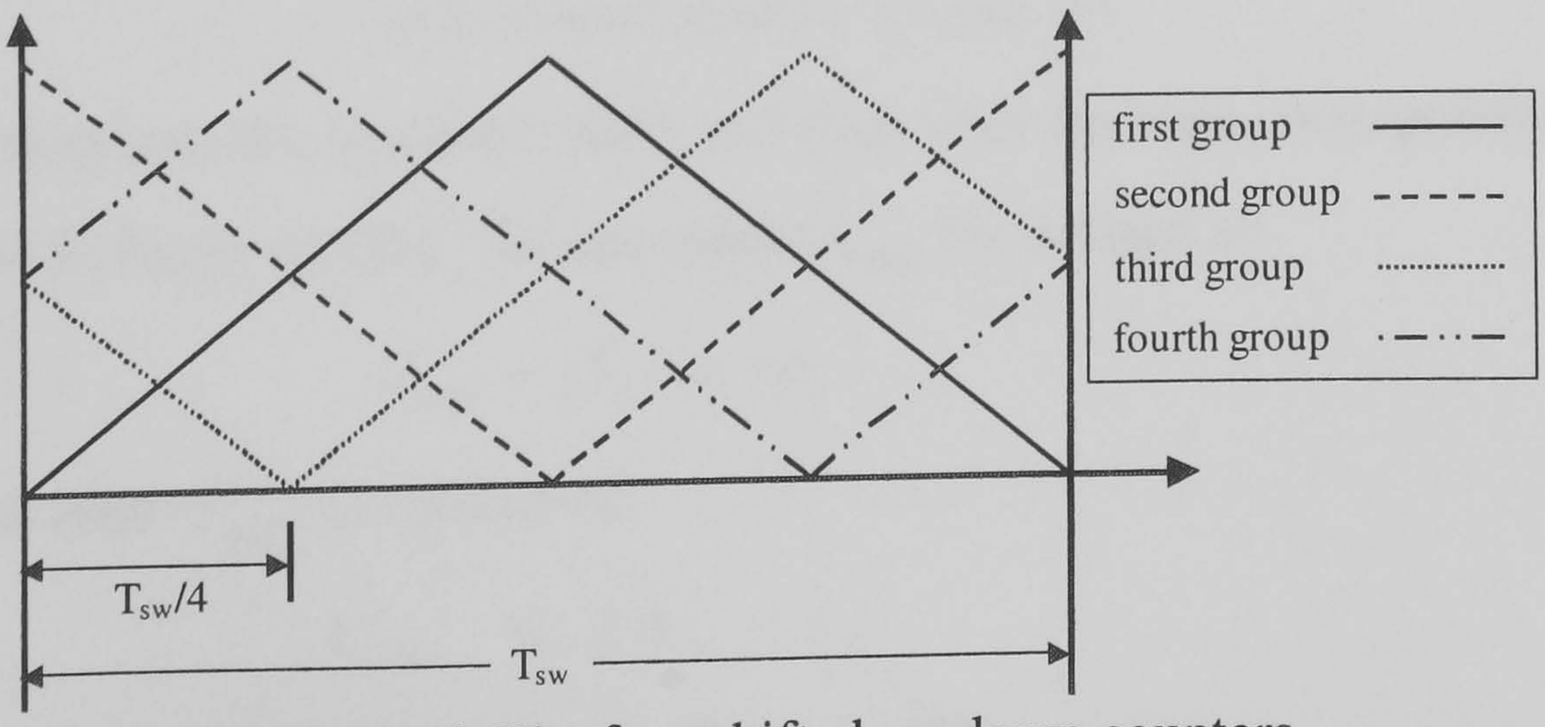


Figure 6.16. The four shifted up-down counters

- ***Case (1):*** $t_7 + t_2 < \frac{1}{2}T_s$

Figure (6.17) illustrates case (1) for the third and fourth groups, over one switching cycle. The condition for case (1) is $t_7 + t_2 < \frac{1}{2}T_s$

The third group sequence starts and ends with a state corresponding to time (t_1), as shown in figure (6.18a). The start time (t_{1start}) is defined as:

$$t_{1start} = \frac{1}{2}T_s - t_0 \tag{6.13}$$

while the end time (t_{1end}) is defined as:

$$t_{1end} = \frac{1}{2}T_s - t_7 - t_2 \tag{6.14}$$

and the sequence of states is indicated in figure (6.18a)

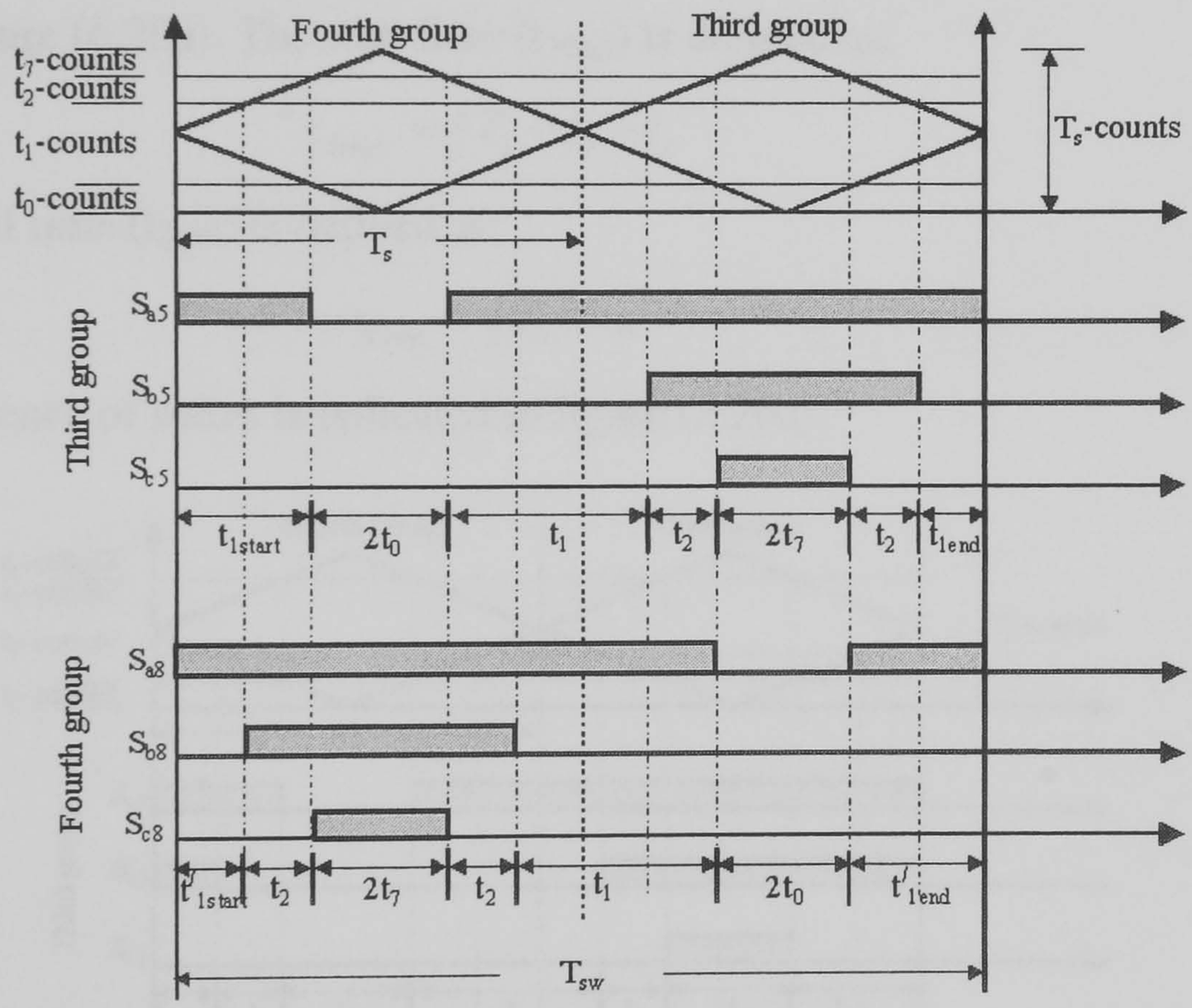


Figure 6.17. One switching cycle of the up-down counters of the third and fourth group in five-level inverter in case (1)

For the fourth group, the sequence starts and ends with the state corresponding to time (t_1), as shown in figure (6.18b). The start time (t'_{1start}) is defined as:

$$t'_{1start} = \frac{1}{2}T_s - t_7 - t_2 \tag{6.15}$$

while the end time (t'_{1end}) is defined as:

$$t'_{1end} = \frac{1}{2}T_s - t_0 \tag{6.16}$$

and the sequence of states is indicated in figure (6.18b).

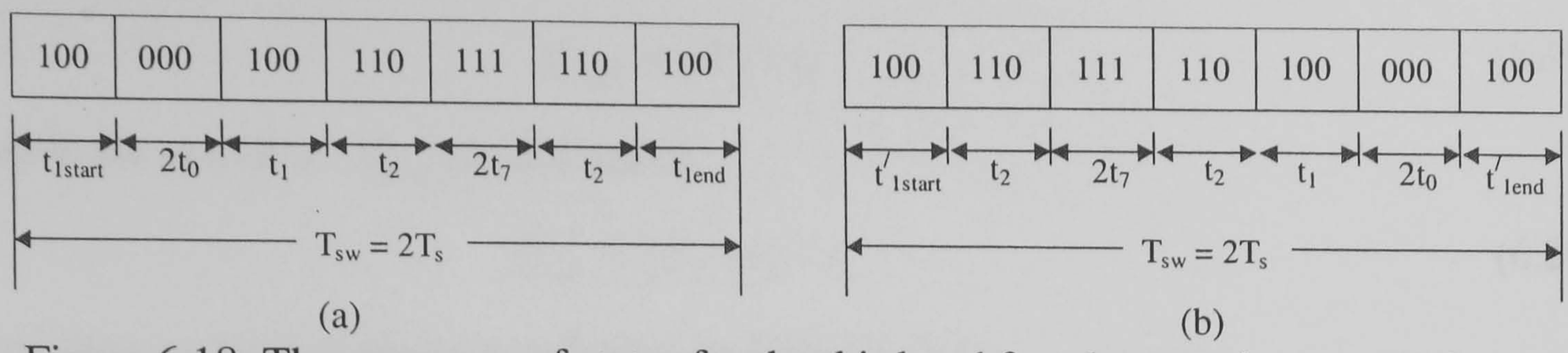


Figure 6.18. The sequence of states for the third and fourth group in case (1) for the five-level inverter
(a) the first group and (b) the second group

- ***Case (2):*** $t_7 + t_2 \geq \frac{1}{2}T_s$

Figure (6.19) illustrates case (2) for the third and fourth groups, over one switching cycle. The condition for case (2) is $t_7 + t_2 \geq \frac{1}{2}T_s$

The third group sequence starts and ends with a state corresponding to time (t_2), as shown in figure (6.20a). The start time (t_{2start}) is defined as:

$$t_{2start} = \frac{1}{2}T_s - t_0 - t_1 \tag{6.17}$$

while the end time (t_{2end}) is defined as:

$$t_{2end} = \frac{1}{2}T_s - t_7 \tag{6.18}$$

and the sequence of states is indicated in figure (2.20a)

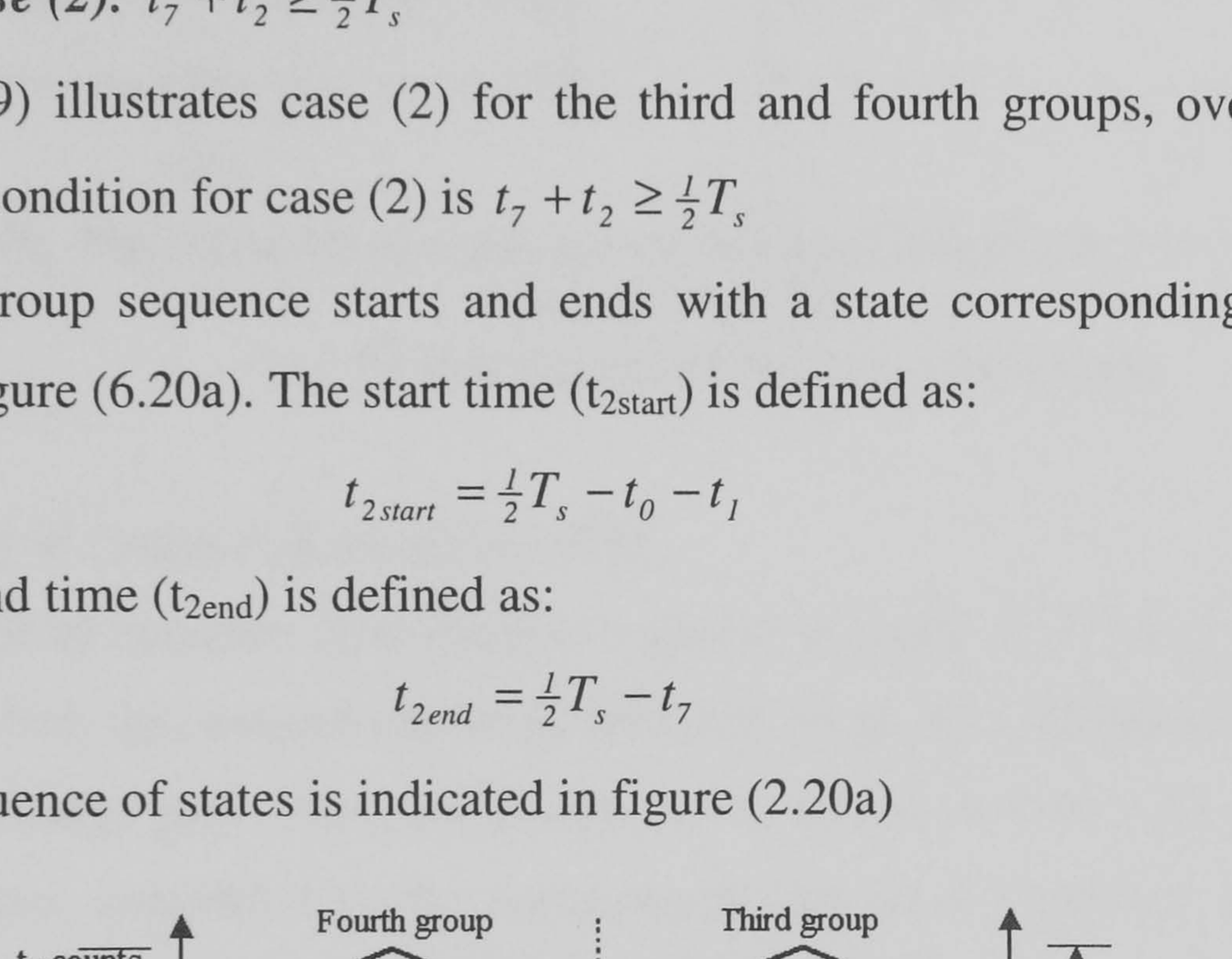


Figure 6.19. One switching cycle of the up-down counters of the third and fourth group in five-level inverter in case (2)

For the fourth group, the sequence starts and ends with the state corresponding to time (t_2), as shown in figure (6.20b). The start time (t'_{2start}) is defined as:

$$t'_{2start} = \tfrac{1}{2}T_s - t_7 \tag{6.19}$$

while the end time (t'_{2end}) is defined as:

$$t'_{2end} = \tfrac{1}{2}T_s - t_0 - t_1 \tag{6.20}$$

and the sequence of states is indicated in figure (6.20b).

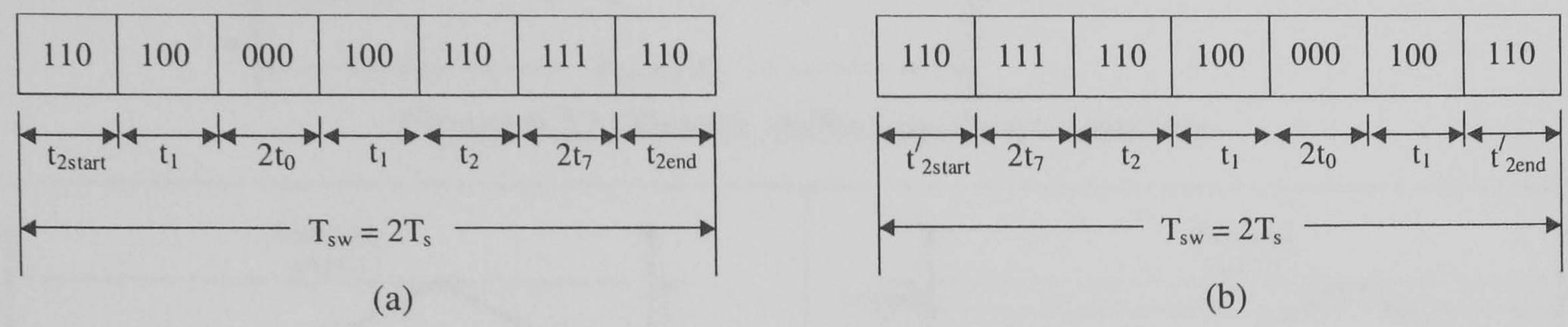


Figure 6.20. The sequence of states for the third and fourth group in case (2) for the five-level SVM
(a) the first group and (b) the second group

iii. Seven-level mapped phase shifted SVM

The seven-level cascaded type inverter is shown in figure (6.21) and as with three and five level SVM, this inverter can be divided into six groups. The main switches of these groups are shaded grey. These six groups can be treated as if they are six separate two-level inverters, controlled by the conventional two-level SVM but with six up-down counters each shifted by $T_{sw}/6$, as shown in figure (6.22).

The first and second groups are mapped as in three-level SVM. Mapping of the remain four groups involves three cases. Figure (6.23) indicates one switching cycle for each of theses groups, for the three different cases and Table 6.3 summarizes the conditions and sequences for each case.

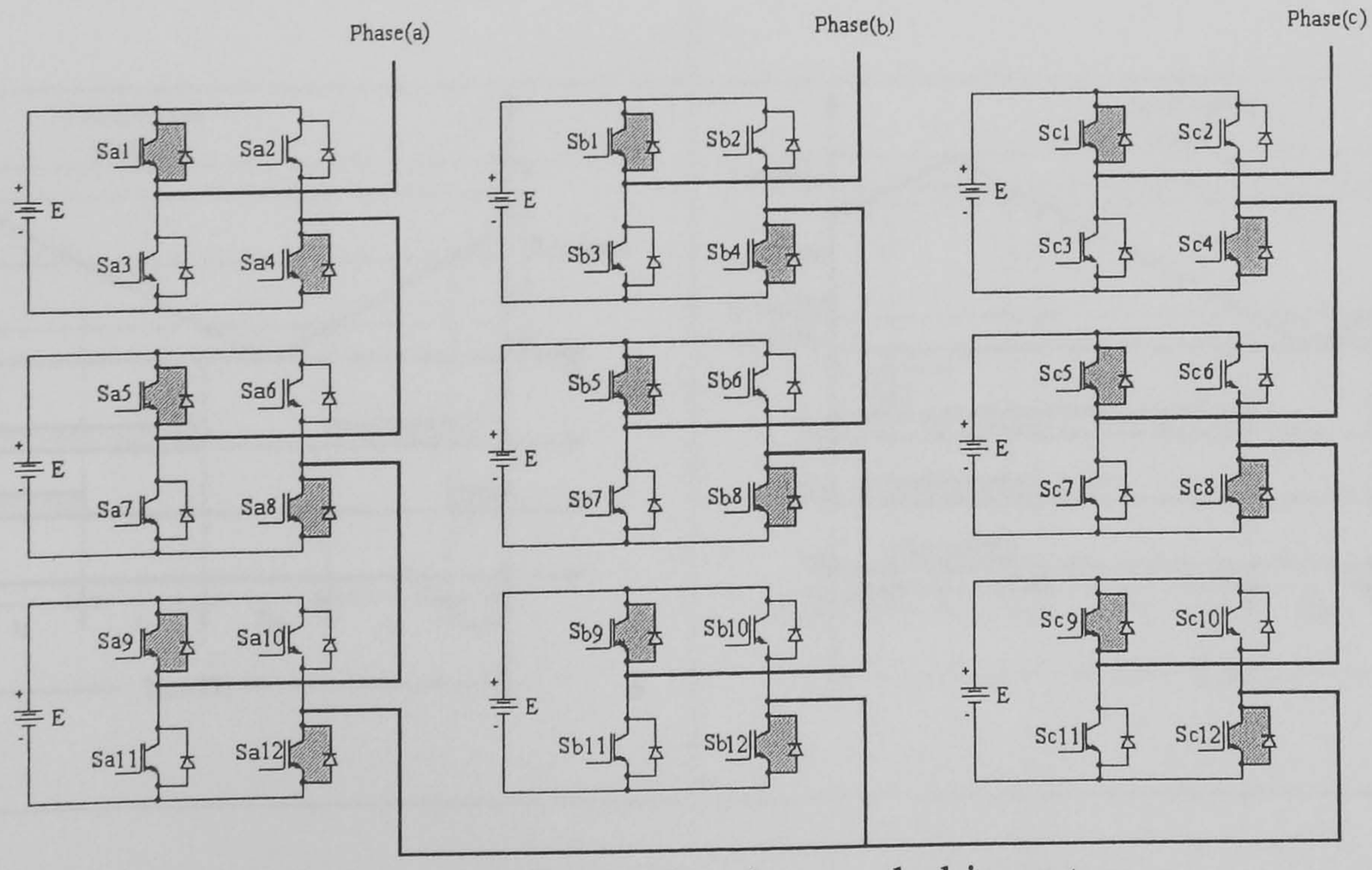


Figure 6.21. Seven-level cascaded inverter

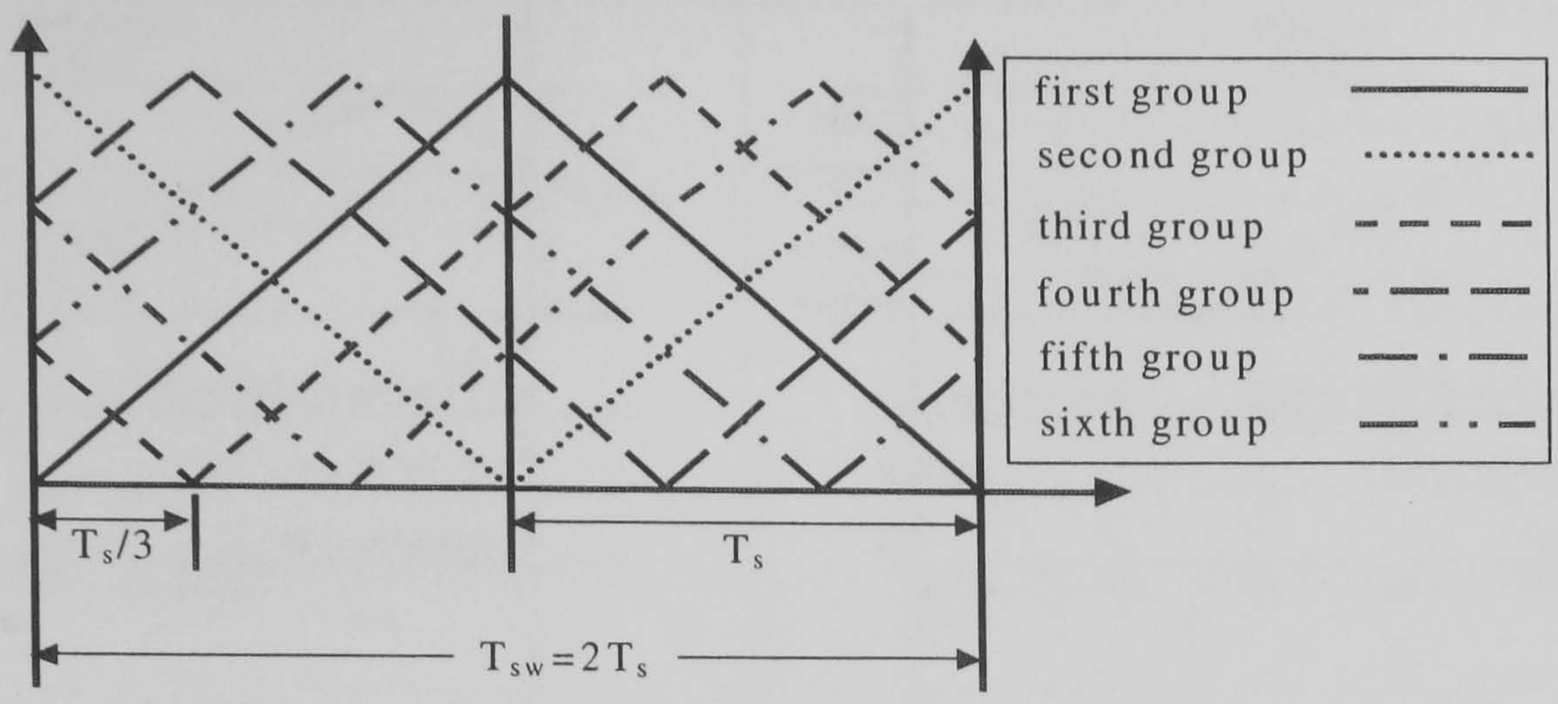
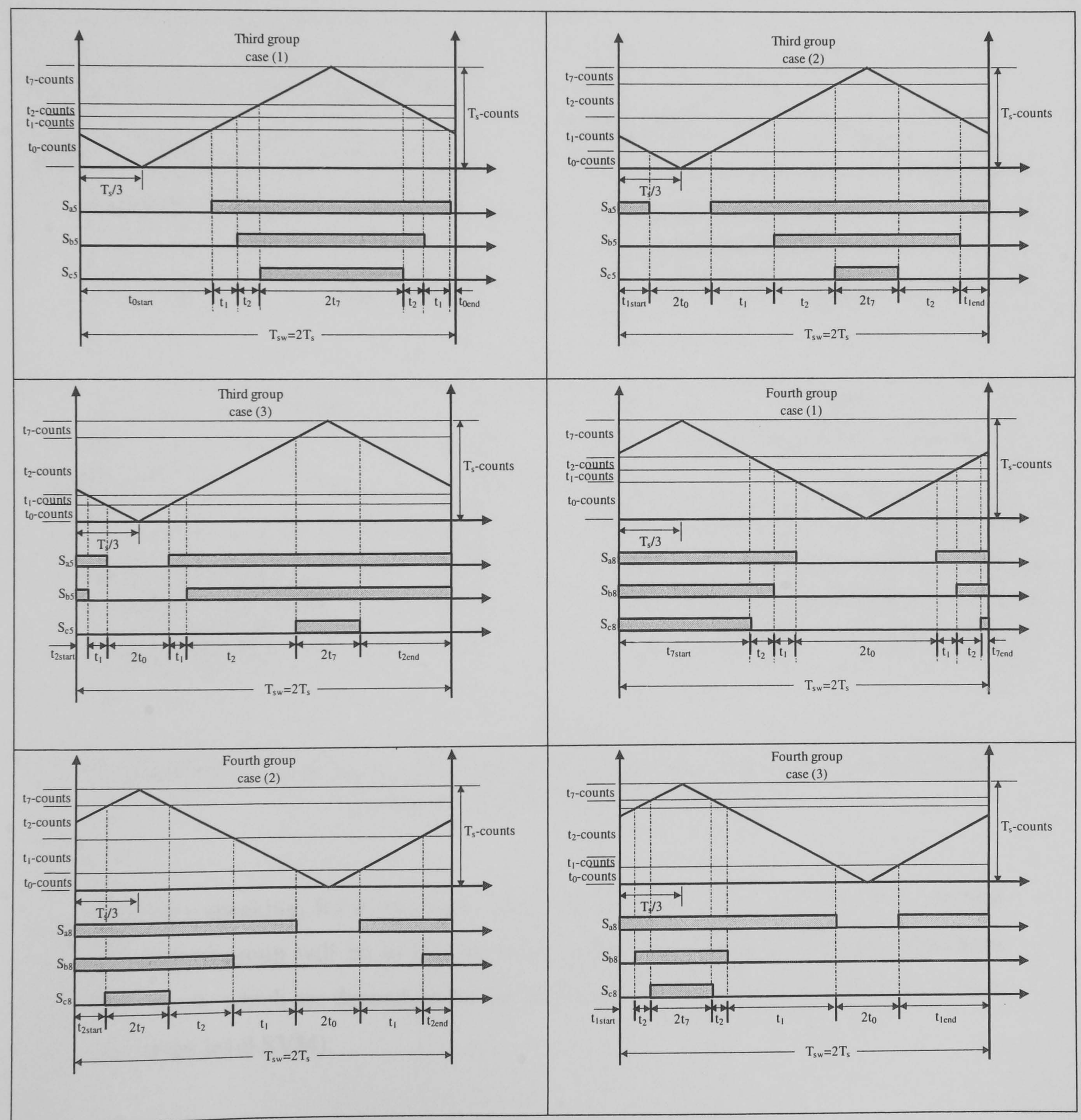


Figure 6.22. The six shifted up-down counters



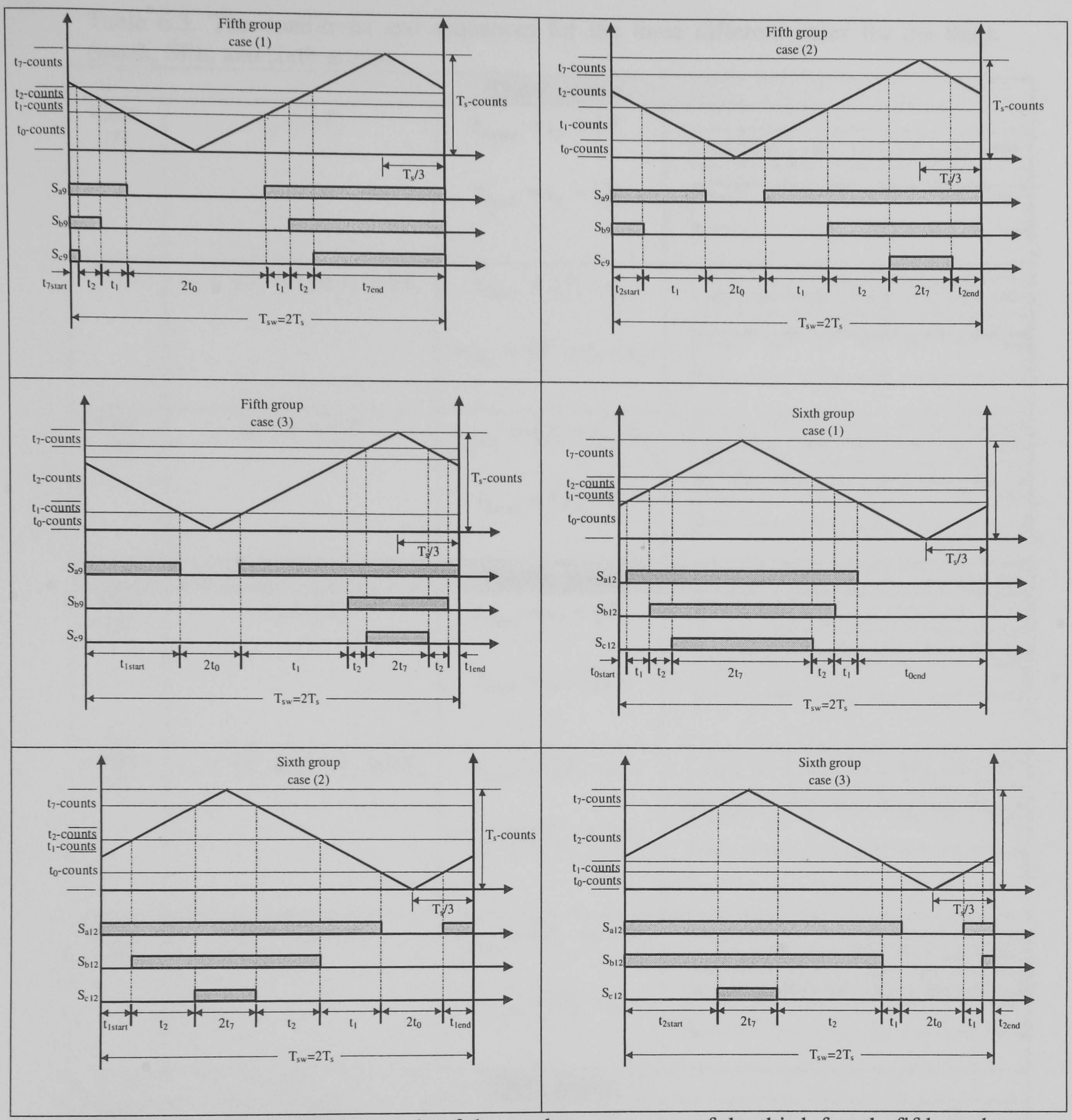
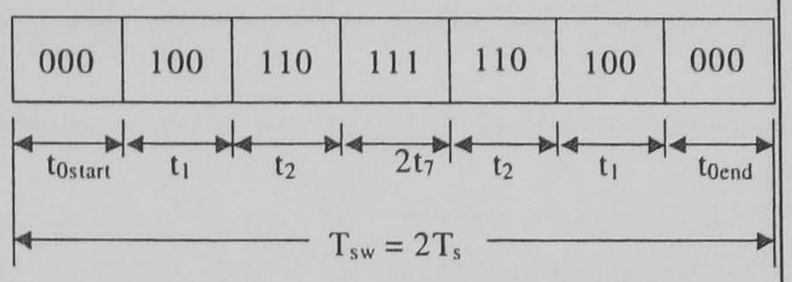
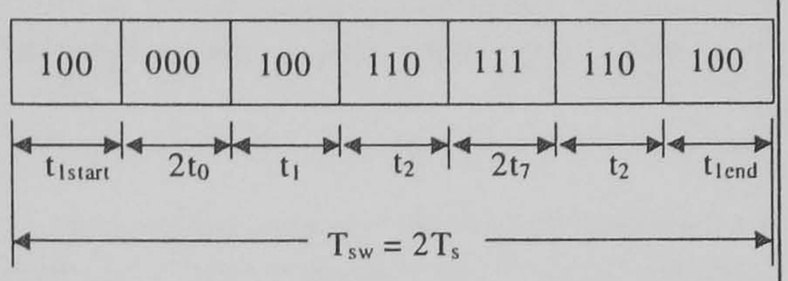
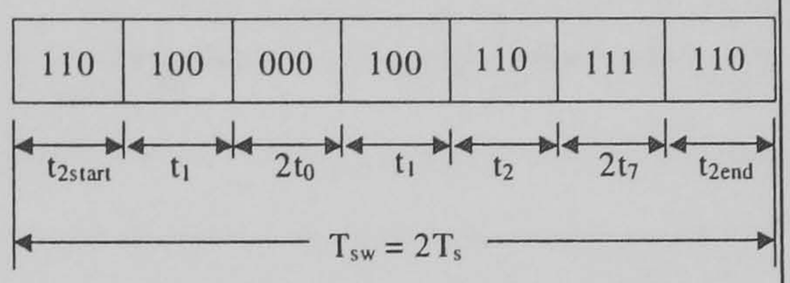
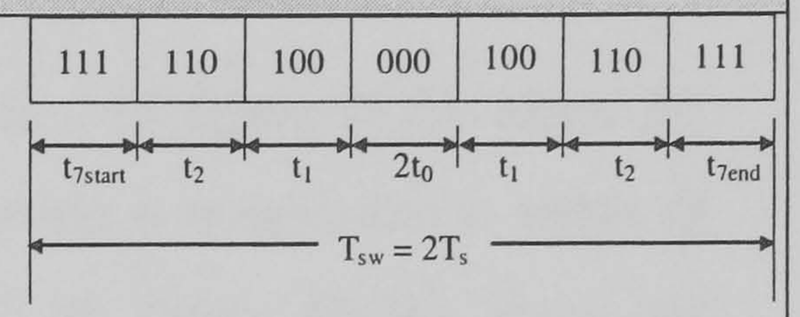
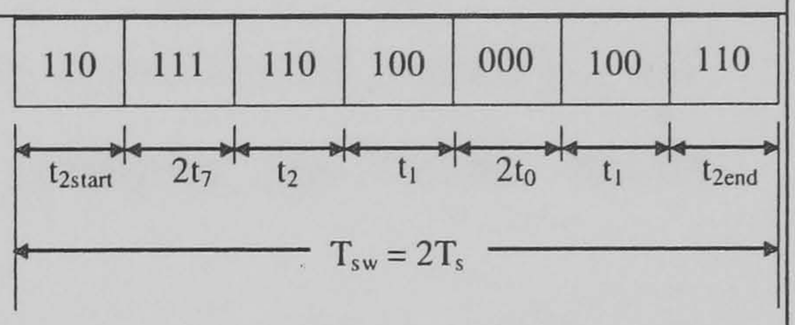
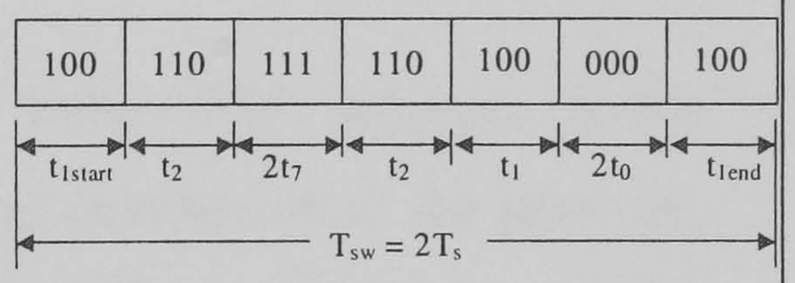
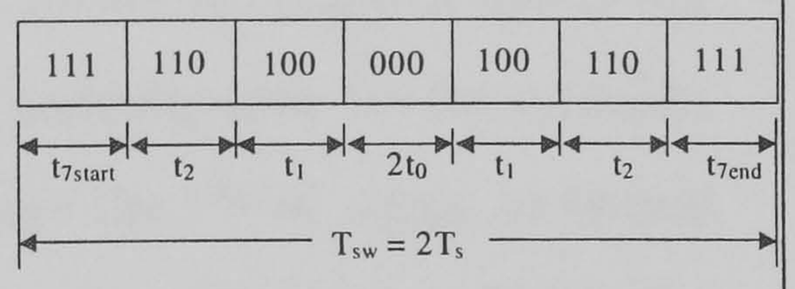
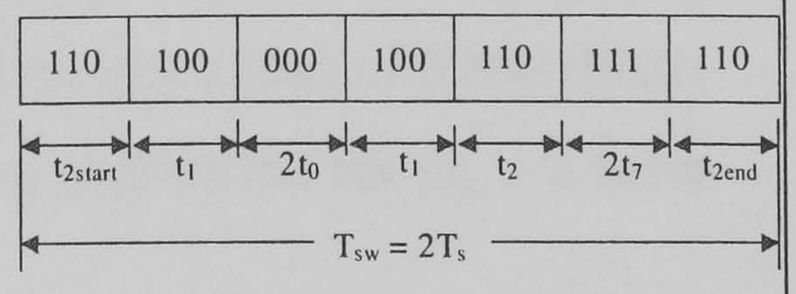
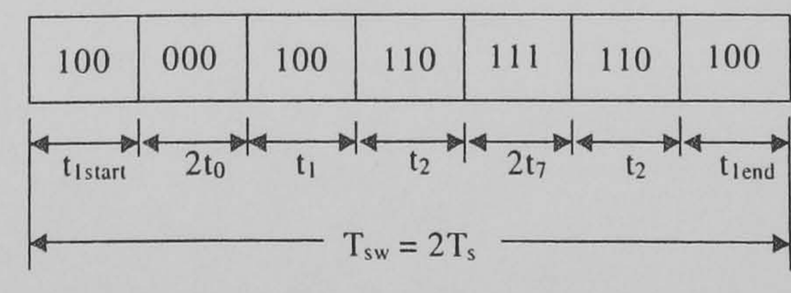
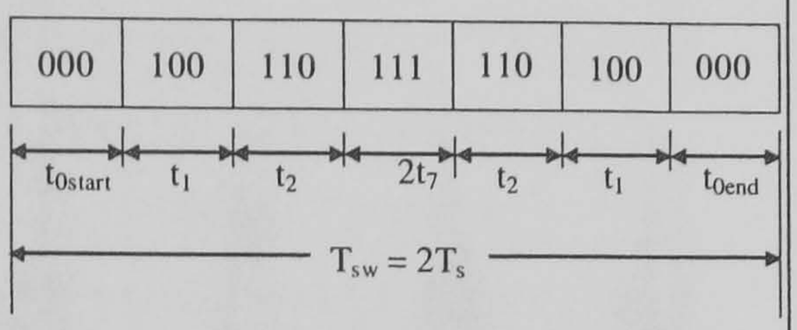
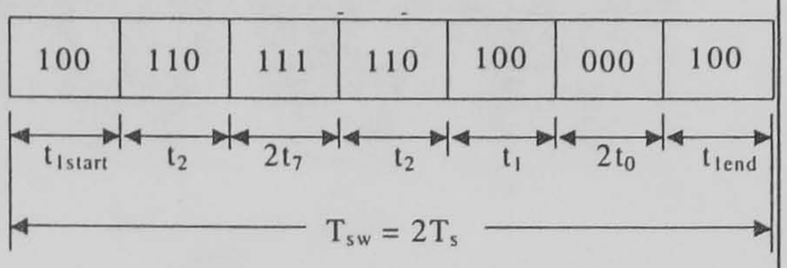
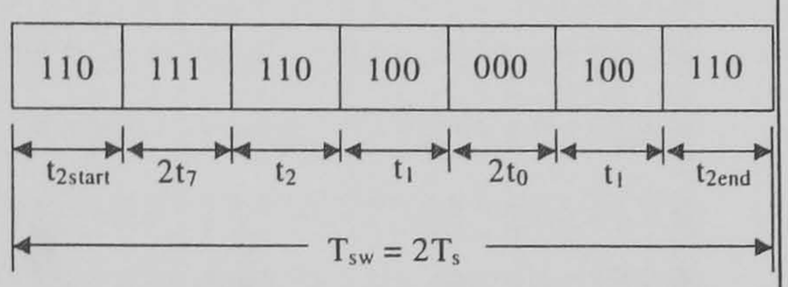


Figure 6.23. One switching cycle of the up-down counters of the third, fourth, fifth, and sixth groups for the three different cases

Generally speaking, for levels higher than seven, there will be *(m-1)* groups. The first and second group will be as in three-level SVM. The other *(m-3)* groups, each have three cases, which are dependent on the number of levels (as discussed with three, five, and seven level SVM).

Table 6.3. The conditions and sequences for the three different cases for the third, fourth, fifth, and sixth groups

Third group			
Case (1)	$t_0 \geq \frac{1}{3}T_s$	$t_{0start} = t_0 + \frac{1}{3}T_s$ $t_{0end} = t_0 - \frac{1}{3}T_s$	
Case(2)	$t_0 < \frac{1}{3}T_s \;\&\; t_0 + t_1 \geq \frac{1}{3}T_s$	$t_{1start} = \frac{1}{3}T_s - t_0$ $t_{1end} = \frac{2}{3}T_s - t_7 - t_2$	
Case (3)	$t_0 + t_1 < \frac{1}{3}T_s$	$t_{2start} = \frac{1}{3}T_s - t_0 - t_1$ $t_{2end} = \frac{2}{3}T_s - t_7$	
Fourth group			
Case (1)	$t_7 \geq \frac{1}{3}T_s$	$t_{7start} = t_7 + \frac{1}{3}T_s$ $t_{7end} = t_7 - \frac{1}{3}T_s$	
Case (2)	$t_7 < \frac{1}{3}T_s \;\&\; t_7 + t_2 \geq \frac{1}{3}T_s$	$t_{2start} = \frac{1}{3}T_s - t_7$ $t_{2end} = \frac{2}{3}T_s - t_0 - t_1$	
Case (3)	$t_7 + t_2 < \frac{1}{3}T_s$	$t_{1start} = \frac{1}{3}T_s - t_7 - t_2$ $t_{1end} = \frac{2}{3}T_s - t_0$	
Fifth group			
Case (1)	$t_7 \geq \frac{1}{3}T_s$	$t_{7start} = t_7 - \frac{1}{3}T_s$ $t_{7end} = t_7 + \frac{1}{3}T_s$	
Case (2)	$t_7 < \frac{1}{3}T_s \;\&\; t_7 + t_2 \geq \frac{1}{3}T_s$	$t_{2start} = \frac{2}{3}T_s - t_0 - t_1$ $t_{2end} = \frac{1}{3}T_s - t_7$	
Case (3)	$t_7 + t_2 < \frac{1}{3}T_s$	$t_{1start} = \frac{2}{3}T_s - t_0$ $t_{1end} = \frac{1}{3}T_s - t_7 - t_2$	

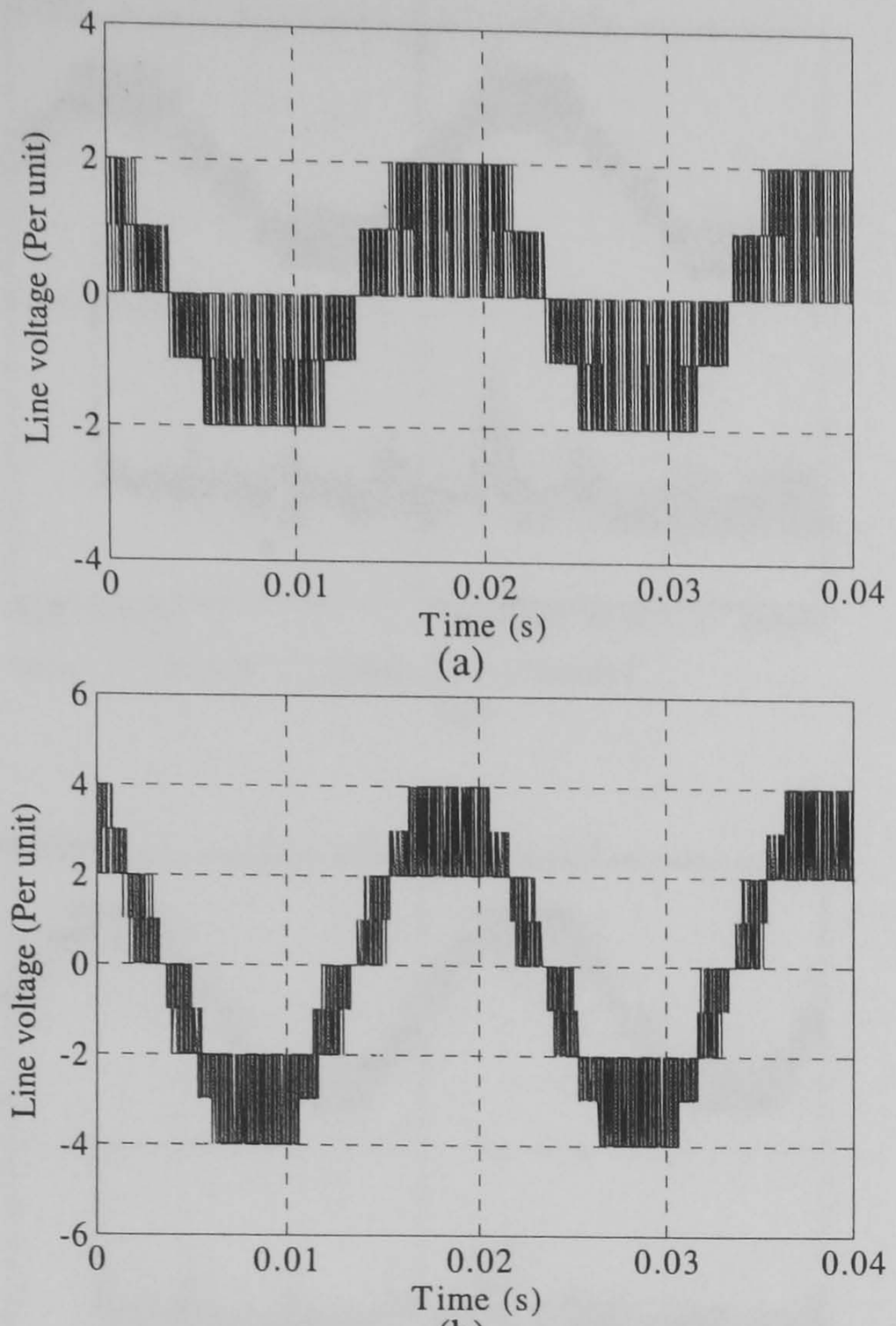
Sixth group			
Case (1)	$t_0 \geq \frac{1}{3}T_s$	$t_{0start} = t_0 - \frac{1}{3}T_s$ $t_{0end} = t_0 + \frac{1}{3}T_s$	
Case (2)	$t_0 < \frac{1}{3}T_s \;\&\; t_0 + t_1 \geq \frac{1}{3}T_s$	$t_{1start} = \frac{2}{3}T_s - t_7 - t_2$ $t_{1end} = \frac{1}{3}T_s - t_0$	
Case (3)	$t_0 + t_1 < \frac{1}{3}T_s$	$t_{2start} = \frac{2}{3}T_s - t_7$ $t_{2end} = \frac{1}{3}T_s - t_0 - t_1$	

6.3.2 Simulation

MPS-SVM is simulated using Matlab/Simulink. Parts a to c of figure (6.24) show the line voltage for MPS-SVM with three, five, and seven levels at a modulation index of 0.9 and a 3 kHz switching frequency. Parts d to f of figure (6.24) show the corresponding power density spectrum. The harmonics are concentrated at $(m\text{-}1)f_{sw}$ and its multiples (at 6 kHz and its multiples, 12 kHz and its multiples, and 18 kHz and its multiples for three, five, and seven levels respectively).

6.3.3 Practical results

The proposed MPS-SVM algorithm is implemented using DSP software (Code Composer (see Appendix C.2)) which calculates the timing distribution of the states (t_0, t_1, t_2, and t_7) and the corresponding states for the AED106. The execution time of the control algorithm for MPS-SVM is 26 μs while it is 44 μs for generalized multilevel SVM (and 18 μs for PS-SVM). PWM generation and the underlap time for the switches (640 ns) are implemented in Xilinx. Figure (6.25) indicates the PWM signal to switch S_{a1} and its spectrum. Parts a and b of figure (6.26) show the output line voltage, the phase current, and spectrums for MPS-SVM at a modulation index (m_a) of 0.866 (linear modulation). Parts c and d of figure (6.26) show the same outputs but for $m_a = 2$ (over modulation).



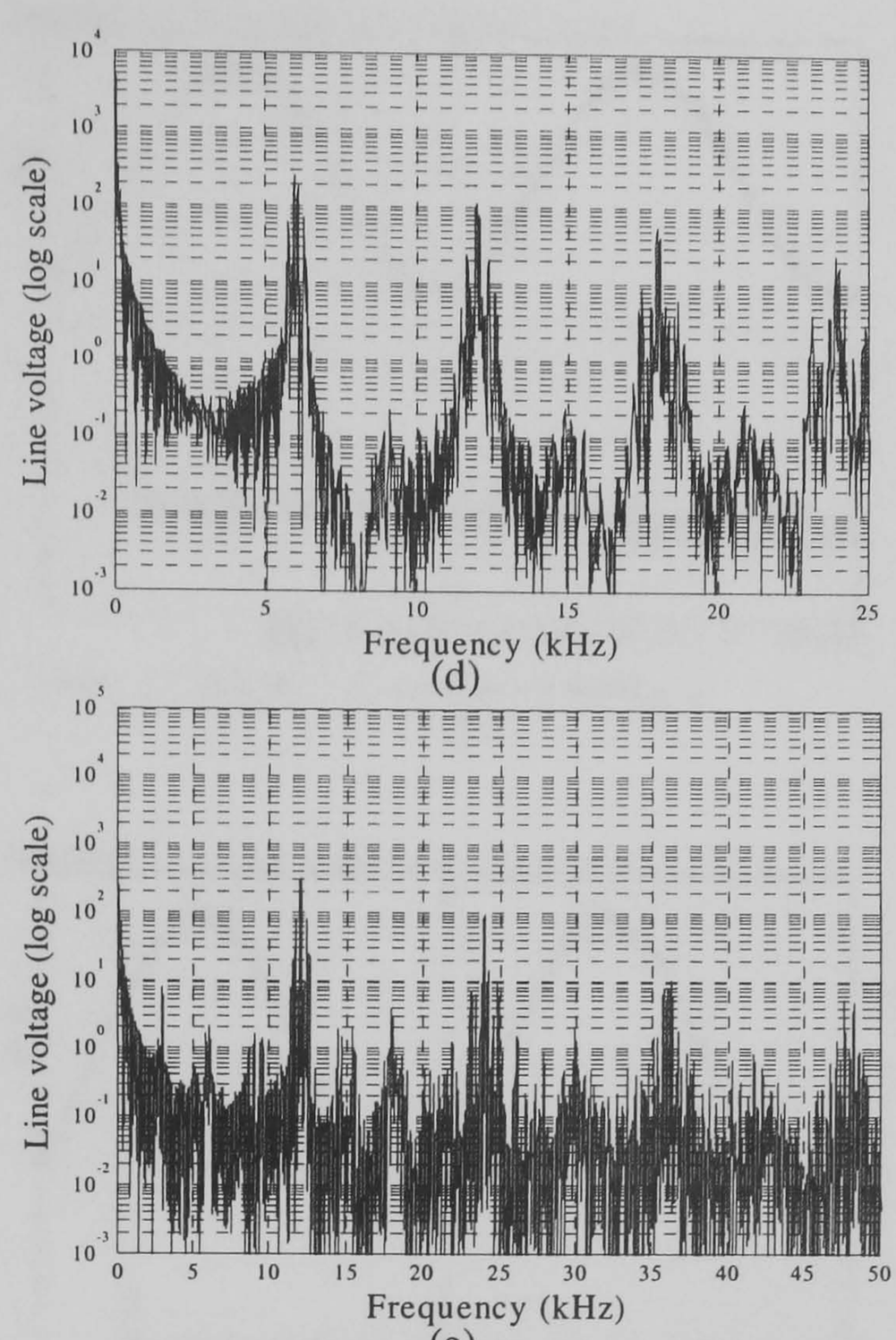


Figure 6.24. Simulated line voltage using MPS-SVM for (a) three, (b) five, and (c) seven levels and their respective power density spectrum (d), (e), and (f) at $m_a = 0.9$, $f_{sw} = 3$ kHz

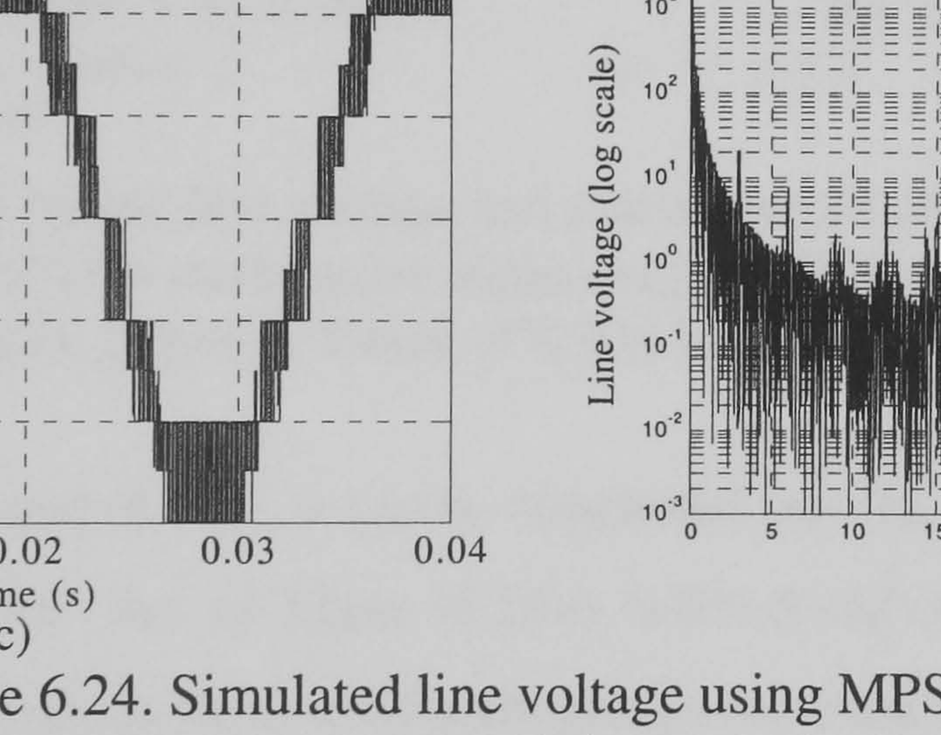
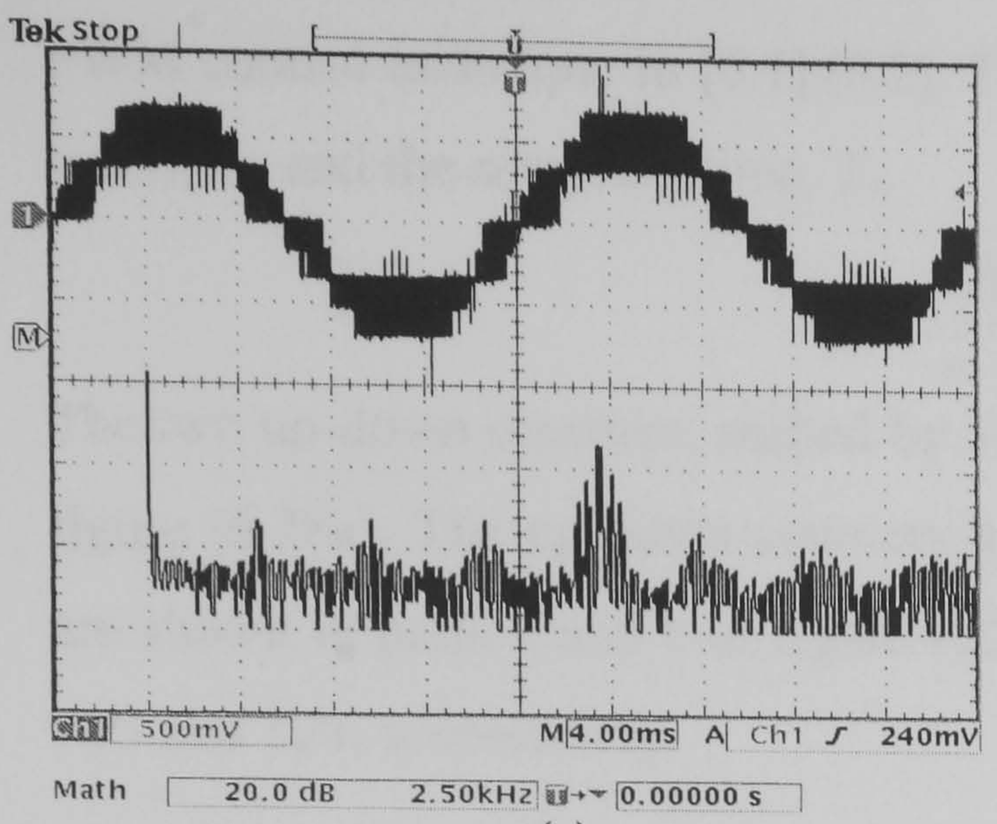
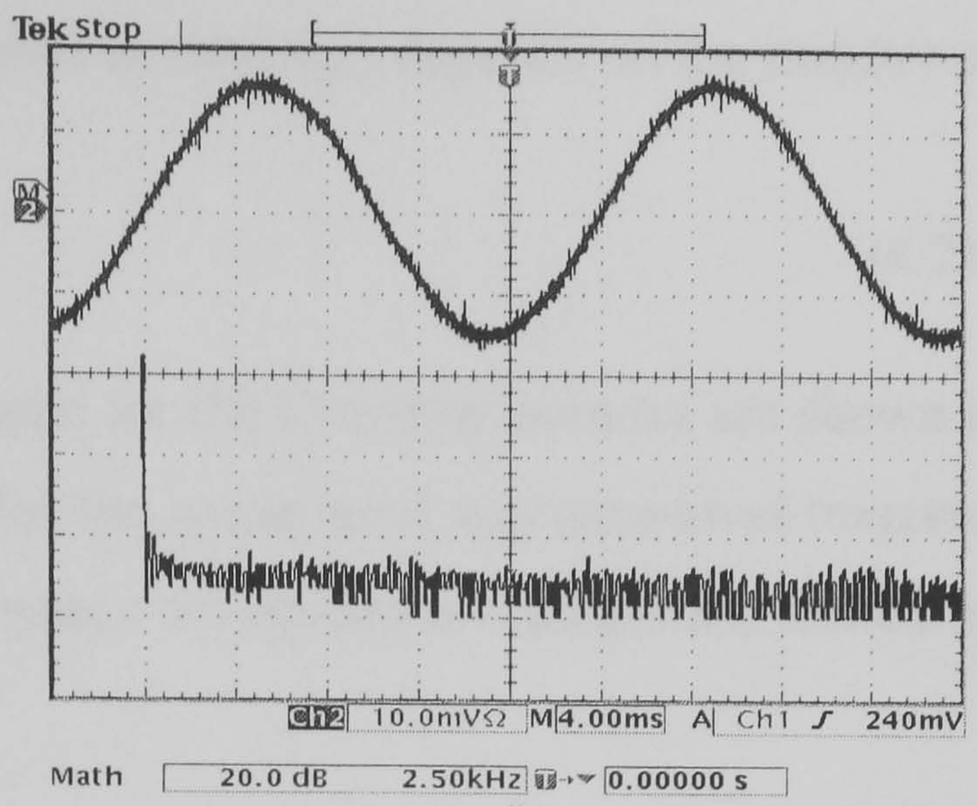


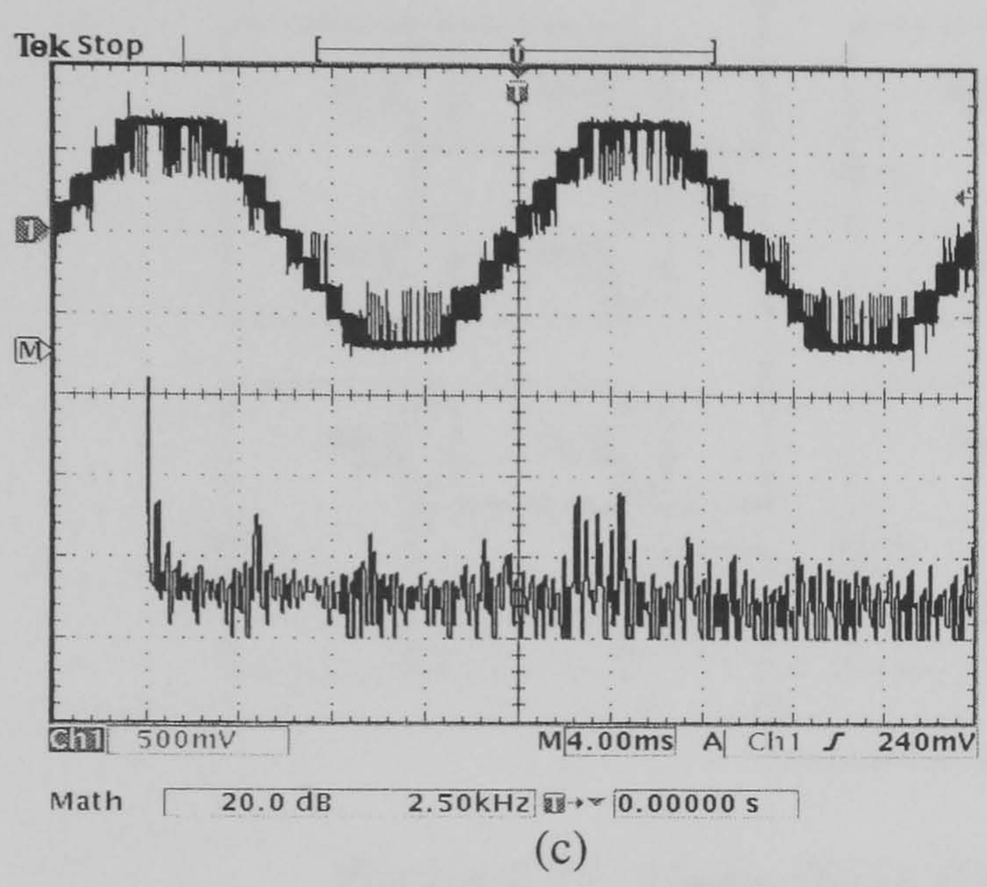
Figure 6.25. The PWM signal to the gate drive of S_{a1} and its spectrum



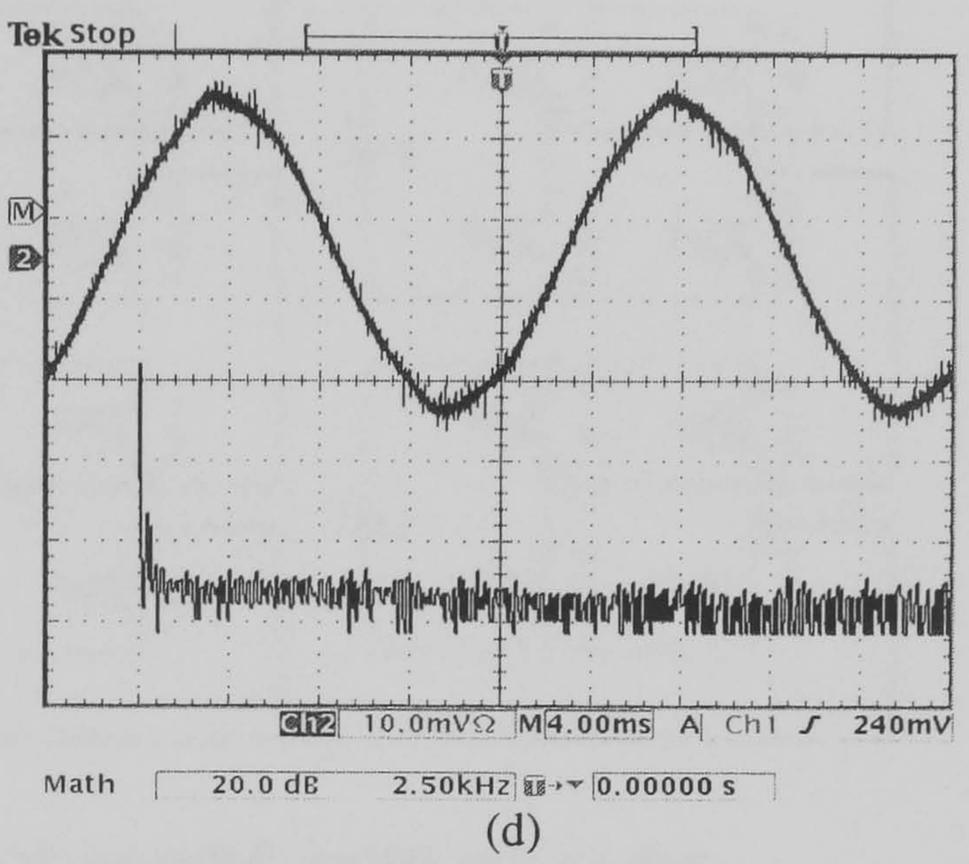
(a)



(b)



(c)



(d)

Figure 6.26. Practical output line voltage and phase current and spectrums (semi log) for MPS-SVM (a) and (b) for modulation index (m_a) = 0.866, (c) and (d) for modulation index (m_a) = 2 (power factor of 0.938 lag) (100V/div & 2A/div)

From figures (6.10a) and (6.26a), it can be concluded that the spectrum of figure (6.10a) (PS-SVM) is better than that of figure (6.26a) (MPS-SVM) because in MPS-SVM the starting and end times of the third and fourth groups are truncated.

6.4 Hybrid SVM

A new SVM approach is proposed to reduce DSP implementation complexity for levels higher than three. The multilevel inverter is subdivided into groups of three-level inverters and the three-level space vector modulation is applied to each group.

6.4.1 Hybrid (H-SVM) implementation

The five-level cascaded multilevel inverter shown in figure (6.27) is subdivided into two three-level inverters. Three-level SVM is used for each group but the two up-down counters used for each group are shifted in time, as in the phase shift carrier based

PWM control technique in [6.1],[6.2]. This shift in time (t_{ps}) depends on the number of levels, m, and the sampling time, T_s,

$$t_{ps} = \frac{2T_s}{m-1} \tag{6.21}$$

The two up-down counters, shifted by $T_s/2$, used for the five-level inverter are shown in figure (6.28a). The up-down counters used for the seven-level and nine-level inverters are shown in parts b and c of figure (6.28), where the up-down counters are shifted by $T_s/3$ and $T_s/4$, respectively.

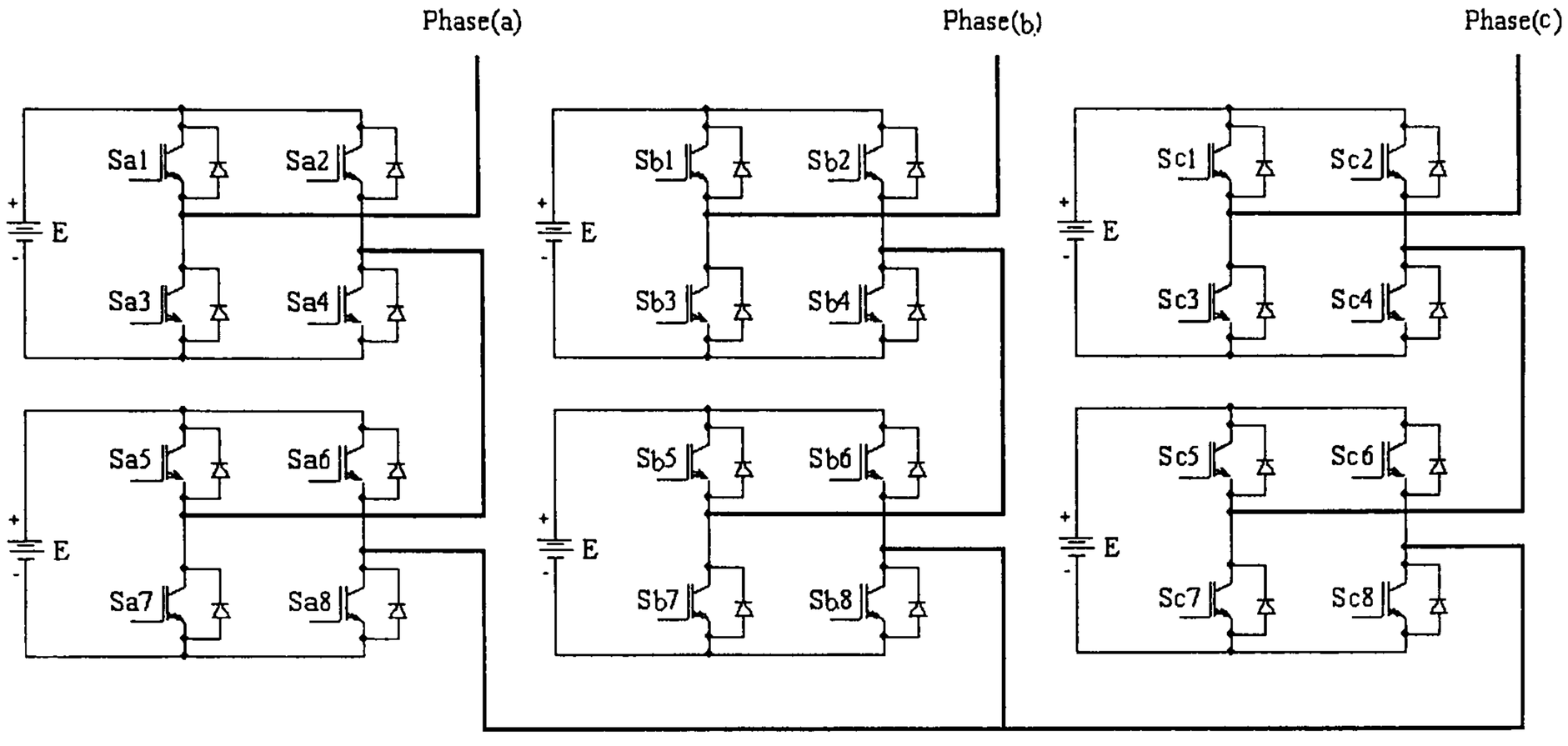


Figure 6.27. Three-phase five-level cascaded multilevel inverter.

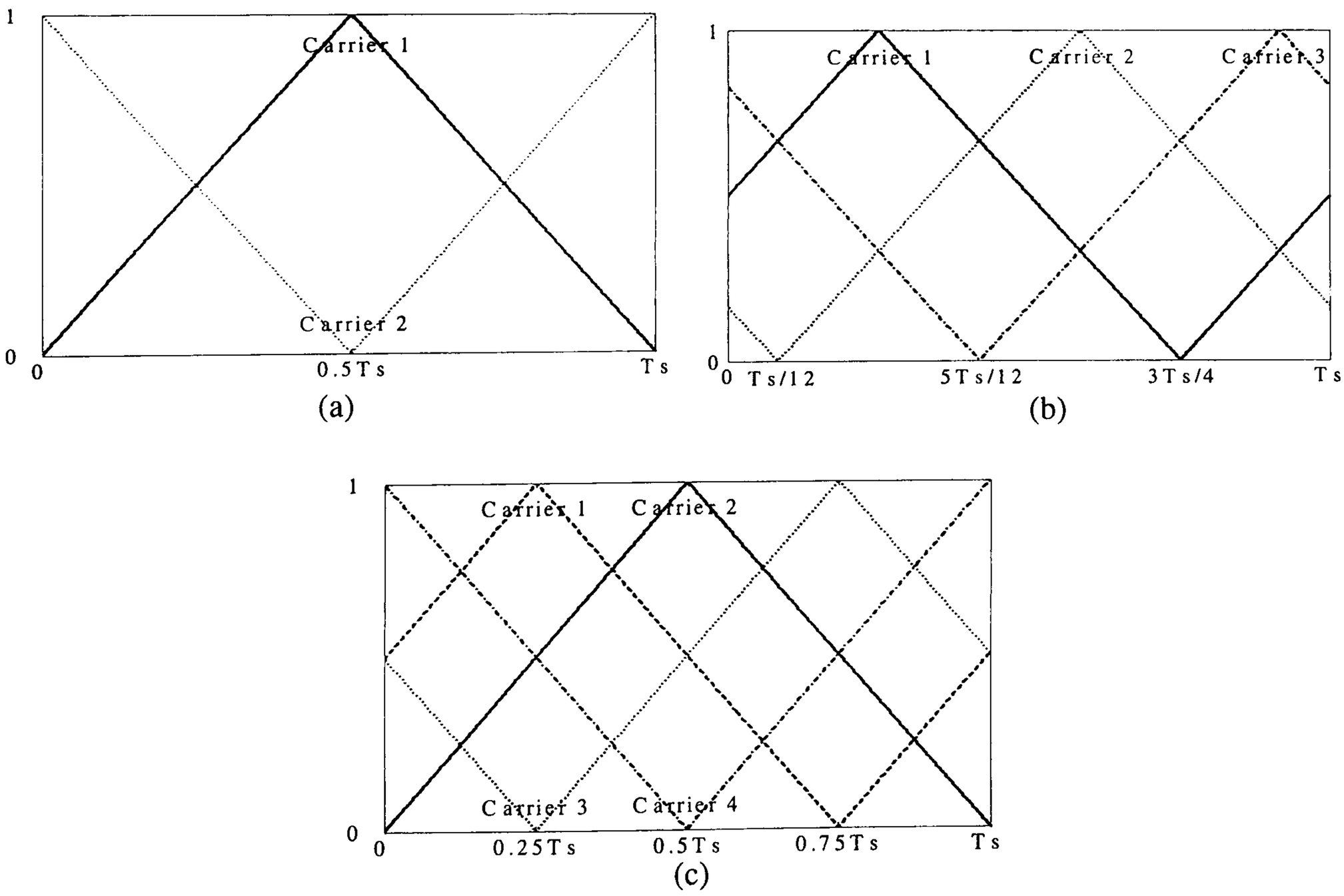


Figure 6.28. The up-down counters used for:
(a) five-level, (b) seven-level, and (b) nine-level inverter

The modulation index for *m*-levels is defined as

$$m_a = \frac{V_{ref}^*}{(m-1)E\cos\left(\frac{\pi}{6}\right)} \tag{6.22}$$

With this modulation method, the switching losses are increased by *(m-1)/2* times that of normal multilevel SVM. But the harmonics are shifted towards $(m-1)f_s/2$ instead of f_s as with normal multilevel SVM, where $f_s = 1/T_s$. But the complexity of the states in normal multilevel SVM is avoided with H-SVM.

6.4.2 Simulation

H-SVM is simulated using Matlab/Simulink. Parts a to c of figure (6.29) show the line voltage for H-SVM with five, seven, and nine levels at a modulation index of 0.9 and a 3 kHz sampling frequency. Parts d to f of figure (6.29) show the corresponding power density spectrum The harmonics are concentrated at $(m-1)f_s/2$ and its multiples (at 6 kHz and its multiples, 9 kHz and its multiples, 12 kHz and its multiples for five, seven, and nine levels respectively).

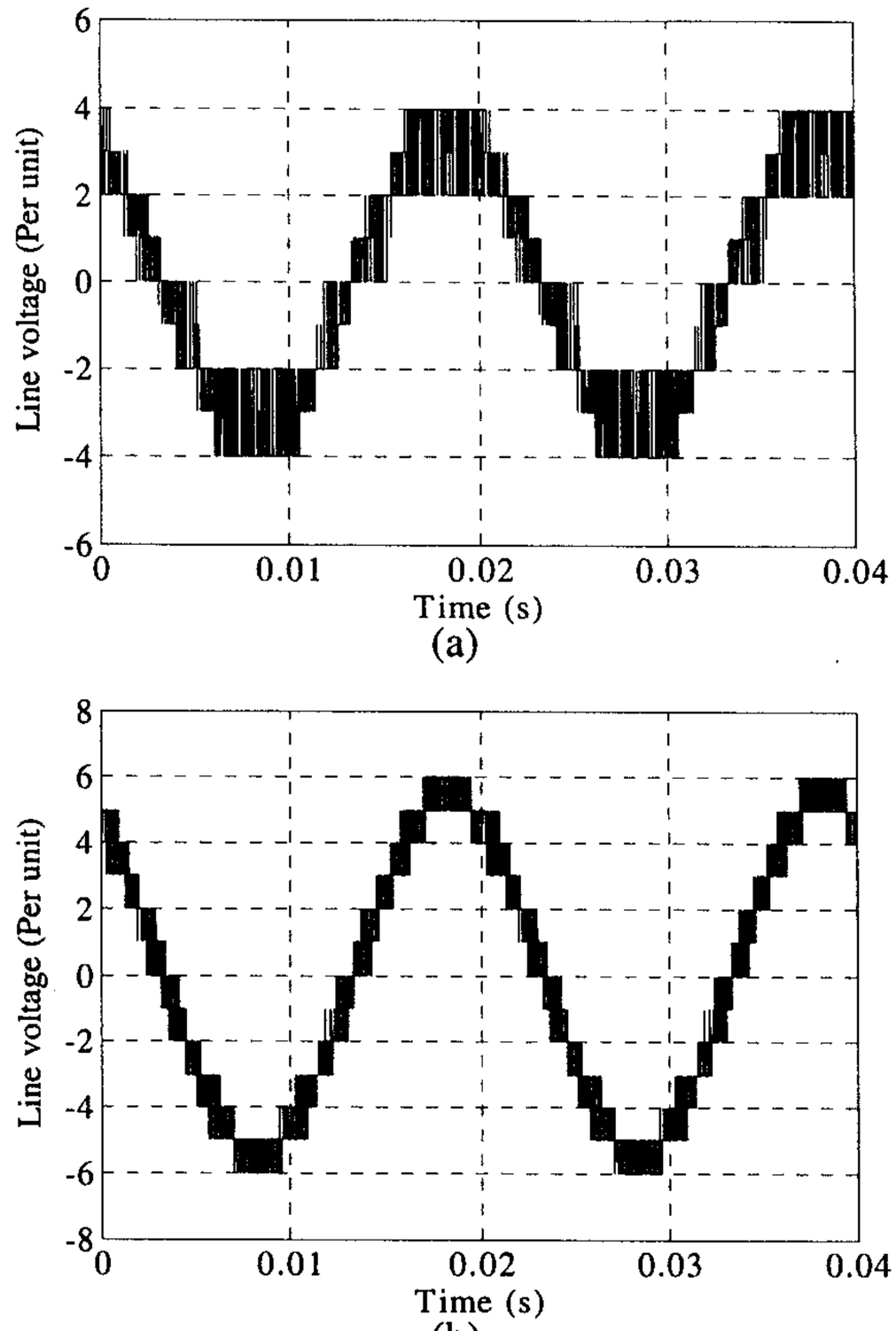
Comparing the spectra of H-SVM (parts e to h of figure (6.29)) with normal multilevel SVM (parts e to h of figure (6.6)), the harmonic magnitudes of normal multilevel SVM are smaller relative to the corresponding H-SVM harmonics.

Parts a to d of figure (6.30) allow comparison of the line voltage total harmonic distortion (THD) of H-SVM and normal multilevel SVM. From these figures, it is concluded that the THD of normal multilevel SVM is better than that of H-SVM for all modulation indices.

Parts a to d of figure (6.31) compare the line voltage distortion factor (DF) of H-SVM, normal multilevel SVM, and normal multilevel SVM with the same effective switching loss as H-SVM ($2f_s$, $3f_s$, and $4f_s$ for five, seven, and nine levels respectively).

From these figures, for the same f_s, it is concluded that the DF of H-SVM is better than normal multilevel SVM, due to the harmonic component being shifted to $(m-1)f_s/2$ compared to f_s in normal multilevel SVM (except for five-levels, where the shift in harmonic components for H-SVM cannot overcome the harmonic magnitude increase which worsens the DF). When both techniques are normalized using the same effective switching frequency, the DF curves of H-SVM converge to those of normal multilevel SVM as the number of levels increases, as shown in parts a to d of figure (6.31).

Figure (6.32) indicates the line voltage fundamental component of H-SVM and normal multilevel SVM. It is concluded that the performance with both techniques is the same.



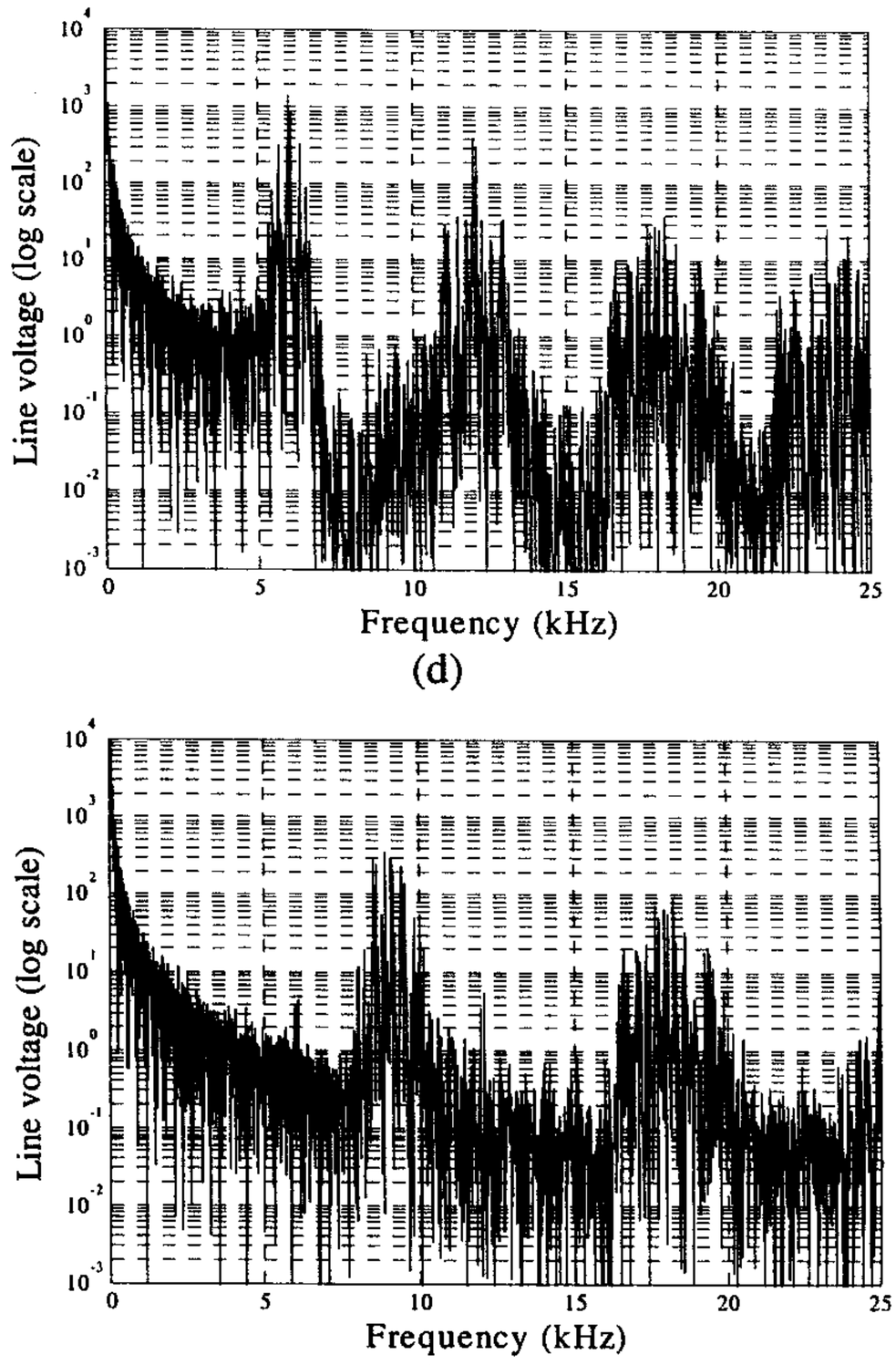
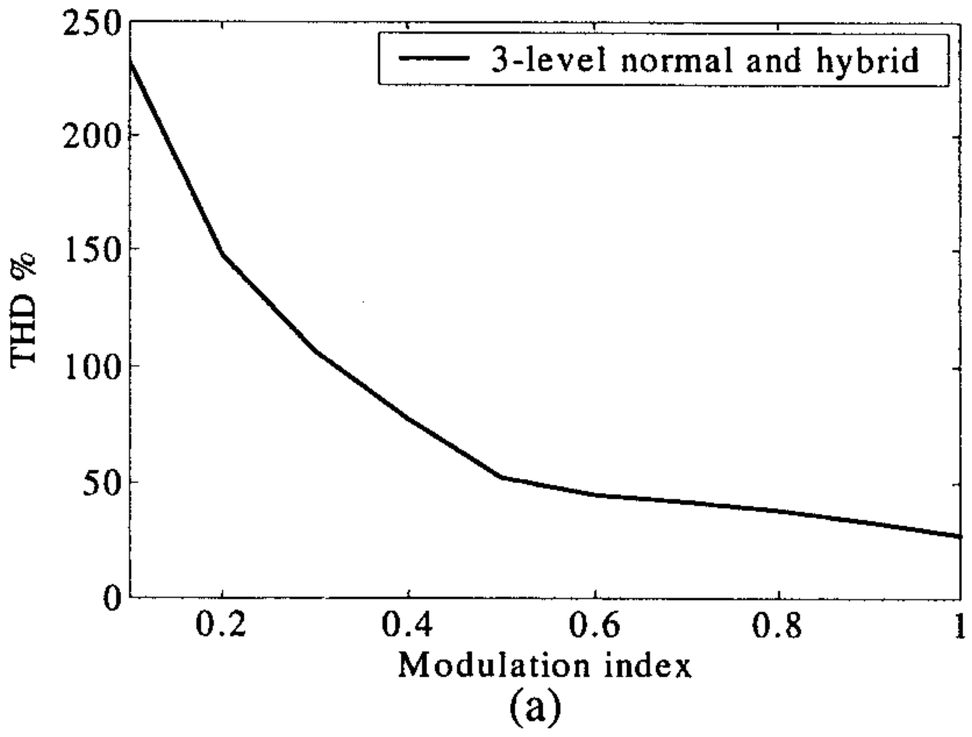
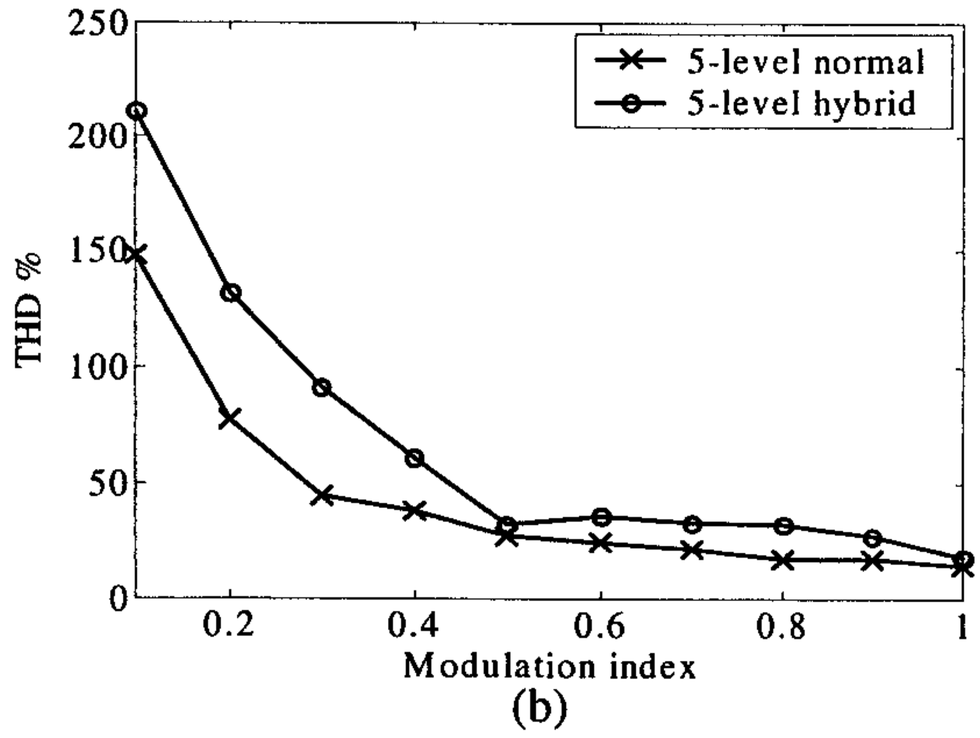


Figure 6.29. Simulated line voltage using H-SVM for:
(a) five, (b) seven, and (c) nine levels and their corresponding power density spectrum (d), (e), and (f) at $m_a = 0.9$, $f_s = 3$ kHz





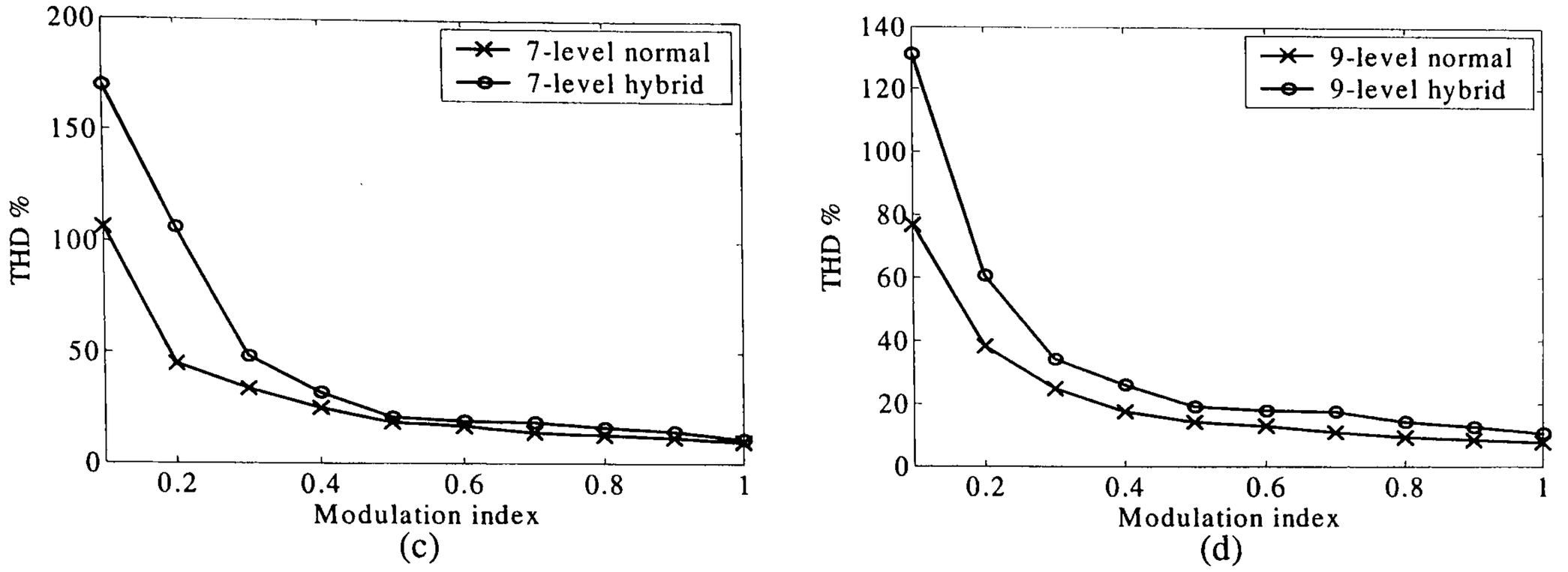


Figure 6.30. The line voltage THD of H-SVM and normal multilevel SVM for: (a) three, (b) five, (c) seven, and (d) nine levels

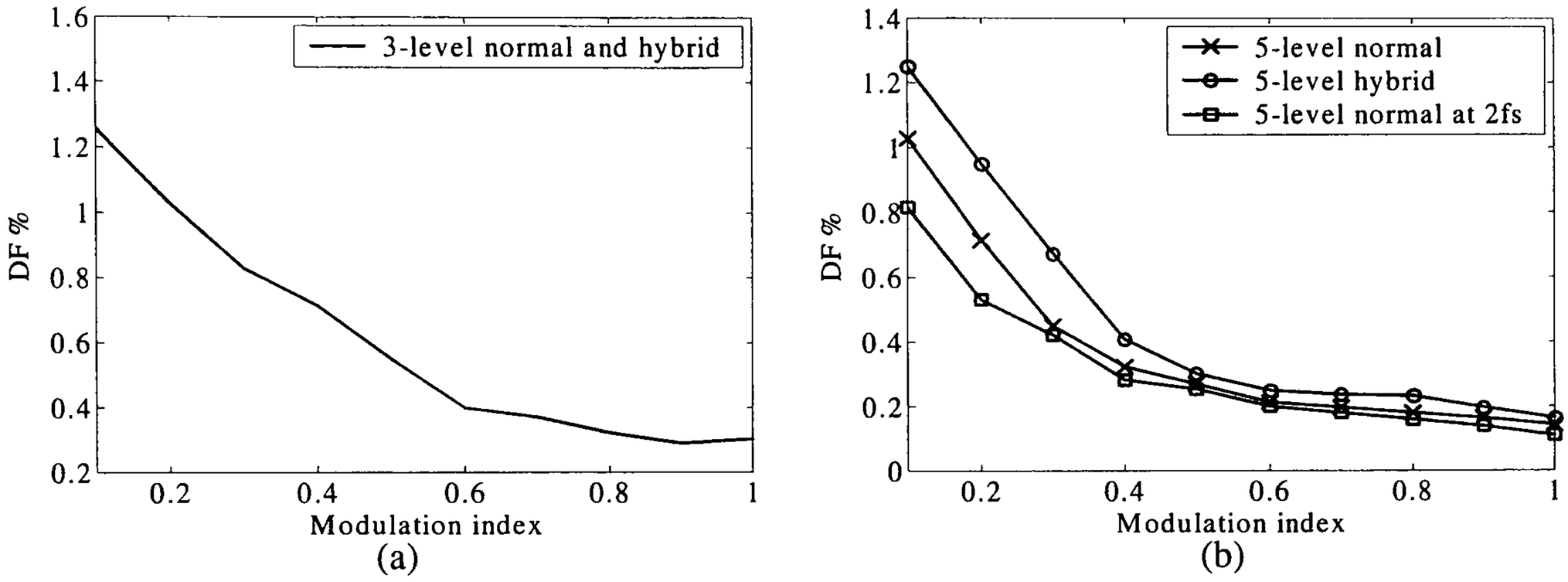


Figure 6.31. The line voltage DF of H-SVM and normal multilevel SVM for: (a) three, (b) five, (c) seven, and (d) nine levels

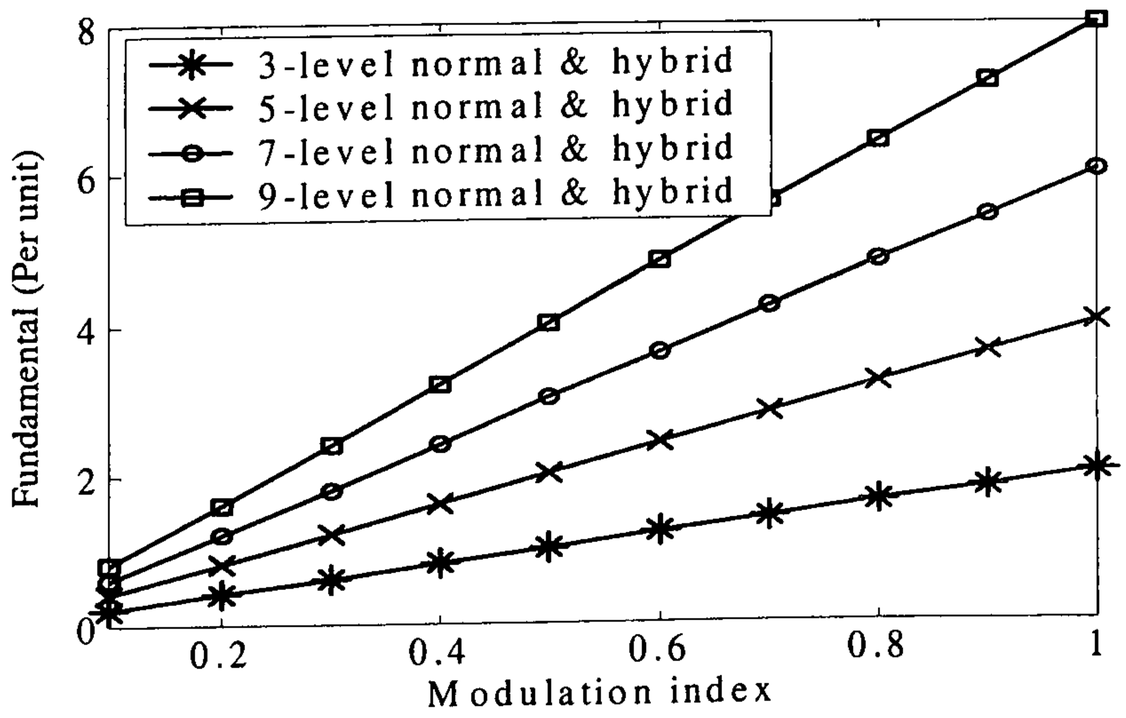


Figure 6.32. Line voltage fundamental component of H-SVM and normal multilevel SVM

6.4.3 Practical results

The execution time of the DSP program is 20 μs, independent of the number of levels (see Appendix C.3). To obtain the required shifted up-down counters, presettable up-down counters are configured in Xilinx. Parts a and b of figure (6.33) show the output line voltage, the phase current, and spectra for H-SVM at a modulation index (m_a) of 0.866. Parts c and d of figure (6.33) show the same outputs but for $m_a = 2$. The low order harmonics in the current spectrum in figure (6.33d) are minimized with the proposed over modulation technique. The simulation results (harmonic position and switching frequency) comparing normal multilevel SVM and H-SVM are validated by the practical results in figure (6.33). Table 6.4 summarizes the characteristics of H-SVM and normal multilevel SVM.

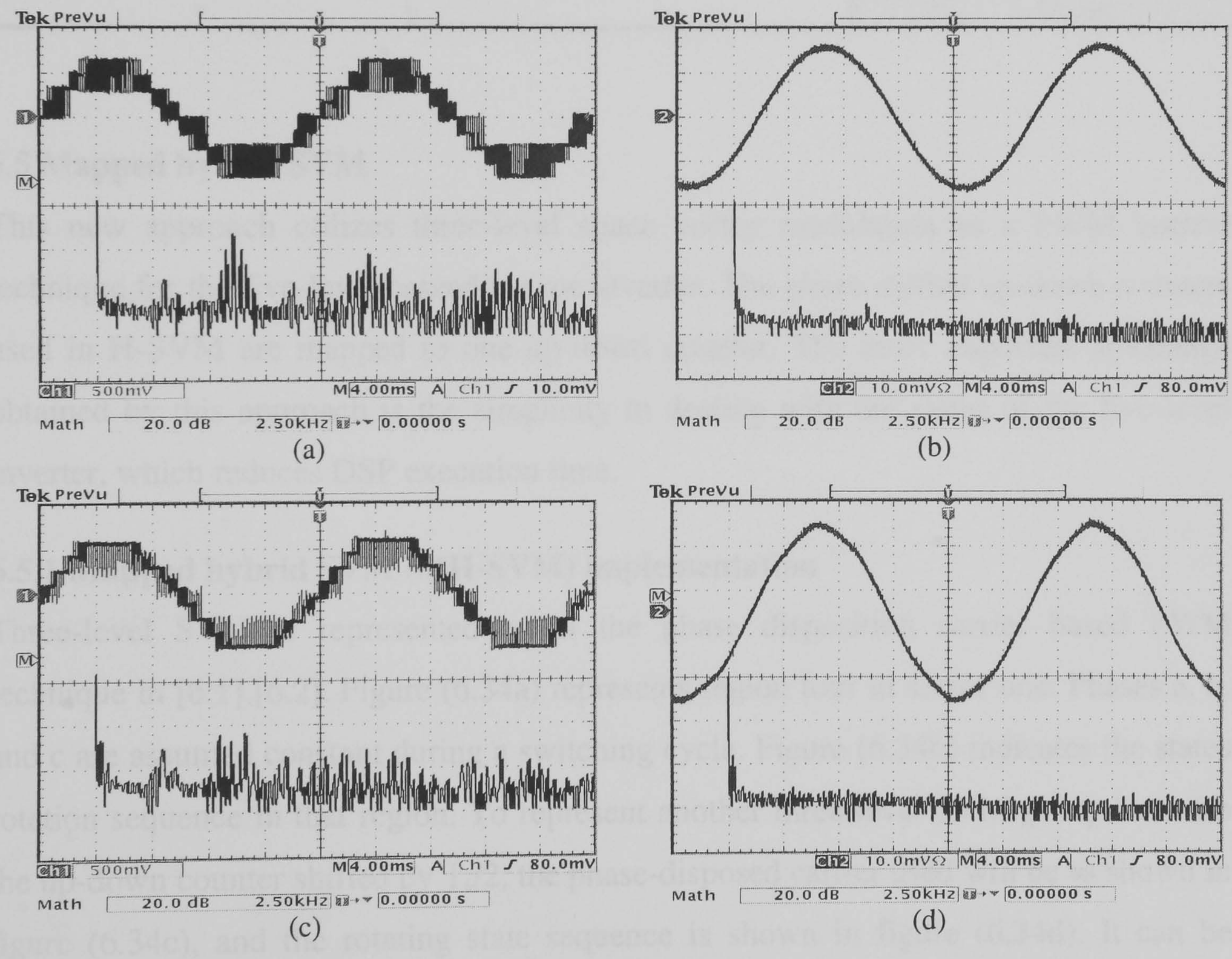


Figure 6.33. Practical output line voltage and phase current and spectrums (semi log) for H-SVM (a) and (b) for modulation index (m_a) = 0.866 (c) and (d) for modulation index (m_a) = 2 (power factor of 0.938 lag) (100V/div & 2A/div)

Table 6.4. Comparison between the H-SVM and the normal multilevel SVM.

	Hybrid SVM (H-SVM)	Normal multilevel SVM
Counter	$(m-1)/2$ counters shifted from each other by $2T_s/(m-1)$	Single counter
Total number of switchings per fundamental cycle	Higher, $((m-1)/2$ times that of normal multilevel SVM)	Lower
Line voltage THD	Worse	Better
Line voltage DF	Better	Worse
Harmonic spectrum	Shifted to $(m-1)f_s/2$ and its multiples	Shifted to f_s and its multiples
Execution time	20 µs	44 µs
Redundant sequence of paths	For three level only	Yes
Complexity	The three level SVM	More complex
dv/dt	A transition of more than one level may be presented in the line voltage	Lower
States	The 27-states of the three level SVM are used	More complex (m^3 states for m-levels)
Line voltage fundamental	The same	
Number of levels	Used for odd number of levels	Used for odd and even number of levels

6.5 Mapped hybrid SVM

This new approach utilizes three-level space vector modulation as a PWM control technique for the five-level cascaded type inverter. The phase-shifted up-down counters used in H-SVM are mapped to one up-down counter. The most important advantage obtained by this approach is the simplicity in dealing with the states of the five-level inverter, which reduces DSP execution time.

6.5.1 Mapped hybrid SVM (MH-SVM) implementation

Three-level SVM is represented as in the phase disposition carrier based PWM technique in [6.1],[6.2]. Figure (6.34a) represents region four in sector one. Phases a, b, and c are assumed constant during a switching cycle. Figure (6.34b) indicates the states rotation sequence in that region. To represent another three-level SVM group but with the up-down counter shifted by $T_s/2$, the phase-disposed carrier used will be as shown in figure (6.34c), and the rotating state sequence is shown in figure (6.34d). It can be concluded that the state sequence in figure (6.34b) is the reverse of figure (6.34d). So to obtain the same five-level H-SVM output, the three-level SVM is applied twice but with one sequence reversed.

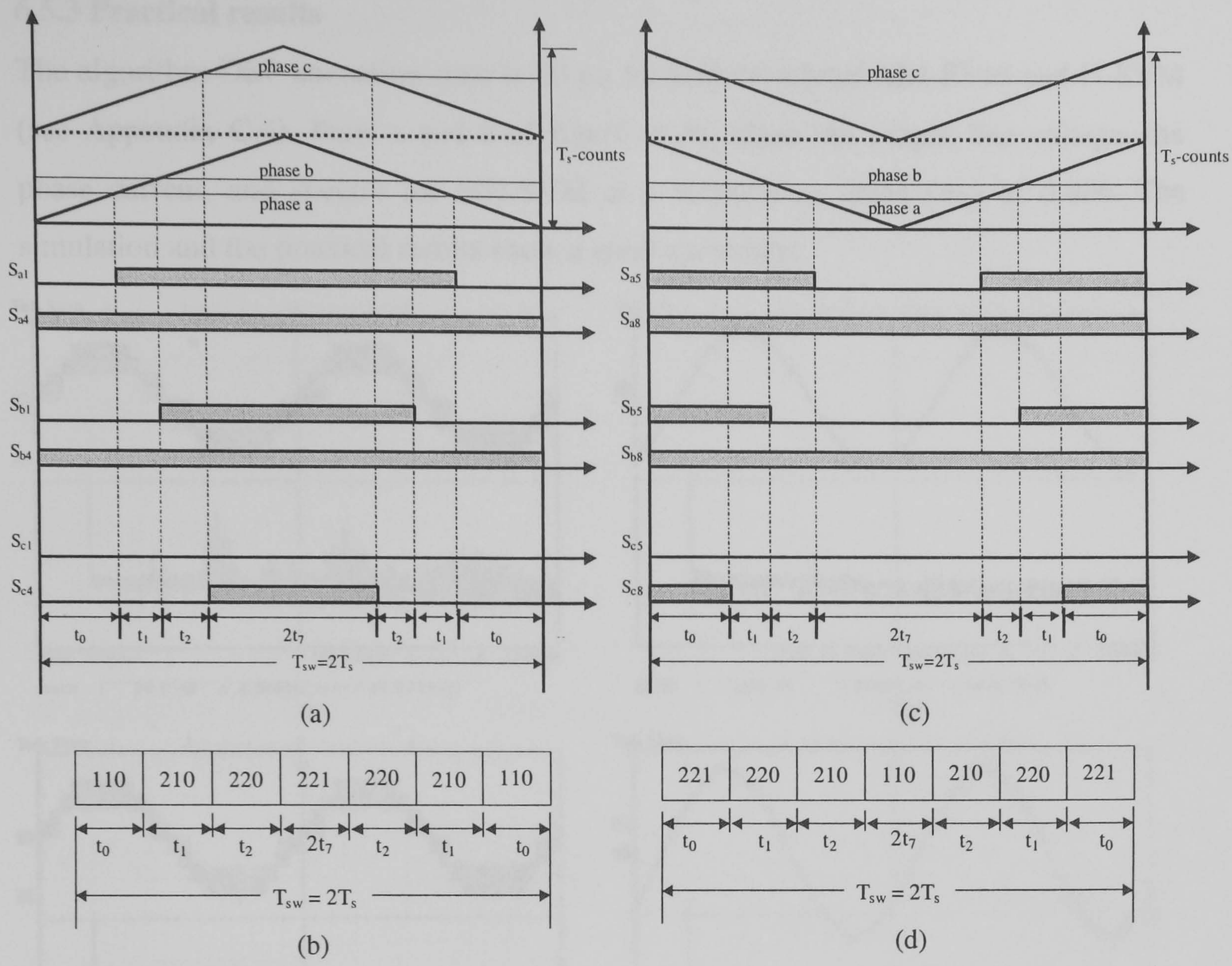


Figure 6.34. Representation for one switching cycle in sector one region four for both up-down counter: (a) first up-down counter and (b) its state transitions, and (c) second up-down counter and (d) its state transitions

6.5.2 Simulation

Five-level MH-SVM is simulated using Matlab/Simulink. Figure (6.35) shows the line voltage and the power spectrum of the line voltage for five-level MH-SVM at modulation index of 0.9 and 3 kHz switching frequency.

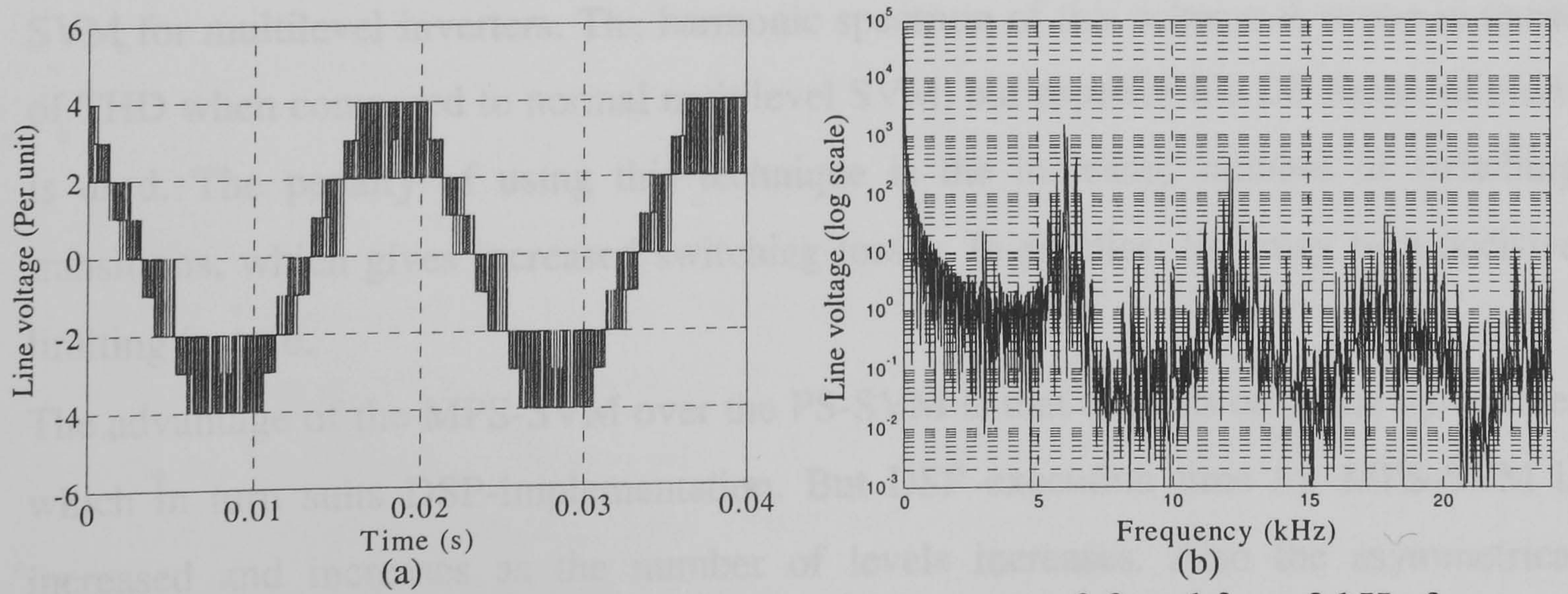


Figure 6.35. Simulated five-level line voltage at $m_a = 0.9$ and $f_{sw} = 3$ kHz for (a) MH-SVM and (b) its power spectrum

6.5.3 Practical results

The algorithm DSP execution time is 20 μs for both five-level MH-SVM and H-SVM (see Appendix C.4). Parts a and b of figure (6.36) show the output line voltage, the phase current, and spectra for MH-SVM at a modulation index (m_a) of 0.866. The simulation and the practical results show a good agreement.

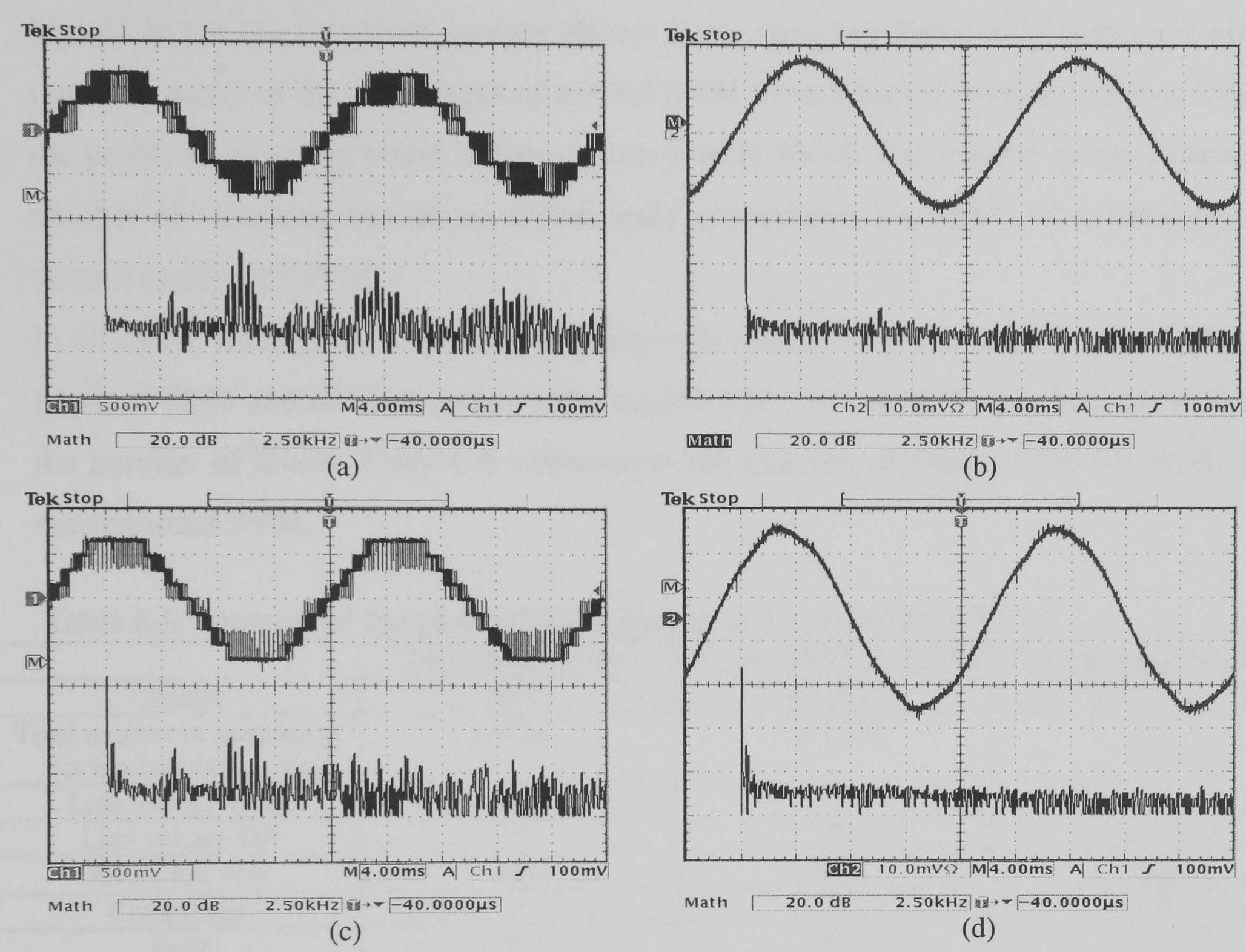


Figure 6.36. Practical output line voltage and phase current and spectra (semi log) for MH-SVM (a) and (b) for modulation index (m_a) = 0.866 (c) and (d) for modulation index (m_a) = 2 (power factor of 0.938 lag) (100V/div & 2A/div)

6.6 Conclusion

PS-SVM has the shortest execution time while retaining many of the advantages of SVM for multilevel inverters. The harmonic spectrum of this scheme is worse in terms of THD when compared to normal multilevel SVM, but superior if a DF figure of merit is used. The penalty of using this technique is the increased number of switching transitions, which gives increased switching losses. In practice, this may be a decisive limiting feature.

The advantage of the MPS-SVM over the PS-SVM is that it needs only one up-counter which in turn suits DSP-implementation. But DSP execution time for MPS-SVM is increased and increases as the number of levels increases. Also the asymmetrical sampling property is not a feature of MPS-SVM.

H-SVM has a shorter execution time while retaining many of the advantages of normal SVM for multilevel inverters. The harmonic spectrum is worse in terms of THD when compared to normal multilevel SVM, but superior if a DF figure of merit is used (for more than five levels). The penalty is the increased number of switching transitions which in turn leads to increased switching loss.

MH-SVM for the five-level inverter allows faster sampling times to be achieved while retaining many of the advantages of normal SVM for multilevel inverters. It overcomes the problems of using phase shifted counters in H-SVM. The penalty is the increased number of switching transitions which leads to increased switching loss, compared to normal multilevel SVM.

In all cases, for a given switching frequency per switch, conventional SVM is better in terms of THD and DF, but result in the longest DSP execution time, which depends on the number of levels. Table 6.5 summarizes the features of phase shifted, hybrid, and conventional SVM.

Table 6.5. Features of the phase shifted, hybrid, and conventional SVM

	Phase shifted SVM	Hybrid SVM (H-SVM)	Normal multilevel SVM
Counter	*(m-1)*	*(m-1)/2*	*one*
Total number of switchings per fundamental cycle	$(m-1)f_s$	$(m-1)f_s/2$	f_s
Line voltage THD	***	**	*
Line voltage DF	*	**	***
Execution time	*18*µs	*20* µs	*44* µs
Complexity	*	**	***
dv/dt	***	**	*
Line voltage fundamental	*The same*		

*** highest, ** mid, * lowest

References

[6.1] L. M. Tolbert and T. G. Habetler, 'Novel multilevel inverter carrier-based PWM method', Ind. Applicat., IEEE Trans., Vol. 35, Sept.-Oct. 1999, pp. 1098-1107.

[6.2] A. M. Massoud, S. J. Finney, and B. W. Williams, 'Control Techniques for Multilevel Voltage Source Inverters', Power Electronics Specialists Conference, 2003. PESC03. IEEE 34rd Annual, Vol. 1, pp. 171-176.

Chapter 7

Active Power Filters

7.1 Harmonics

A harmonic is a component of a periodic wave having a frequency that is an integral multiple of the fundamental power line frequency.

7.1.1 Harmonic Production

Harmonics are a by-product of modern electronics. They occur frequently because of a large number of personal computers (single phase loads), uninterruptible power supplies (UPS), variable frequency drives (AC and DC) or any electronic equipment using solid state power switching supplies to convert incoming AC to DC/AC. Non-linear loads produce harmonics by drawing current in abrupt short pulses, rather than in a smooth sinusoidal manner. The terms "linear" and "non-linear" define the relationship between current and voltage. A non-linear load has a discontinuous current relationship that does not correspond to the applied voltage waveform.

The point of common coupling (PCC) is the location where the harmonic voltage and current distortion are measured or calculated. The PCC can be on the primary or secondary of a utility transformer or at the service entrance of the facility.

7.1.2 Effects and Negative Consequences of harmonics

High levels of harmonic distortion can lead to distribution system problems and may cause other equipment to shutdown [7.1]. Distortion problems can be severe in small power networks where impedance may be significant, resulting in increased voltage distortion at the PCC [7.2]. Harmonics may adversely affect conductors, capacitors, fuses, transformers, generators, meters, supplies, computers, telephones, etc.

7.2 Types of Harmonics

7.2.1 Current source harmonics

For thyristor inverters with inductive loads, the harmonic current content and characteristics are less dependent of the AC side, hence this type of harmonic source behaves like a current source [7.3]. Thus they are called a harmonic current source and are represented as a current source.

7.2.2 Harmonic voltage sources

Another typical harmonic source is that of diode rectifiers with DC smoothing capacitors. Generally the impedance of capacitors decreases at higher frequencies [7.3]. Connecting large capacitance to the DC side of the diode rectifier causes a much lower impedance for harmonics. The harmonic current amplitude on the AC side is greatly affected by the impedance of the AC side. Therefore, a diode rectifier behaves like a voltage source (rather than a current source).

7.2.3 Problems of harmonic compensation for harmonic voltage sources

It is common to attempt to use shunt active filters for harmonic compensation of harmonic voltage sources. However, the impedance of the diode rectifier to harmonics is not much higher than that of the source side. So the compensation current injected by the shunt active filter flows into both the source and diode rectifier. Therefore shunt active filters can not cancel the harmonics completely but may cause problems such as enlarging the DC ripple and AC peak current of the diode rectifier. To avoid these problems, F. Z. Peng et al. showed that added series inductance is required [7.4] if a shunt active filter is used. In [7.4] the use of a series active filter is proposed to overcome these problems.

7.3 Passive Filters

To solve the problem of harmonics, two approaches have been considered in the last two decades. In the first approach, better AC current inverters with sinusoidal current and controllable power factor on the AC side have been studied and the problem is therefore avoided. This solution can be used in new products. For non-linear loads already in use, compensation by either passive or active filters is the normal solution. Traditionally, the passive filter, capacitor bank, and thyristor control reactor (TCR) are used to filter the harmonics and to compensate the reactive current due to non-linear loads [7.5]. Advantages of passive filters are easy maintenance, less expensive, and less complexity, however, in practice these filters have many disadvantages [7.6]-[7.10].

- As both the harmonic and the fundamental current components flow into the filter, the filter capacity must be rated by taking into account both current components.
- When the harmonic current components increase, the filter can be overloaded.
- Parallel resonance between the power system and the passive filter causes amplification of harmonic currents on the source side at a specific frequency.

- De-tuning of the harmonic frequency with aging of the passive components.
- Filtering characteristics are dependent on the source impedance which is usually not accurately known and may change with network configuration.
- The filter can cause series resonance with the source leading to large currents flowing through the device.
- The operating frequency of the AC system varies around its nominal value as the loading condition of the system changes and, therefore, the sharpness of ac filters need to account for these changes.
- They only filter the frequencies they were previously tuned for.
- Designing AC passive filters is not a trivial task. It tends to be so complex that the practical meaning of its results can easily become lost.
- There are constraints on the choice of filter component values so as to compromise the requirements on AC-current harmonic flow in the AC system and on reactive power supplied.

7.4 Thyristor Controlled Reactor

Thyristor based static VAR compensators (SVC's) for reactive power flow control were first developed in the late 1960s and are commonly used today by power utilities. These can be used in either a thyristor switched capacitor (TSC) configuration or as a thyristor controlled reactor (TCR) [7.10]. The TCR is designed to supply variable reactive power instead of the capacitor bank for fixed reactive power. Nevertheless, in order to provide variable reactive power, the TCR capacitor must be complemented by an inductor. Moreover, the TCR cannot provide instantaneous reactive power because of its inherent time delay. The conventional passive filter and TCR cause leading or lagging current by repeatedly accumulating energy in the energy storage elements and then releasing it back into the system.

7.4.1 Reactive Power Compensation

Reactive power is normally compensated by using conventional techniques such as thyristor-controlled reactors and capacitors [7.11]. It is not common to use sophisticated active power filter circuits in order to compensate only for reactive power. Reactive power compensation is mainly suited for low power applications due to the fact that the amount of current needed is of the same order as the rated load current. It would be poor utilization of sophisticated equipment to tackle correction without the use of other power factor correction devices.

7.5 Loading Power and Power Factor

Traditionally, active power, defined as the average value of the product of voltage and current, has been recognized to cause real electric energy flow between two sub-systems [7.12]. Conversely, reactive power, defined as a conservative and orthogonal term to active power, has been considered to cause no real energy flow but increases the steady state current in sinusoidal systems.

7.5.1 Loading power definition

Loading power [7.13] can be divided, as shown in figure (7.1), into:

- *Active power* is defined as the average rate of the energy transfer from the source to the load over an interval of time. Active current [7.14] is defined as the minimum effective current associated with the transfer of the average power to the load over a predefined period.
- *Fictitious power* includes all components of power that cause the loading power to be higher than the active power.
- *Reactive power* can be divided into fundamental and residual power. The *fundamental reactive power* is the cross product of the fundamental component of voltage and current. While the *residual reactive power* component is the difference between the reactive and the fundamental reactive powers. For a single-phase circuit, reactive power is the power that circulates between the source and the load. While in poly-phase circuits, reactive power is the power that circulates between the source and the phases and the power that circulates among phases.
- *Deactive power* is associated with the non-similarity or uncorrelation between the voltage and current waveforms. For this reason the deactive power can be called uncorrelated fictitious power.

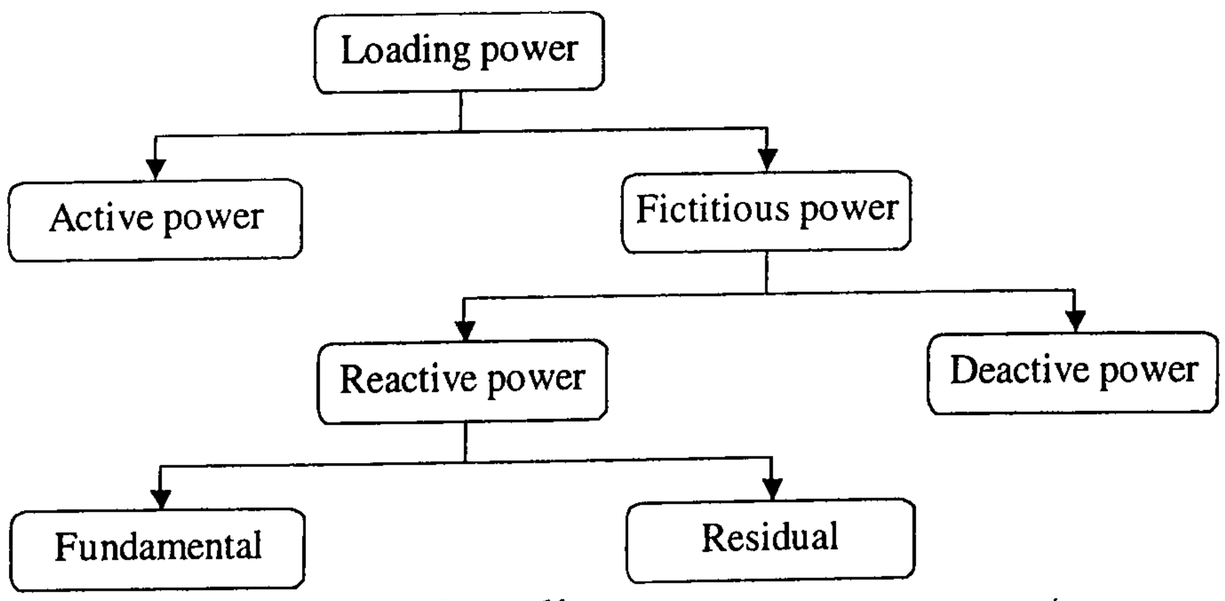


Figure 7.1. Loading power components

7.5.2 Power factor definition in 3-D space current coordinate system

In this definition, the current is expressed in terms of three mutually orthogonal components [7.15]– active, reactive, and distorted components as shown in figure (7.2). Therefore, their r.m.s. values fulfil the following relationships

$$I^2 = I_a^2 + I_r^2 + I_d^2 \tag{7.1}$$

$$I^2 = I_1^2 + I_d^2 \tag{7.2}$$

where

$$I_1^2 = I_a^2 + I_r^2 \tag{7.3}$$

where I : system r.m.s. current

I_a : active r.m.s. component of I

I_r : reactive r.m.s. component of I

I_d : distorted r.m.s. component of I

I_1 : fundamental r.m.s. component of I

If the supply voltage is an undistorted sinusoidal waveform, then only the fundamental component of the system current contributes to average power flow. So the power factor angle shown in figure (7.2) can be expressed as

$$\cos(\phi) = \frac{I_a}{I} \tag{7.4}$$

and the total harmonic distortion (THD) can be expressed as (see figure (7.2)):

$$THD = \frac{I_d}{I_1} \tag{7.5}$$

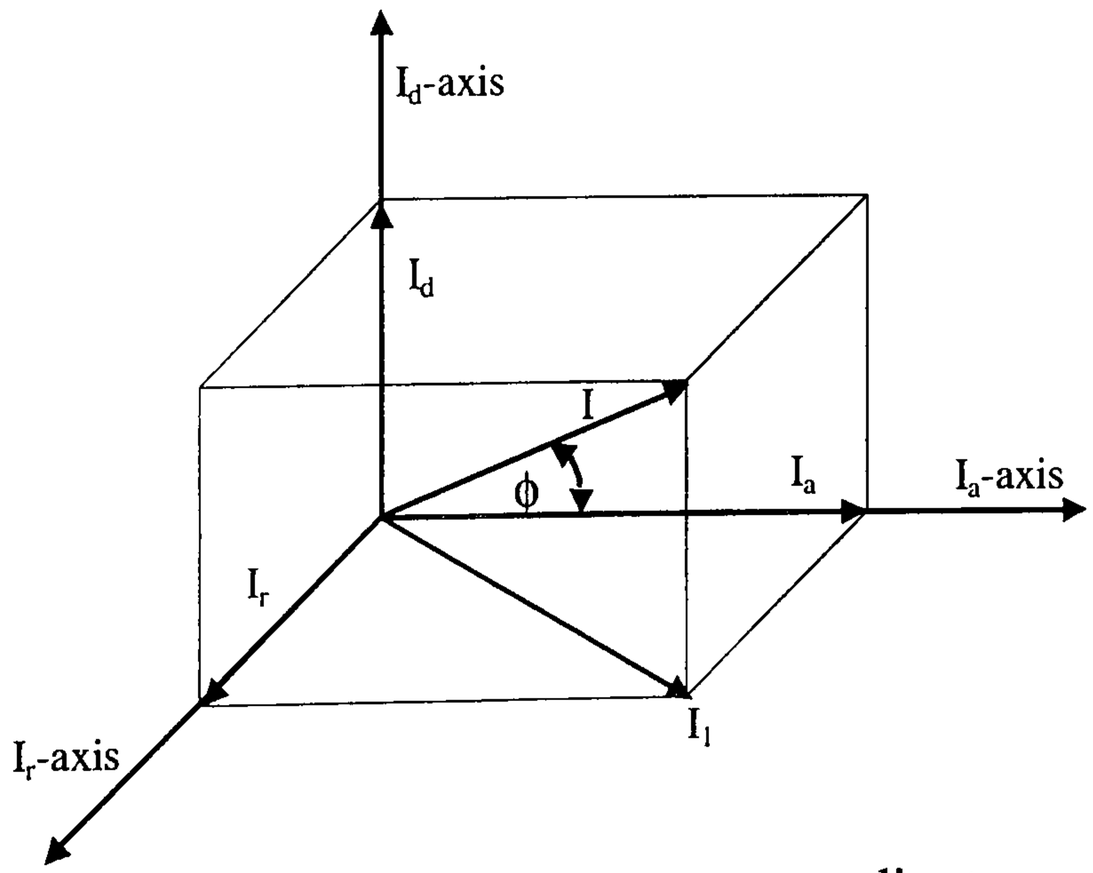


Figure 7.2. 3-D space current coordinate system

7.6 Active Power Filters

Active power filters are divided into AC and DC filters [7.16]. Active DC filters have been designed to compensate for current and/or voltage harmonics on the DC side of thyristor inverters for HVDC systems and on the DC link of a PWM rectifier/inverter for traction systems [7.17]-[7.21]. AC active filters, generally known as active filters (AFs), are also called active power line conditioners, instantaneous reactive power compensators, active power filters, and active power quality conditioners [7.22]. AFs are a mature technology for providing compensation for harmonics, reactive power, and/or neutral current in ac networks. AFs are also used to eliminate voltage harmonics, to regulate terminal voltage, to suppress voltage flicker, and to improve voltage balance in three-phase systems [7.22]. Active power filters, rather than passive filters, have better harmonic compensation characteristics for coping with impedance variation of the AC power line and the frequency variation of harmonic currents. A voltage source PWM inverter is usually used in active power filters (APF) and VAR compensators. A voltage source APF has a capacitor on the DC side with constant DC voltage whereas a current source APF has an inductor with constant DC current. Although the voltage source type is better with regards to losses and filter capacity to eliminate PWM carrier harmonics, the current source type is better with regards to dynamics of compensating current as well as reliability and protection [7.7]. Active filters have a few disadvantages [7.10]:

- The initial and running costs, losses, and complexity of an active filter are much higher than that of a passive filter.
- It is difficult to build an active filter with both a high power rating and a fast dynamic current response.

Depending on the topology, the APF can be classified as series, shunt, or unified power quality conditioner which uses a combination of both. Combinations of active series and passive shunt filtering are known as hybrid filters [7.22].

The maximum harmonic order to be suppressed has no theoretical limit, and is determined by the switching pattern of the active filter. Injecting PWM current enables the harmonic components of orders not greater than the pulse number per half cycle, to be removed completely [7.23]. If harmonic components change in magnitude and frequency, active filters can continue to function without changing any components.

7.6.1 The current source inverter as an APF

This inverter behaves as a nonsinusoidal current source, providing the harmonic current requirements of the nonlinear load. A diode is used in series with the self-commutating device (IGBT) for reverse voltage blocking [7.22]. However, GTO-based configurations may not need the series diode, but have a restricted switching frequency. The inverters are considered sufficiently reliable, but have high losses and require high capacitance. Moreover, they are difficult to use in multilevel or multistep modes to improve performance at higher power levels.

7.6.2 The voltage source inverter as an APF

The voltage source APF has a self-supporting dc voltage bus with a large dc capacitor [7.22]. It has become more dominant since it is lighter, cheaper, and easily expandable to multilevel and multistep versions. It is more popular in UPS-based applications, because in the presence of the mains, the same inverter bridge can be used as an AF to eliminate harmonics in critical nonlinear loads.

7.6.3 Shunt active power filter

Parallel filters have the advantage of carrying only the compensation current plus a small amount of active fundamental current supplied to compensate for system losses [7.24],[7.30].

7.6.4 Series active power filter

The series active filter does not compensate for load current harmonics but acts as a high-impedance to the current harmonics from the power source side. Series active filters are less common industrially than their rivals, parallel active filters. This is because they have to handle the full load current, which increases their current rating considerably compared with parallel filters. This effect may be worse on the secondary side of the coupling transformer, increasing the I^2-R losses and the physical size of the filter. The main advantage of series filters over the parallel version is that they can eliminate voltage-waveform harmonics and balance three-phase voltages [7.24]. The approaches available for detecting harmonic voltage are mainly the filtering method with a fixed filter (such as low pass filter) and sampling digital calculation methods based on the FFT. However there are some problems with these approaches. With the former it is difficult to select the circuit parameters because of the requirement for selectivity and phase. Time lag and frequency drift reduce precision. The latter methods

need high precision analogue to digital converters and detection is slow, tending to eliminate it from real time application [7.25]. Table 7.1 summarizes the salient features of both filters.

Table 7.1. Comparison of parallel and series active filters [7.3]:

	Shunt active filter	Series active filter
Connection	In shunt	In series
Active filter acts as	Current source	Voltage source
Rating	Supports full load voltage but low current	Conducts full load current but low voltage
Function	Current harmonics	Voltage harmonics
Adaptive loads	Inductive or current source loads or harmonic current sources, e.g., phase controlled thyristor rectifiers of DC drives	Capacitive or voltage source loads or harmonic voltage sources, e.g., diode rectifiers with direct smoothing capacitors of AC drives
Compensation characteristics	Excellent and independent of the source impedance for current source loads but depends on source impedance when the load impedance is low	Excellent and independent of the source impedance and the load impedance for voltage source loads, but depend on the load impedance when the loads are a current source type
Application considerations	Injected current flows into the load side and may cause overcurrent when applied to a capacitive or voltage source load	A low impedance parallel branch (parallel passive filter or power factor improvement capacitor bank) is needed when applied to an inductive or current source load

7.6.5 Combinational filters

The inverter type series active filter, which constitutes a high impedance for high-frequency harmonics [7.24], can be accompanied by a parallel passive filter to provide a path for the harmonic currents of the load. Alternatively, an active filter is designed to eliminate only part of the low-order current harmonics while the passive filter is designed to eliminate the bulk of the load-current harmonics [7.24] as shown in figure (7.3a). The main drawback of this technique is that it contains many power components, especially the passive filter. Since filters are permanently connected to the system, this approach is only suitable for a single load with a predefined harmonic source.

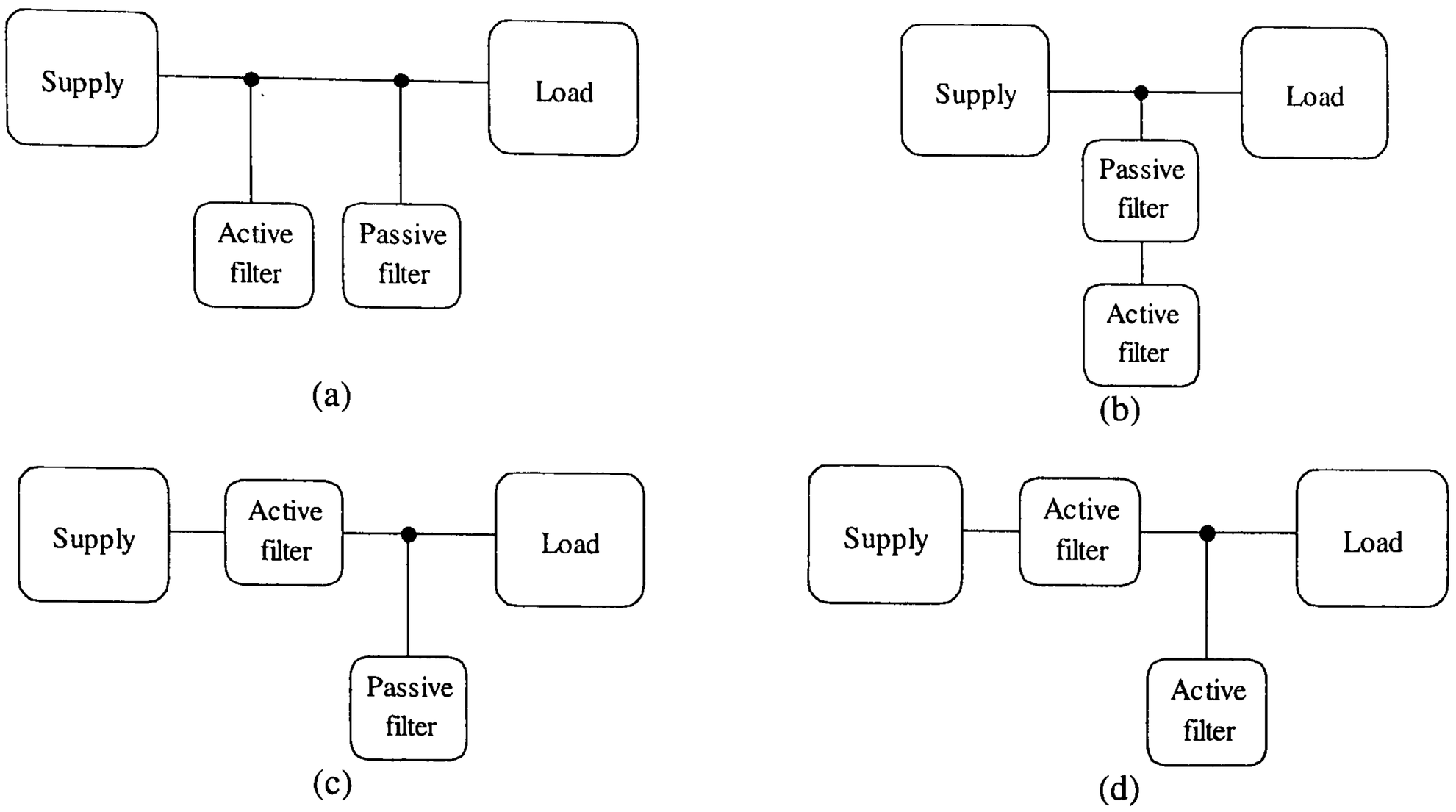


Figure 7.3. Filters combinations:
(a) parallel active and passive filters, (b) active filter in series with parallel passive filter, (c) series active and parallel passive filter, and (d) unified power quality conditioner

Several publications exist for an active filter in series with parallel passive filters, figure (7.3b), especially for medium and high voltage applications where the passive filter reduces the voltage stress on active filter switches [7.24].

To reduce the complexity of the active and passive filter, the active filter is connected in series while the passive filter is connected in parallel [7.24], as shown in figure (7.3c). This configuration overcomes the problems of source impedance interaction with the passive filter.

The unified power quality conditioner for the distribution system shown in figure (7.3d) is different in operation, purpose, and control strategy from the unified power flow controller for transmission systems [7.16]. The functions being performed by the series active filter are harmonic isolation between the sub-transmission system and the distribution system, voltage regulation, and voltage flicker/imbalance compensation at the PCC. The functions performed with the shunt active filter are harmonic current and/or negative sequence current compensation and DC link voltage regulation between both active filters.

7.6.6 High-power applications

The implementation of high-power dynamic filters may not be cost effective, because of the lack of high switching frequency power devices that can control the current flow at high-power ratings [7.24]. Device voltage ratings are limited to 6.5 kV. Harmonic

pollution in the high-power ranges is not the major problem, as it is in lower-power systems. High-power systems include power-transmission grids and ultrahigh-power DC drives as well as DC transmission systems. The effect of harmonics generated at the low-power side are minimised, either naturally or by the installation of several medium- and low-power active filters downstream, which contribute to the compensation. Static VAR compensation is the major concern and is usually catered for by using traditional static power conditioners/filters, such as several sets of synchronous condensers connected in parallel or cascaded multilevel inverter VAR compensators.

One of the few applications of active filters in high-power systems is the Japanese bullet train (Sinkansen), which uses a parallel combination of several active filters. The control and co-ordination requirements are complex.

7.7 Design Methodology

A parameter which is important in shunt active filter design is the order 'm_h' of the highest harmonic to be reduced [7.26]. Then the frequency capability of the active filter capability will be:

$$f_{af} = m_h . f_s \tag{7.6}$$

where f_s is the fundamental frequency of the power network. The frequency f_{af} is chosen in accordance with the maximum switching frequency of the voltage source inverter VSI (f_{VSI}). If f_{af} is higher than f_{VSI} , it will be impossible to control the VSI line currents and the harmonics will not be eliminated. As a compromise, $3 f_{af} \leq f_{VSI} \leq 10 f_{af}$, is used, as shown in figure (7.4). The lower factor results when semiconductors are the limiting aspect whilst the high factor is applicable to low power VSIs using high-frequency switches, such as MOSFETs and IGBTs.

A passive filter can be used to reduce the harmonics above the active filter capabilities. The most important harmonic in the current spectrum is related to the VSI switching ripple. In the case of a constant switching frequency f_{VSI} , this component is localized. This is not the case with current control algorithms such as hysteresis and delta modulation. The cut-off frequency of the passive filter f_{pf} is therefore set at

$$f_{pf} = f_{af} \tag{7.7}$$

The next design step is related to the control system since it will be implemented in a digital structure. The anti-aliasing filters for the analogue quantities are fundamental for providing good performance.

The last frequency is related to the VSI switching frequency which has to meet both harmonic elimination and power semiconductor technology requirements. For VSIs, the switching frequency f_{VSI} is dependent on the inverter power requirement. Generally, this power clearly limits the maximum value of f_{VSI}. To circumvent this limit for high power VSIs, the two-level VSI topology can be changed to a multilevel VSI (m>2).

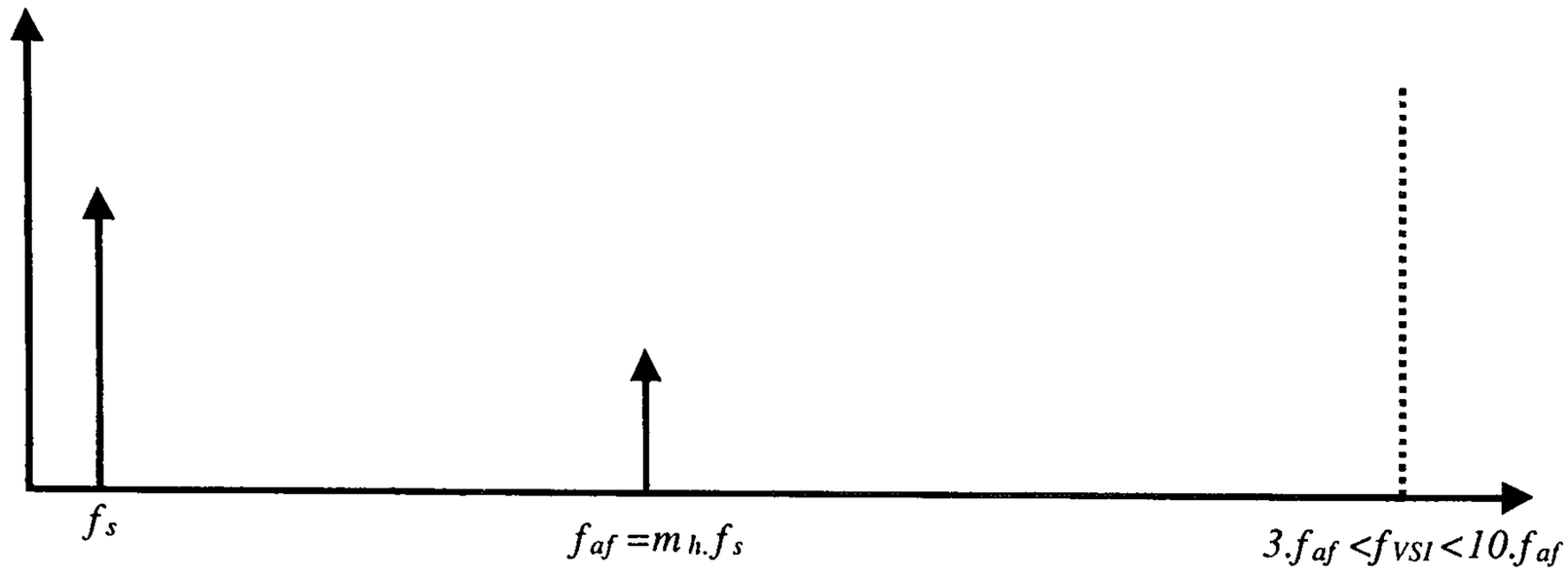


Figure 7.4. Active filter design methodology

7.8 Harmonic Current Extraction Techniques

Various power theories and techniques have been developed for harmonic current extraction as the traditional definitions for active power and reactive power for a linear load is not suitable for a non-linear load. Extraction techniques can be classified into time-based and frequency-based techniques as shown figure (7.5).

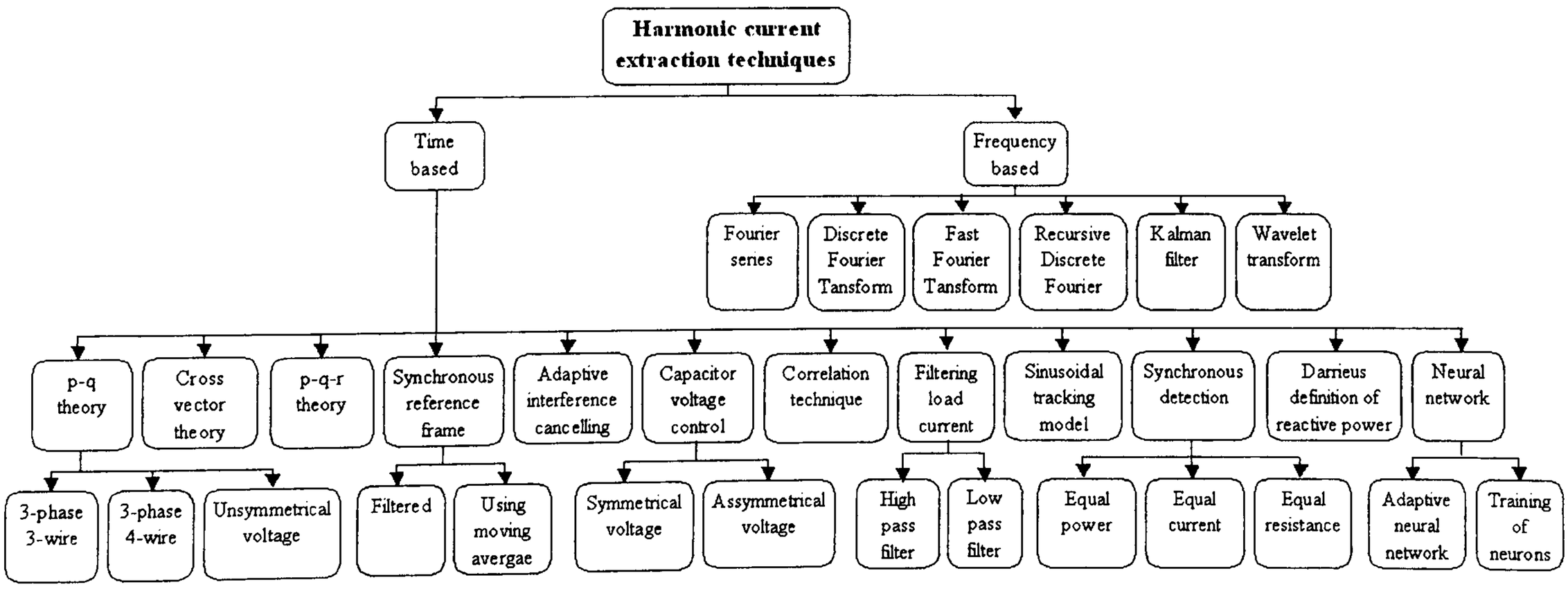


Figure 7.5. Classification of harmonic current extraction techniques

7.8.1 Instantaneous reactive power theory

i. Three-phase three-wire

In 1983, Nabae et al. [7.4], [7.27] proposed an instantaneous reactive power theory

based on the instantaneous value concept. The conventional instantaneous active power for a three-phase circuit can be defined in α–β coordinates as:

$$p = e_\alpha . i_\alpha + e_\beta . i_\beta \tag{7.8}$$

where p is equal to the conventional equation. The instantaneous reactive power is defined as:

$$q = e_\alpha \times i_\beta + e_\beta \times i_\beta \tag{7.9}$$

For a three-phase non-linear load, if the reactive and harmonic producing currents are to be compensated, the compensating current can be expressed as:

$$\begin{pmatrix} i_{c\alpha} \\ i_{c\beta} \end{pmatrix} = \begin{pmatrix} e_\alpha & e_\beta \\ -e_\beta & e_\alpha \end{pmatrix}^{-1} \begin{pmatrix} \tilde{p} \\ q \end{pmatrix} \tag{7.10}$$

where $\tilde{p}$ is the AC component of the instantaneous active power

ii. Three-phase four-wire

Instantaneous reactive power theory can be extended to three-phase circuits which include zero-phase sequence components [7.4], [7.27]. A new term is introduced which is the instantaneous zero-phase sequence power p_0 and is defined as:

$$p_0 = e_0 . i_0 \tag{7.11}$$

The three independent quantities p_0, p, and q can be expressed as:

$$\begin{pmatrix} p_0 \\ p \\ q \end{pmatrix} = \begin{pmatrix} e_0 & 0 & 0 \\ 0 & e_\alpha & e_\beta \\ 0 & -e_\beta & e_\alpha \end{pmatrix} \begin{pmatrix} i_0 \\ i_\alpha \\ i_\beta \end{pmatrix} \tag{7.12}$$

Since the zero-sequence current must be compensated, the reference compensation current in the zero-coordinate is i_0 itself.

iii. Unsymmetrical voltage

If the system voltage is nonsymmetrical [7.50], the new instantaneous reactive power q is defined by:

$$q = e'_a i_a + e'_b i_b + e'_c i_c \tag{7.13}$$

where e'_a, e'_b, and e'_c have 90° (or -90°) delay with respect to e_a, e_b, and e_c.

7.8.2 Cross Vector Theory

The cross vector theory in [7.32], [7.52] defines an instantaneous real power p and three instantaneous imaginary powers. The instantaneous reactive power theory can be defined in the a-b-c reference frame as:

$$q = e \times i = \begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} = \begin{bmatrix} \begin{vmatrix} e_b & e_c \\ i_b & i_c \end{vmatrix} & \begin{vmatrix} e_c & e_a \\ i_c & i_a \end{vmatrix} & \begin{vmatrix} e_a & e_b \\ i_a & i_b \end{vmatrix} \end{bmatrix}^t \tag{7.14}$$

It can be defined in the α–β–0 reference frame as:

$$\begin{pmatrix} p \\ q_0 \\ q_\alpha \\ q_\beta \end{pmatrix} = \begin{pmatrix} e_0 & e_\alpha & e_\beta \\ 0 & -e_\beta & e_\alpha \\ e_\beta & 0 & -e_0 \\ -e_\alpha & e_0 & 0 \end{pmatrix} \begin{pmatrix} i_0 \\ i_\alpha \\ i_\beta \end{pmatrix} \tag{7.15}$$

Similarities and differences between the "3-phase 4-wire" p-q theory and the cross vector theory can be summarized as follows. The first theory considers the zero-sequence circuit as a single-phase circuit independent of the α-phase and β-phase circuits and deals with the zero-sequence current as an instantaneous active current only. This means that no instantaneous reactive current exists in the zero-sequence circuit. For the second theory the zero-sequence, α-phase, and β-phase circuits are considered. This implies that the zero-sequence current can be divided into zero-sequence instantaneous active and reactive currents.

Assuming that the active filter is ideal, the neutral is isolated, and the voltages are balanced, the active filter current can be expressed as [7.29], [7.33]:

$$\begin{aligned} i_{ca} &= i_{La} - \frac{e_a . p}{\left(e_a^2 + e_b^2 + e_c^2\right)} \\ i_{cb} &= i_{Lb} - \frac{e_b . p}{\left(e_a^2 + e_b^2 + e_c^2\right)} \\ i_{cc} &= i_{Lc} - \frac{e_c . p}{\left(e_a^2 + e_b^2 + e_c^2\right)} \end{aligned} \tag{7.16}$$

where i_{La}, i_{Lb}, and i_{Lc} are the load currents and i_{ca}, i_{cb}, and i_{cc} are the compensating currents

7.8.3 The instantaneous power theory using the rotating p-q-r reference frame

Three power components are defined as linearly independent in the p-q-r reference frames [7.34]. Thus, the three current components can be controlled independently by compensating for the three instantaneous power components in the p-q-r reference frames. As shown in figure (7.6a), a new α'-β'-0 reference frame is established by rotating the 0-axis of the α-β-0 reference frame by θ_1, aligning the α–axis with the

projected voltage space vector on the α-β plane. The current space vector in the α\-β\-0 reference frame can be described as:

$$\begin{pmatrix} i'_\alpha \\ i'_\beta \\ i_0 \end{pmatrix} = \begin{pmatrix} \cos\theta_1 & \sin\theta_1 & 0 \\ -\sin\theta_1 & \cos\theta_1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} i_\alpha \\ i_\beta \\ i_0 \end{pmatrix} \tag{7.17}$$

$$\text{where} \quad \theta_1 = \tan^{-1}\left(\frac{e_\beta}{e_\alpha}\right)$$

Next, as shown in figure (7.6b), the p-q-r reference frame can be formed by rotating the β\-axis of the α\-β\-0 reference frame by θ_2 , aligning the α\-axis with the voltage space vector. The current space vector on the p-q-r reference frame is described as:

$$\begin{pmatrix} i_p \\ i_q \\ i_r \end{pmatrix} = \begin{pmatrix} \cos\theta_2 & 0 & \sin\theta_2 \\ 0 & 1 & 0 \\ -\sin\theta_2 & 0 & \cos\theta_2 \end{pmatrix} \begin{pmatrix} i'_\alpha \\ i'_\beta \\ i_0 \end{pmatrix} \tag{7.18}$$

$$\text{where} \quad \theta_2 = \tan^{-1}\left(\frac{e_0}{e_{\alpha\beta}}\right) \quad \text{and} \quad e_{\alpha\beta} = \sqrt{e_\alpha^2 + e_\beta^2}$$

The instantaneous active/reactive powers can be defined respectively by the scalar/vector products of the voltage and the current space vectors.

$$p = \vec{e}_{pqr} \cdot \vec{i}_{pqr} = e_p i_p \tag{7.19}$$

$$q = \vec{e}_{pqrr} \times \vec{i}_{pqr} = [0, -e_p i_r, e_p i_q]^t \tag{7.20}$$

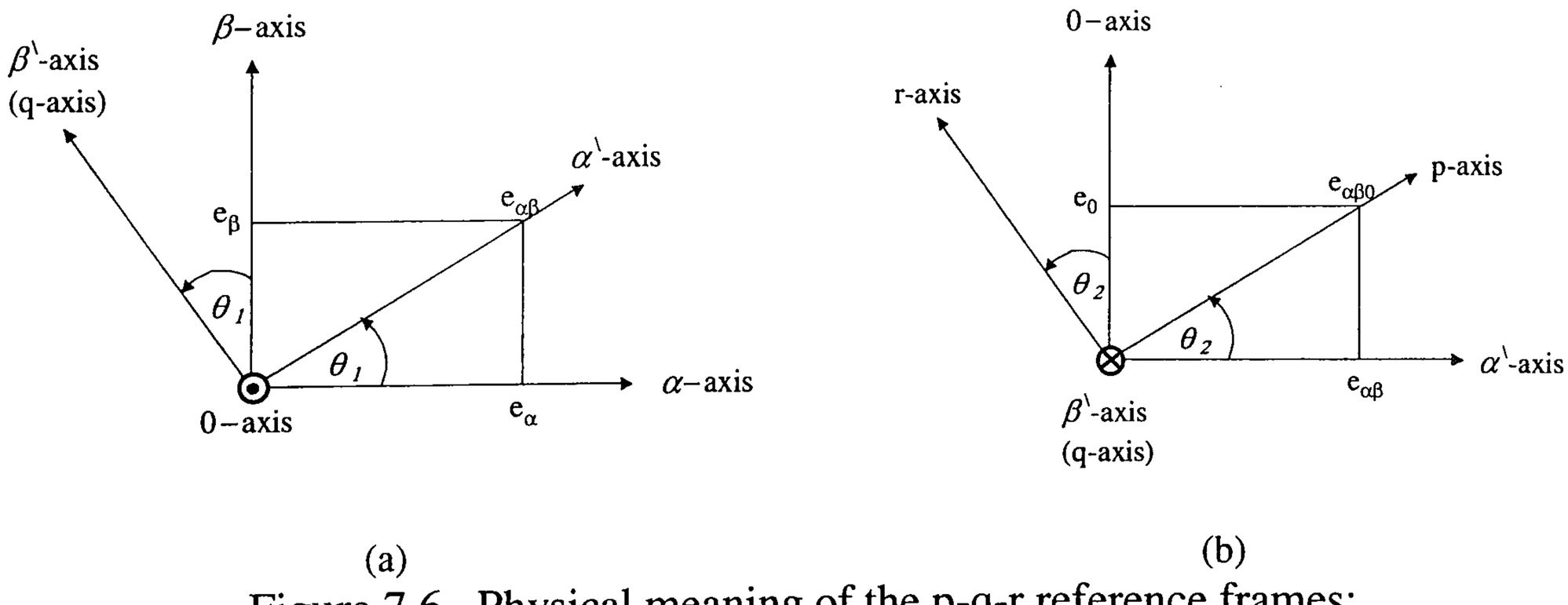


Figure 7.6. Physical meaning of the p-q-r reference frames:
(a) relation between α–β-0 references frame and α\ – β\ –0 refernce frames (view from the top of the 0-axis) (b) relation between α\ – β\ –0 reference frames and p-q-r reference frames (view from the bottom of the q-axis)

Note that *p-q* theory does not observe power conservation since the instantaneous zero sequence reactive power is not defined by the theory. Cross vector theory defines one

instantaneous real power and three instantaneous imaginary powers that observe power conservation, where the three instantaneous imaginary powers are linearly dependent which means they cannot be separately compensated.

The *p-q-r* theory [7.35], [7.36] takes advantage of both *p-q* theory and cross vector theory. The defined instantaneous power observes power conservation. Both instantaneous real and imaginary powers can be defined in the zero-sequence circuit in three-phase four-wire systems. The three power components are linearly independent.

7.8.4 Synchronous reference frame

A synchronous reference frame [7.6],[7.2] was suggested by Divan. The load currents are transformed from the a-b-c stationary reference frame to a d-q synchronously rotating reference frame as

$$\begin{pmatrix} i_d \\ \\ i_q \end{pmatrix} = \frac{2}{3} \begin{pmatrix} \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \\ \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \tag{7.21}$$

where θ is the angle of rotation of the d-q coordinates and is equal to ωt, where ω is the power supply angular frequency. The d and q current components represent the active and reactive power components of the current respectively. The currents can be decomposed into:

$$i_d = \bar{i}_d + \tilde{i}_d \tag{7.22}$$

$$i_q = \bar{i}_q + \tilde{i}_q \tag{7.23}$$

where $\bar{i}_d$ and $\bar{i}_q$ are the fundamental active and reactive current components, while $\tilde{i}_d$ and $\tilde{i}_q$ are the harmonics active and reactive current components.

A low pass filter is used to extract the DC components. The moving average process is another filtering method [7.44].

7.8.5 Adaptive interference cancelling technique

The adaptive interference cancelling technique [7.31] maintains the system in the best operating state by continuously self-tuning. The fundamental components in the load current and the AC source voltage are mutually correlated. In the detecting system in figure (7.7), the AC source voltage is used as the reference input and the load current is used as the primary input, that is, the fundamental component acts as the noise while harmonics act as the signal.

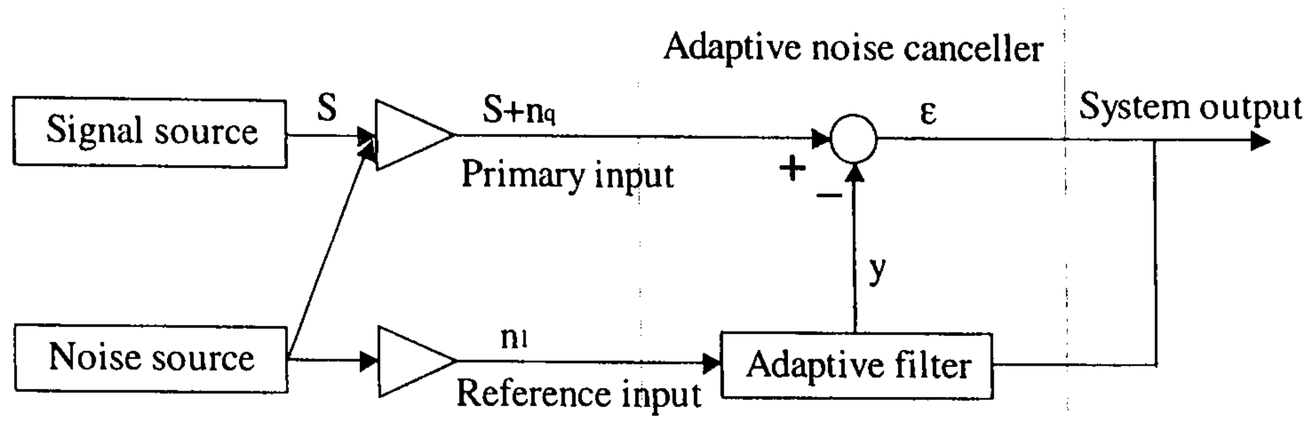
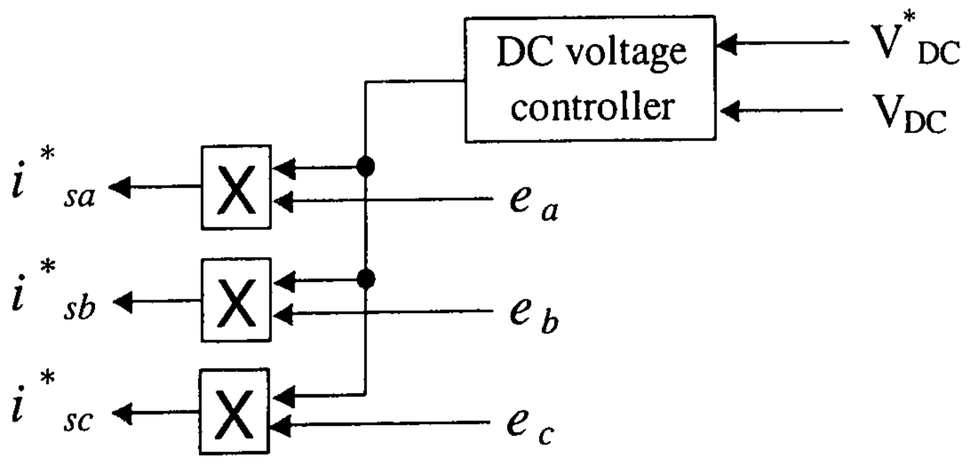


Figure 7.7. Adaptive noise cancelling concept

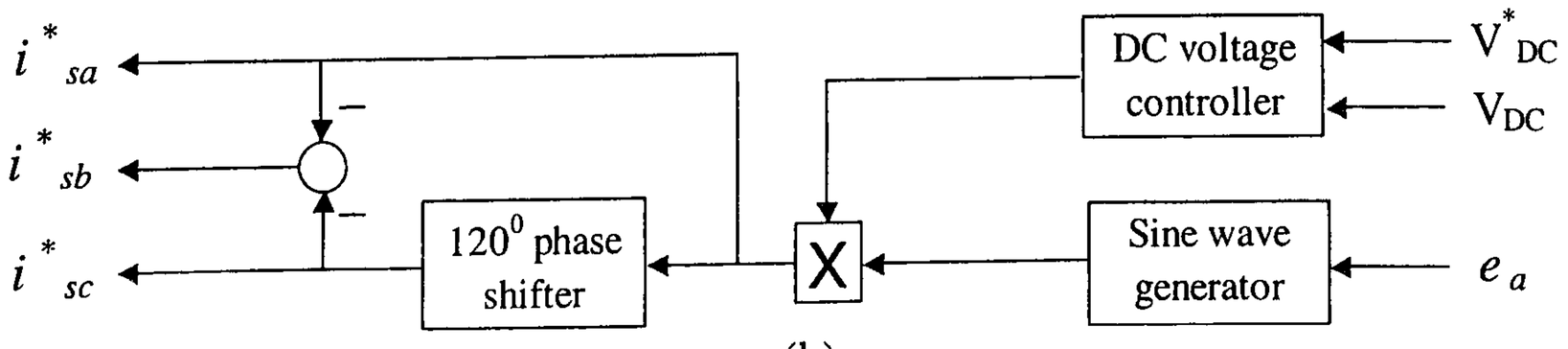
7.8.6 Capacitor voltage control

This technique depends on regulating the DC-bus voltage of the power inverter [7.37]. Harmonic extraction is performed using capacitor voltage control as in [7.38] to [7.41]. This technique is based on power balance where the supply real power must be equal to the load real power plus the inverter losses. To maintain power balance, the capacitor must instantaneously compensate for the difference between the supply and the load power (figure (7.8a)). Controlling the capacitor voltage using a PI controller results in an output which is proportional to instantaneous power balance changes. Multiplying this output by the per unit voltages of the PCC results in the reference supply current. With this concept, the control circuit can be significantly simplified. For obtaining a balanced current under non-ideal mains voltages, only one phase of the mains voltage is used as the phase reference to calculate the desired mains current, as shown in figure (7.8b). For an unbalanced supply, the per unit voltage of the supply voltage is calculated with respect to a common base [7.42] defined as

$$v_{sm} = \sqrt{\frac{2}{3}\left(e_a^2 + e_b^2 + e_c^2\right)} \tag{7.24}$$



(a)



(b)

Figure 7.8. Capacitor voltage control technique

7.8.7 Time domain correlation function technique

Enslin proposed division of the apparent power into two orthogonal components namely real power and fictitious power [7.10]. Fictitious power is also sub-divided into two orthogonal components: reactive and deactive power using correlation techniques. Enslin uses auto-correlation to calculate the r.m.s. values of the measured currents and voltages over the period T. Cross-correlation between the current and voltage over the period dT is used to calculate the active power. The auto-correlation is defined as:

$$R_{vv}(\tau) = \frac{1}{dT}\int_{0}^{dT} v(t).v(t-\tau).dt \tag{7.25}$$

From (7.25), the voltage r.m.s. is defined as:

$$V = (R_{vv}(0))^{\frac{1}{2}} \tag{7.26}$$

The cross-correlation is:

$$R_{vi}(\tau) = \frac{1}{T}\int_{0}^{dT} v(t).i(t-\tau).dt \tag{7.27}$$

From (7.27), the active power can be defined as:

$$P = R_{vi}(0) \tag{7.28}$$

So the active current component is:

$$i_a(t) = \frac{P}{V^2}.v(t) \tag{7.29}$$

7.8.8 Load current filtering

In this method, the distorted load current is filtered, extracting the fundamental current component [7.7]. Thus the filter output current is equal to the fundamental component of the load current. In order to provide the reactive power required by the load, the current signal obtained from the filter is synchronized with the respective phase to neutral source voltage. This technique [7.24] suffers from the phase and magnitude errors introduced by the filter. Two main categories emerge. Using the high-pass-filter method is straightforward for removing low-order frequencies in the load-current signal. Because of differentiation, this technique is vulnerable to noise. A low-pass-filter method is preferred.

7.8.9 Sinusoidal tracking model

In [7.45], the detected load current is applied to the sinusoidal tracking model without transformation. The output of this model is used as the fundamental component of the source current. The resonant frequency is set to the fundamental frequency of the source

voltage. Figure (7.9) shows an equivalent circuit of the sinusoidal tracking model. It is assumed that $\omega_r = 1/L = 1/C$. The state equation of this circuit is

$$\begin{pmatrix} \dot{v} \\ \dot{i} \end{pmatrix} = \begin{pmatrix} 0 & \omega_r \\ -\omega_r & 0 \end{pmatrix} \begin{pmatrix} v \\ i \end{pmatrix} + \begin{pmatrix} 0 \\ \omega_r \end{pmatrix} u \tag{7.30}$$

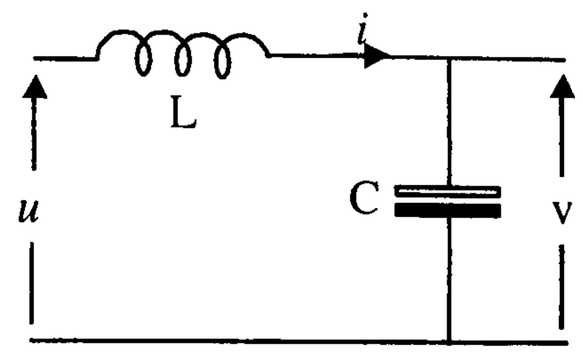


Figure 7.9. Equivalent circuit of sinusoidal tracking model

The output equation is

$$y = k_r \begin{pmatrix} -\sin\theta_r & \cos\theta_r \end{pmatrix} \begin{pmatrix} v \\ i \end{pmatrix} \tag{7.31}$$

where ω_r and k_r are the resonant frequency and the control gain of sinusoidal tracking model, and θ_r is the phase angle of sinusoidal tracking model at the resonance frequency.

7.8.10 Synchronous detection method

For the compensating component calculation there are three approaches [7.56]: equal power synchronous detection (PSD), equal current synchronous detection (CSD), and equal resistance synchronous detection (RSD).

Equal power approach

The three-phase real active power for sinusoidal voltage and current is defined as

$$P = \tfrac{1}{2}(E_{ma} I_{ma} + E_{mb} I_{mb} + E_{mc} I_{mc}) \tag{7.32}$$

For equal power synchronous detection

$$E_{ma} I_{ma} = E_{mb} I_{mb} = E_{mc} I_{mc} \tag{7.33}$$

The line currents after compensation are expressed as:

$$\begin{aligned} i_a(t) &= \frac{P}{3}\left(\frac{2.e_a(t)}{E_{ma}^2}\right) \\ i_b(t) &= \frac{P}{3}\left(\frac{2.e_b(t)}{E_{mb}^2}\right) \end{aligned} \tag{7.34}$$

$$i_c(t) = \frac{P}{3}\left(\frac{2.e_c(t)}{E_{mc}^2}\right)$$

where $e_a(t)$ is the voltage source of phase a, E_{ma} is peak amplitude of the 'a' phase voltage, $i_a(t)$ is the compensated line current. Similarly for the other two phases. Based on the equal power approach, the active power after compensation in each phase is the same. The resulting line currents are different, depending on the corresponding phase voltage.

Equal current approach

For equal current synchronous detection,

$$I_{ma} = I_{mb} = I_{mc} \tag{7.35}$$

The line currents after compensation are

$$i_a(t) = \frac{2.P.e_a(t)}{E_{ma}\left(E_{ma} + E_{mb} + E_{mc}\right)}$$

$$i_b(t) = \frac{2.P.e_b(t)}{E_{mb}\left(E_{ma} + E_{mb} + E_{mc}\right)} \tag{7.36}$$

$$i_c(t) = \frac{2.P.e_c(t)}{E_{mc}\left(E_{ma} + E_{mb} + E_{mc}\right)}$$

The equal current approach compensates the load current to obtain equal line currents. The resulting current waveforms are sinusoidal, equal, and in the correct phase sequence.

Equal resistance approach

For equal resistance synchronous detection,

$$\frac{E_{ma}}{I_{ma}} = \frac{E_{mb}}{I_{mb}} = \frac{E_{mc}}{I_{mc}} \tag{7.37}$$

The line currents after compensation are expressed as:

$$i_a(t) = \frac{2.P.e_a(t)}{\left(E_{ma}^2 + E_{mb}^2 + E_{mc}^2\right)}$$

$$i_b(t) = \frac{2.P.e_b(t)}{\left(E_{ma}^2 + E_{mb}^2 + E_{mc}^2\right)} \tag{7.38}$$

$$i_c(t) = \frac{2.P.e_c(t)}{\left(E_{ma}^2 + E_{mb}^2 + E_{mc}^2\right)}$$

The equal resistance approach assumes that the load resistance will be equal after compensation. The line currents vary depending on the phase voltages.

7.8.11 Darrieus definition of reactive power

In 1970 Darrieus extended the concept of reactive power to non-sinusoidal cases [7.43]. Emile Pillet arranges Darrieus definition in the form:

$$Q = \frac{\omega}{T}\int_0^T i \left(\int_1 u d\tau\right) dt \tag{7.39}$$

Therefore the three-phase reactive power can be defined as

$$q = \omega\left[i_a \int e_a d\tau + i_b \int e_b d\tau + i_c \int e_c d\tau\right] \tag{7.40}$$

In $\alpha\beta 0$ coordinates using an invariant power form, the instantaneous reactive power is given by:

$$q = \omega\left[i_\alpha \int e_\alpha d\tau + i_\beta \int e_\beta d\tau + i_0 \int_0 e_0 d\tau\right] \tag{7.41}$$

7.8.12 Identification by Fourier series

A periodic current $i(t)$ with a zero dc value can be represented [7.49] by:

$$i(t) = \sum_{n=1}^{\infty}\left[a_n \cos(n\omega_f t) + b_n \sin(n\omega_f t)\right] \tag{7.42}$$

where ω_f is the fundamental angular frequency. With a numerical implementation of a moving Fourier series, the coefficients become:

$$a_n(k) = \frac{2}{N}\sum_{j=k-(N-1)}^{k} i(jT_s)\cos(n\omega_f jT_s) \tag{7.43}$$

$$b_n(k) = \frac{2}{N}\sum_{j=k-(N-1)}^{k} i(jT_s)\sin(n\omega_f jT_s) \tag{7.44}$$

where T_s is the sampling period and N an integer. Or recursively:

$$a_n(k) = a_n(k-1) + \frac{2}{N}\left[i(kT_s) + i\left((k-N)T_s\right)\right]\cos(n\omega_f kT_s) \tag{7.45}$$

$$b_n(k) = b_n(k-1) + \frac{2}{N}\left[i(kT_s) + i\left((k-N)T_s\right)\right]\sin(n\omega_f kT_s) \tag{7.46}$$

with $N = T_f/(2T_s)$. The identification response time corresponds to half the fundamental period. In this way the individual current harmonics can be identified.

7.8.13 Other methods

A method to generate the current reference for shunt active power filters is presented in [7.53] which uses a neural network to extract the fundamental sinusoid from a distorted load current waveform. In [7.54], an artificial neural network (ANN) with a large

number of inputs and neurons is used, where the harmonic estimation uses training to determine the weights for different neurons. In [7.55], an adaptive neural network (ANN) is used to determine adaptively the fundamental and harmonic component, instead of training the neurons.

The application of DFTs and FFTs for harmonic current extraction can be found in [7.47]. However, the Recursive Discrete Fourier Transform (RDFT), presented in [7.47], can renew the spectrum values immediately after input of a new data set. Thus the RDFT is more suitable for real-time implementation than DFT and FFT.

The Kalman filter uses a mathematical model of the states to be estimated and a Kalman filter recursive estimation algorithm is presented in [7.48].

Wavelet bases is based on the definition of the active and reactive power in the time-frequency domain using the complex wavelet transform [7.51]. The sub-band of interest is the one that cover the fundamental.

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Chapter 8

Predictive Current Control for the Shunt Active Power Filter

Harmonic mitigation has been a goal in the field of power systems research since the early 60s. Passive filters are used due to their simplicity, low cost, and ease of maintenance. But the disadvantages [8.1],[8.2] of these filters are: the effect of the source impedance on the filtering characteristics and aging of passive components. In the early 80s, Akagi et al. [8.3],[8.4] proposed the instantaneous reactive power theory which made the active power filter practical. Many other methods for harmonic current extraction have been proposed, and have been introduced in chapter seven.

The shunt active filter is the most widely used filter. It acts as a harmonic current source which injects same magnitude anti-phase current to eliminate the load harmonic and reactive components of the current. Figures (8.1) and (8.2) show the single line diagram and the inverter used as the three-phase shunt active power filter.

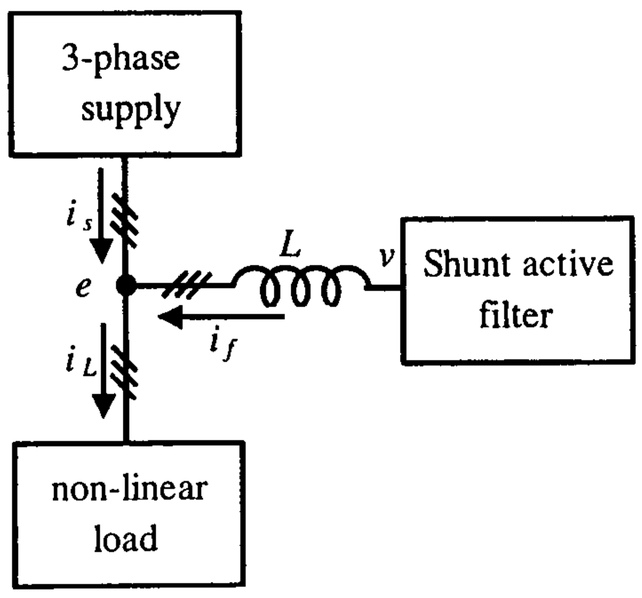

Figure 8.1. Shunt active power filter single line diagram

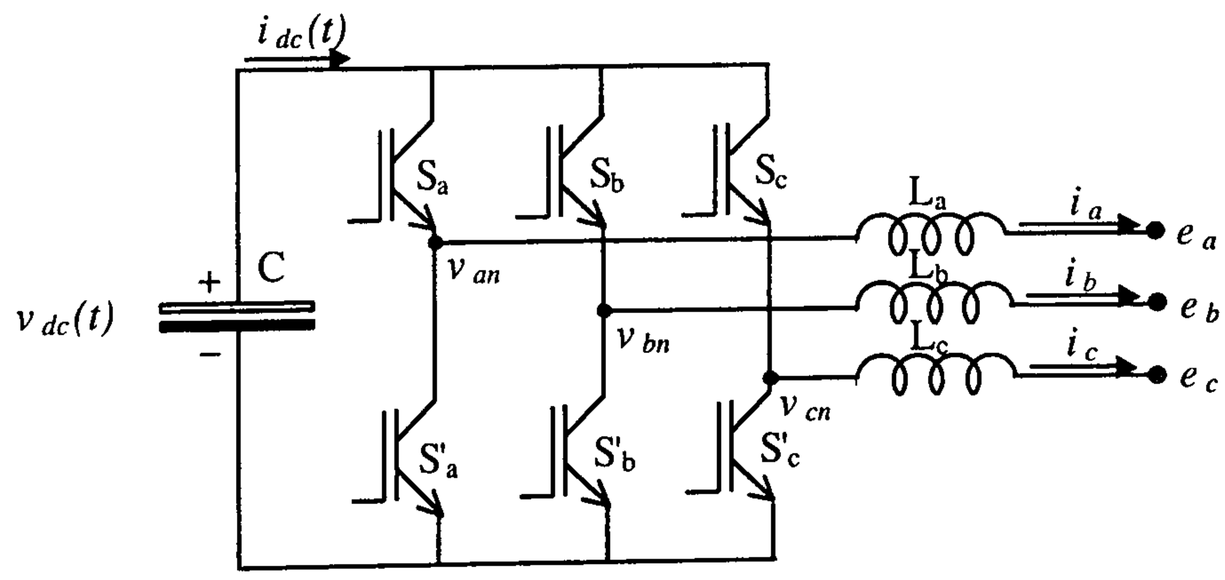

Figure 8.2. The inverter used as a shunt active power filter

In this chapter, new predictive current control for the two-level shunt active power filter is proposed. The active filter output voltage is predicted using the supply current, not the active filter current. Harmonic current extraction is achieved by using the capacitor voltage control technique [8.5] and space vector modulation is used as a pulse width modulation (PWM) technique.

8.1 Proposed method

There are two important controlling parts in shunt active power filter design. The first is the harmonic extraction technique and the second is the current control technique. Harmonic extraction is achieved using capacitor voltage control as in [8.5],[8.12]-[8.14]. Among the most common three current controllers (predictive [8.15]-[8.18], ramp comparison [8.18], and hysteresis [8.18]), predictive current control is now the most commonly used as it is suitable for DSP-implementation, has more precise current control, has minimum distortion, and provides good static and dynamic performance. Therefore, current control is performed using innovative predictive current control with SVM. Besides the advantages of using the predictive current control, the proposed method has advantages such as; the number of sensors used is minimized (the measured quantities are the supply currents, voltages of the point of common coupling (PCC), and capacitor voltage), and the reference currents are the supply currents instead of the active filter currents. This gives good current tracking performance as the reference supply current is sinusoidal while the active filter current mainly consists of harmonic components. The computation burden is reduced. SVM PWM enables the inverter to compensate for load harmonics and reactive currents at a lower capacitor voltage because SVM gives a 15% gain compared to other PWM techniques. Decreasing the capacitor voltage decreases the switching loss and also improves the utilisation of the semiconductor switches used. SVM introduces the lowest THD and lowest ripple current among PWM techniques and has a constant switching frequency.

8.1.1 Capacitor voltage control

Harmonic extraction is performed using the capacitor voltage control introduced in chapter seven [8.5],[8.12]-[8.14]. This technique is based on power balance, where the supply real power must equal the load real power plus the inverter losses. To maintain power balance, the capacitor must compensate for the difference between the supply and the load power instantaneously. So controlling the capacitor voltage using a PI controller results in an output which is proportional to the instantaneous changes in power balance. Multiplying this output by the per unit voltages of the PCC results in the reference supply current. Figure (8.3) shows the proposed system block diagram.

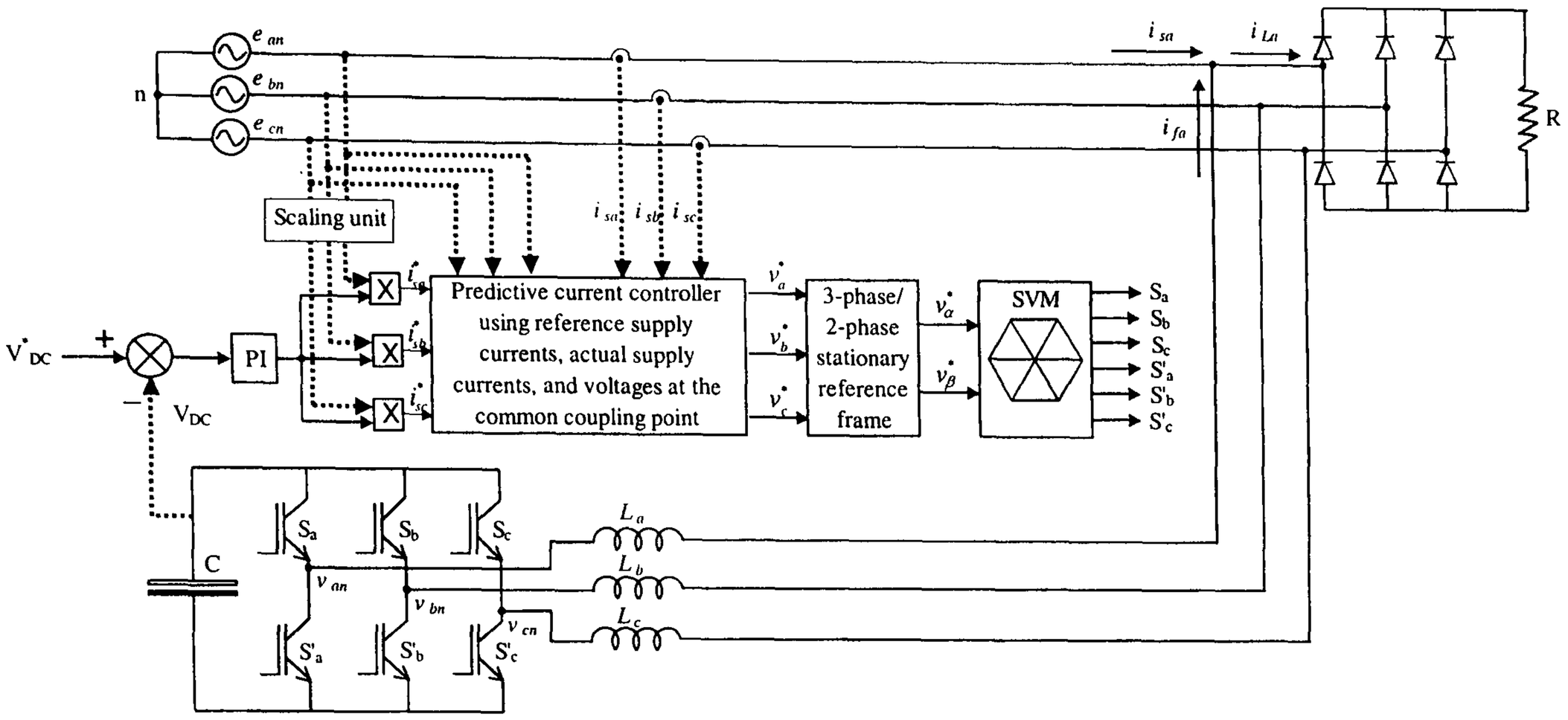

Figure 8.3. Block diagram of the proposed technique
(The dotted lines indicate the measured quantities)

8.1.2 Predictive current control

The reference, measured supply currents, and voltages of the PCC are used to predict the reference output voltage of the inverter required to make the measured current reach its reference at the next sampling instant. The supply is assumed to be balanced, sinusoidal, and with zero impedance. The predicted inverter output reference voltages are used to obtain the inverter switching decision using SVM PWM. In figure (8.3), the equation relating the active filter current, inverter output voltage, and the PCC voltage is:

$$v_x = L_x \frac{di_{fx}}{dt} + e_x \tag{8.1}$$

where x represents the phases a, b, or c;

L_x is the interfacing inductance;

v_x is the active filter output voltage for the x-phase;

e_x is the x-phase voltage of the common coupling point; and

i_{fx} is the x-phase active filter current.

Inductor resistance is neglected. Equation (8.1) can be represented in a discrete form as follows:

$$v_x^*(n+1) = L_x\left(\frac{i_{fx}^*(n+1) - i_{fx}(n)}{T_s}\right) + e_x(n) \tag{8.2}$$

where $i_{fx}^*(n+1)$ and $v_x^*(n+1)$ are the x-phase active filter current and the predicted output voltage references respectively, at sampling instant $n+1$, and T_s is the sampling time.

Using Kirchhoff's current law at the PCC:

$$i_{fx}(n) = i_{Lx}(n) - i_{sx}(n) \tag{8.3}$$

where $i_{Lx}(n)$ and $i_{sx}(n)$ are the x-phase load and supply currents respectively at the sampling instant n. Since the sampling instant $n+1$ is not available, $i^*_{fx}(n+1)$ is replaced by $i^*_{fx}(n)$. This introduces one sampling time delay which becomes less significant as the sampling frequency increases. The active filter reference current can be expressed as:

$$i^*_{fx}(n) = i_{Lx}(n) - i^*_{sx}(n) \tag{8.4}$$

Substituting equations (8.3) and (8.4) into (8.2) results in:

$$v^*_x(n+1) = L_x\left(\frac{i_{sx}(n) - i^*_{sx}(n)}{T_s}\right) + e_x(n) \tag{8.5}$$

Equation (8.5) represents the predicted inverter output voltage, expressed in terms of the reference and actual supply currents.

8.2 Simulation

8.2.1 Shunt active power filter state-space model

As shown in figure (8.2), the inverter output line voltages are expressed as follows:

$$\begin{aligned} v_{ab}(t) &= v_{dc}(t).[s_a - s_b] \\ v_{bc}(t) &= v_{dc}(t).[s_b - s_c] \\ v_{ca}(t) &= v_{dc}(t).[s_c - s_a] \end{aligned} \tag{8.6}$$

where s_a, s_b, and s_c are the switching states of the upper inverter switches, which are '1' for the on-state and '0' for the off-state. v_{dc}(t) is the instantaneous capacitor voltage. For balanced supply voltages and equal interfacing inductances, the APF voltages with respect to the neutral point of the supply are defined as:

$$\begin{aligned} v_{an}(t) &= \tfrac{1}{3}\left[v_{ab}(t) - v_{ca}(t)\right] \\ v_{bn}(t) &= \tfrac{1}{3}\left[v_{bc}(t) - v_{ab}(t)\right] \\ v_{cn}(t) &= \tfrac{1}{3}\left[v_{ca}(t) - v_{bc}(t)\right] \end{aligned} \tag{8.7}$$

From equations (8.6) and (8.7), the phase-to-neutral voltages are:

$$\begin{aligned} v_{an}(t) &= \tfrac{1}{3}v_{dc}(t).[2.s_a - s_b - s_c] \\ v_{bn}(t) &= \tfrac{1}{3}v_{dc}(t).[2.s_b - s_a - s_c] \\ v_{cn}(t) &= \tfrac{1}{3}v_{dc}(t).[2.s_c - s_a - s_b] \end{aligned} \tag{8.8}$$

The three active filter currents, ia, i_b, and i_c can be expressed as:

$$L\frac{di_a(t)}{dt} = v_{an}(t) - e_a(t)$$
$$L\frac{di_b(t)}{dt} = v_{bn}(t) - e_b(t) \tag{8.9}$$
$$L\frac{di_c(t)}{dt} = v_{cn}(t) - e_c(t)$$

Substituting equation (8.7) into equation (8.8) yields

$$L\frac{di_a(t)}{dt} = \tfrac{1}{3}v_{dc}(t).[2.s_a - s_b - s_c] - e_a(t)$$
$$L\frac{di_b(t)}{dt} = \tfrac{1}{3}v_{dc}(t).[2.s_b - s_a - s_c] - e_b(t) \tag{8.10}$$
$$L\frac{di_c(t)}{dt} = \tfrac{1}{3}v_{dc}(t).[2.s_c - s_a - s_b] - e_c(t)$$

Equation (8.10) shows three independent currents. In simulation, the three currents must be checked to sum to zero. Equation (8.10) cannot be used for either unbalanced supply voltages or unequal interfacing inductances. The capacitor current can be expressed in terms of the filter currents i_a, i_b, and i_c as follows:

$$i_{dc}(t) = [2s_a - 1].i_a(t) + [2s_b - 1].i_b(t) + [2s_c - 1].i_c(t) \tag{8.11}$$

The DC voltage is:

$$i_{dc}(t) = -C.\frac{dv_{dc}(t)}{dt} \tag{8.12}$$

Substituting equation (8.10) into equation (8.11) yields

$$-C.\frac{dv_{dc}(t)}{dt} = [2s_a - 1].i_a(t) + [2s_b - 1].i_b(t) + [2s_c - 1].i_c(t) \tag{8.13}$$

Equations (8.10) and (8.13) represent the state space model in the form

$$\dot{X} = A.X + B.U \tag{8.14}$$

where A, X , B, and U are defined as follows

$$A = \begin{bmatrix} 0 & 0 & 0 & \frac{2.s_a - s_b - s_c}{3.L} \\ 0 & 0 & 0 & \frac{2.s_b - s_a - s_c}{3.L} \\ 0 & 0 & 0 & \frac{2.s_c - s_b - s_a}{3.L} \\ \frac{1-2.s_a}{C} & \frac{1-2.s_b}{C} & \frac{1-2.s_c}{C} & 0 \end{bmatrix}$$

$$\mathrm{X} = \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \\ v_{dc}(t) \end{bmatrix},\ \mathrm{B} = \begin{bmatrix} \frac{-1}{L} & 0 & 0 \\ 0 & \frac{-1}{L} & 0 \\ 0 & 0 & \frac{-1}{L} \\ 0 & 0 & 0 \end{bmatrix},\ \text{and } U = \begin{bmatrix} e_a(t) \\ e_b(t) \\ e_c(t) \end{bmatrix}$$

8.2.2 Simulation results

The state space model of the active filter presented in section (8.2.1) is simulated using Matlab/Simulink (see Appendix H.1). The SVM is programmed using an m-file with an s-function block in Simulink. The parameters used in simulation (and also practically) are shown in Table 8.1. The non-linear load is a three-phase uncontrolled bridge rectifier feeding a 70 Ohm resistive load. Parts a to c of figure (8.4) show the simulated load, active filter, and supply currents respectively.

Table 8.1. The system parameters

V_{DC}^{*}	300 V
Supply voltage	110 V
C	50 μF
L	10 mH
Sampling frequency	24.42 kHz
Switching frequency	12.21 kHz

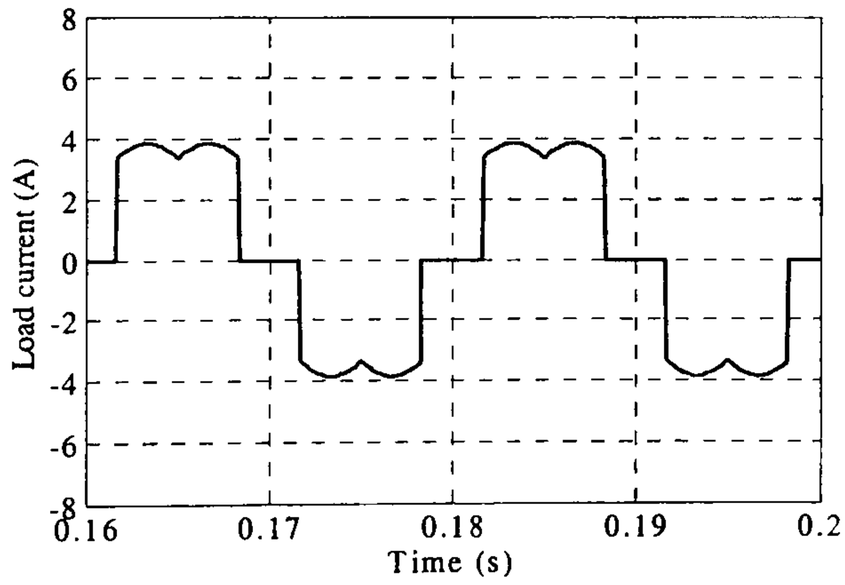

Figure 8.4. Simulation results:
(a) load current, (b) active filter current, and (c) supply current

8.3 Practical results

The execution time of the DSP program is 34 μs (see Appendix D). Voltage and current transducers are used to measure the supply phase voltages (assumed sinusoidal, balanced, and with zero impedance) and currents, and the capacitor voltage. The DSP software compares the reference and measured capacitor voltages, the reference active filter current is extracted, and then the reference voltages are predicted. Using SVM, the sector number and the time periods (t_0, t_1, t_2, t_7) are determined. An external interrupt goes high for the maximum and minimum values (with a frequency of 24.4 kHz) of a digital up-down counter (the digital increment reference period (DIRP) is 160 ns and the counter counts from 0 to 256 to 0 DIRP) within the Xilinx project. This means that the measured quantities will be updated twice in the switching period (switching frequency is 12.2 kHz) as shown in figure (8.5). Then the Xilinx project determines the switching decisions from the sector and time periods (t_0, t_1, t_2, t_7). A dead time of 480 ns (3 DIRP) is provided using the Xilinx project. Figure (8.6) indicates the flow chart of the practical system procedures. Part (a) of figure (8.7) shows the load and supply currents. Parts b to d of figure (8.7) show the load current, supply current, active filter current, and their spectrum. The results compare favourably with the simulation result in figure (8.4)

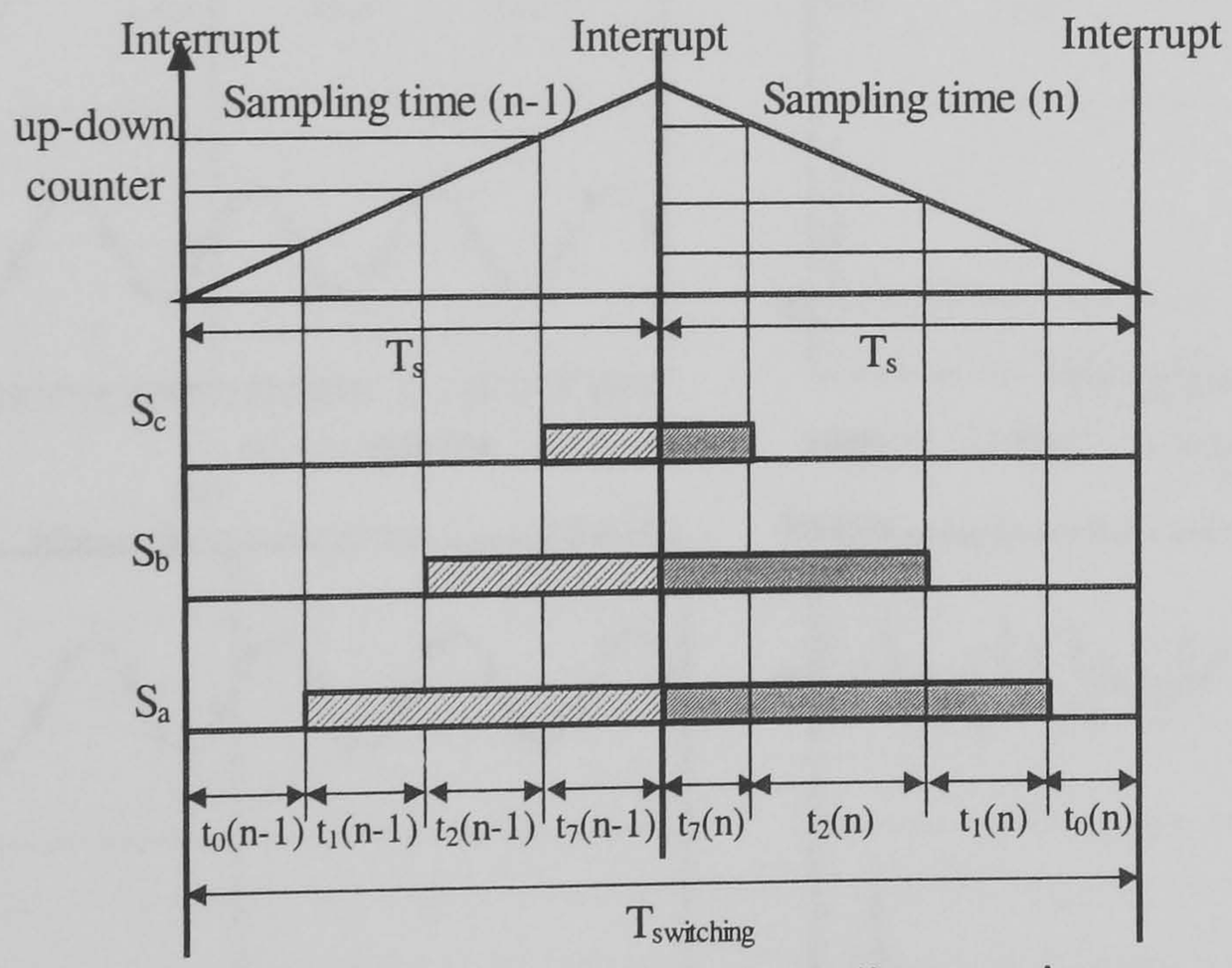

Figure 8.5. One sampling time diagram in sector 1

8.4 Conclusion

An innovative predictive current controller has been proposed for the shunt active power filter. The active filter output voltage is predicted using the supply current, not the active filter current. The approach has been validated by simulation and practically, where the practical and simulation results show a good resemblance. The limitations of

the simulation are that the supply voltages are assumed balanced and of zero impedance, and this is the condition under which the practical experiments have been carried out.

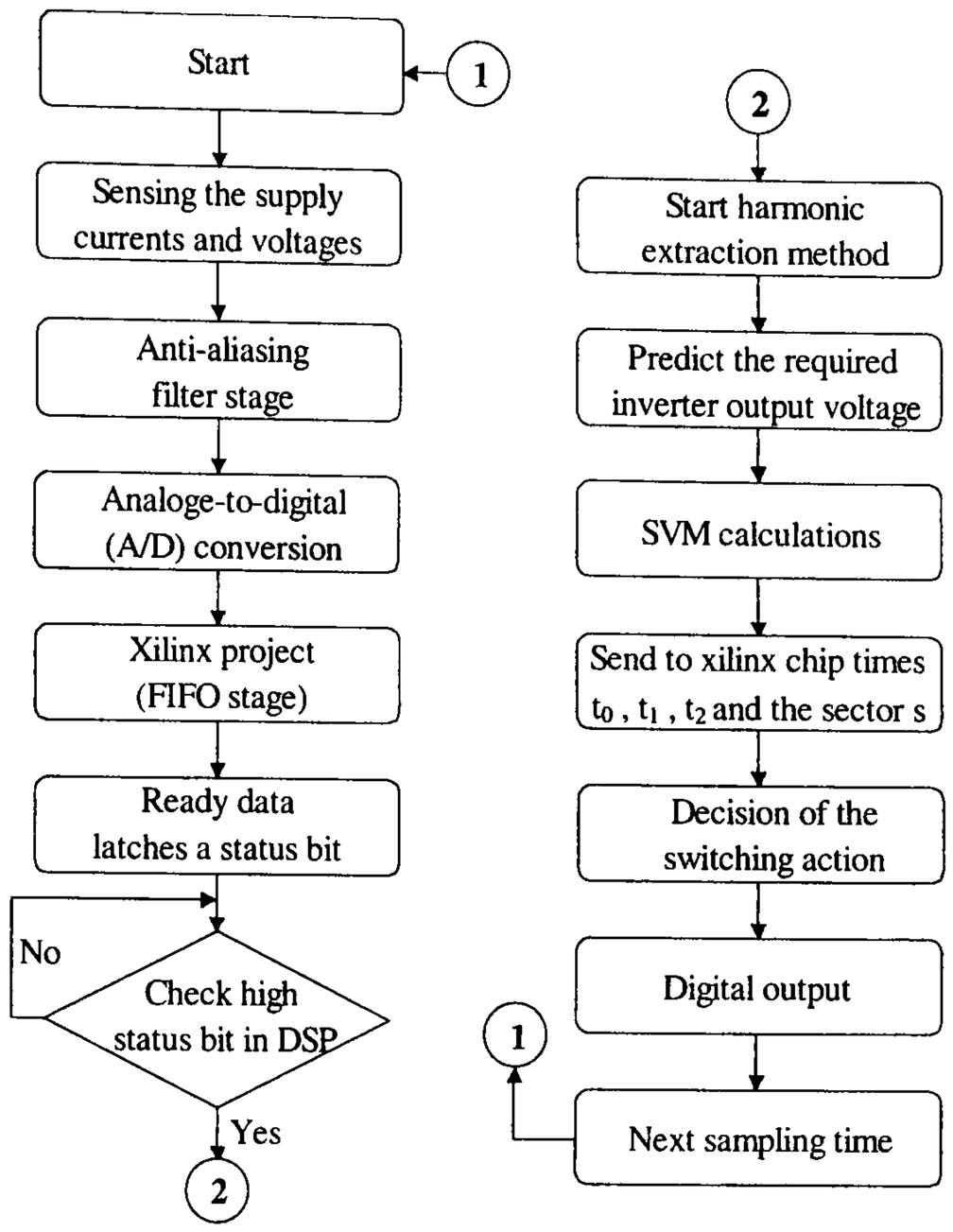

Figure 8.6. Practical system flow chart

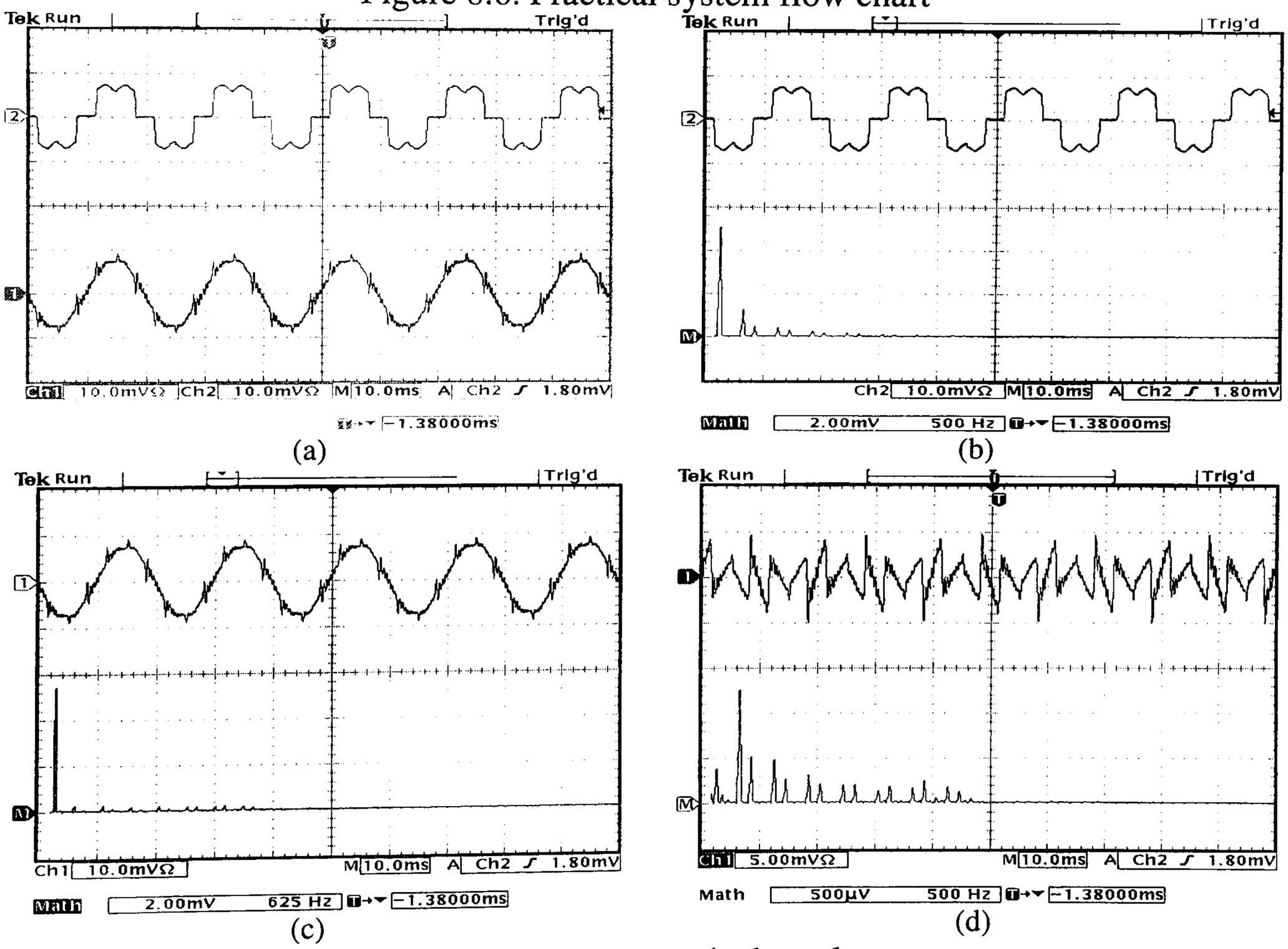

Figure 8.7. The practical results:
(a) the load and supply currents (5A/div), (b) the load current and its spectrum (5A/div), (c) the supply current and its spectrum (5A/div), and (d) the active filter current and its spectrum (2.5A/div)

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Chapter 9

Three-level Cascaded Shunt Active Power Filter

In this chapter, the three-level cascaded inverter is used as a shunt active power filter that utilizes multilevel inverter advantages of better total harmonic distortion, reduced semiconductor switch ratings, and reduced switching losses. The capacitor voltage control technique used in chapter eight as a harmonic current extraction technique is extended to the three-level shunt active power filter. Predictive current control based on the supply current (not the active filter current), as explained in chapter eight is used. Two space vector modulation (SVM) techniques, the normal three-level SVM and the three-level PS-SVM, are used. The proposed three-level shunt active power filter is validated by simulation using MATLAB/SIMULINK and practically with a laboratory prototype. Figure (9.1) shows the applicable single line diagram, while figure (9.2) shows the three-level shunt active filter circuit.

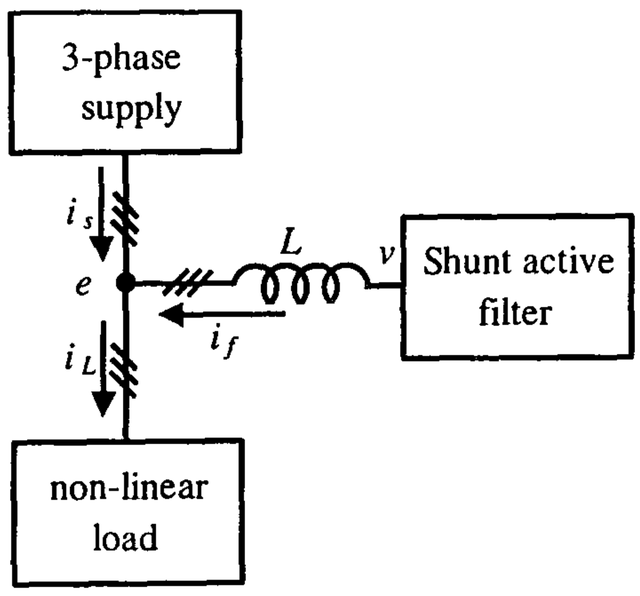


Figure 9.1. Shunt active power filter single line diagram

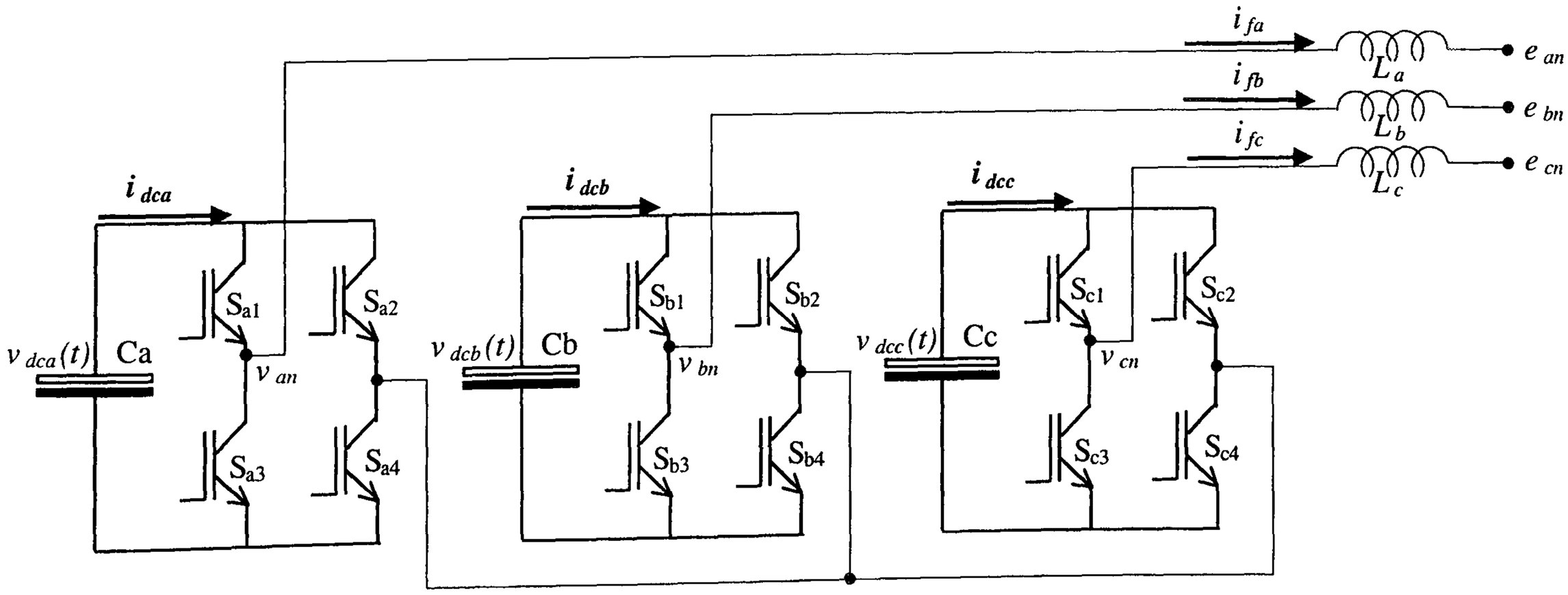


Figure 9.2. The three-level inverter used as a shunt active power filter

9.1 The proposed method

The harmonic current extraction technique and the current control technique are the two important sections of the shunt APF controller. The capacitor voltage control harmonic extraction technique [9.1]-[9.4] can be extended to the three-level APF. The innovative predictive current control discussed in chapter eight is implemented. Two three-level space vector modulation (SVM) techniques are used as a pulse width modulation (PWM) technique (normal three-level SVM discussed in chapter five and three-level PS-SVM discussed in chapter six). In addition to the advantages of using predictive current control (outlined in chapter eight), the proposed method has advantages such as; the number of sensors used is minimized (the measured quantities are the supply currents, PCC voltages, and the capacitor voltages), the reference currents are the supply currents instead of the active filter currents which gives good current tracking performance as the reference supply current is sinusoidal while the active filter current has significant harmonic components. Using a three-level inverter reduces the ratings of the semiconductor switches, improves total harmonic distortion, and reduces switching losses. Using three-level SVM as a PWM technique enables the inverter to compensate for the load harmonics and reactive current at a lower capacitor voltage because SVM gives an increase of 15% in gain, has the lowest THD, and a constant switching frequency [9.5].

Capacitor voltage control

Harmonic extraction is performed using the capacitor voltage control used in chapter eight [9.1]-[9.4] but extended to the three-level inverter. Figure (9.3) shows the proposed block diagram.

9.2 The APF simulation model

9.2.1 Three-level shunt active power filter state-space model

For the active power filter shown in figure (9.2), the three inverter output phase voltages are expressed as:

$$v_{x0}(t) = v_{dcx}(t).[s_{x1} - s_{x2}] \quad where\ x = a,\ b,\ or\ c \tag{9.1}$$

Assuming balanced supply voltages and equal interfacing inductances, the three inverter output line voltages are

$$\begin{aligned} v_{ab}(t) &= v_{dca}(t).[s_{a1} - s_{a2}] - v_{dcb}(t).[s_{b1} - s_{b2}] \\ v_{bc}(t) &= v_{dcb}(t).[s_{b1} - s_{b2}] - v_{dcc}(t).[s_{c1} - s_{c2}] \end{aligned} \tag{9.2}$$

$$v_{ca}(t) = v_{dcc}(t).[s_{c1} - s_{c2}] - v_{dca}(t).[s_{a1} - s_{a2}]$$

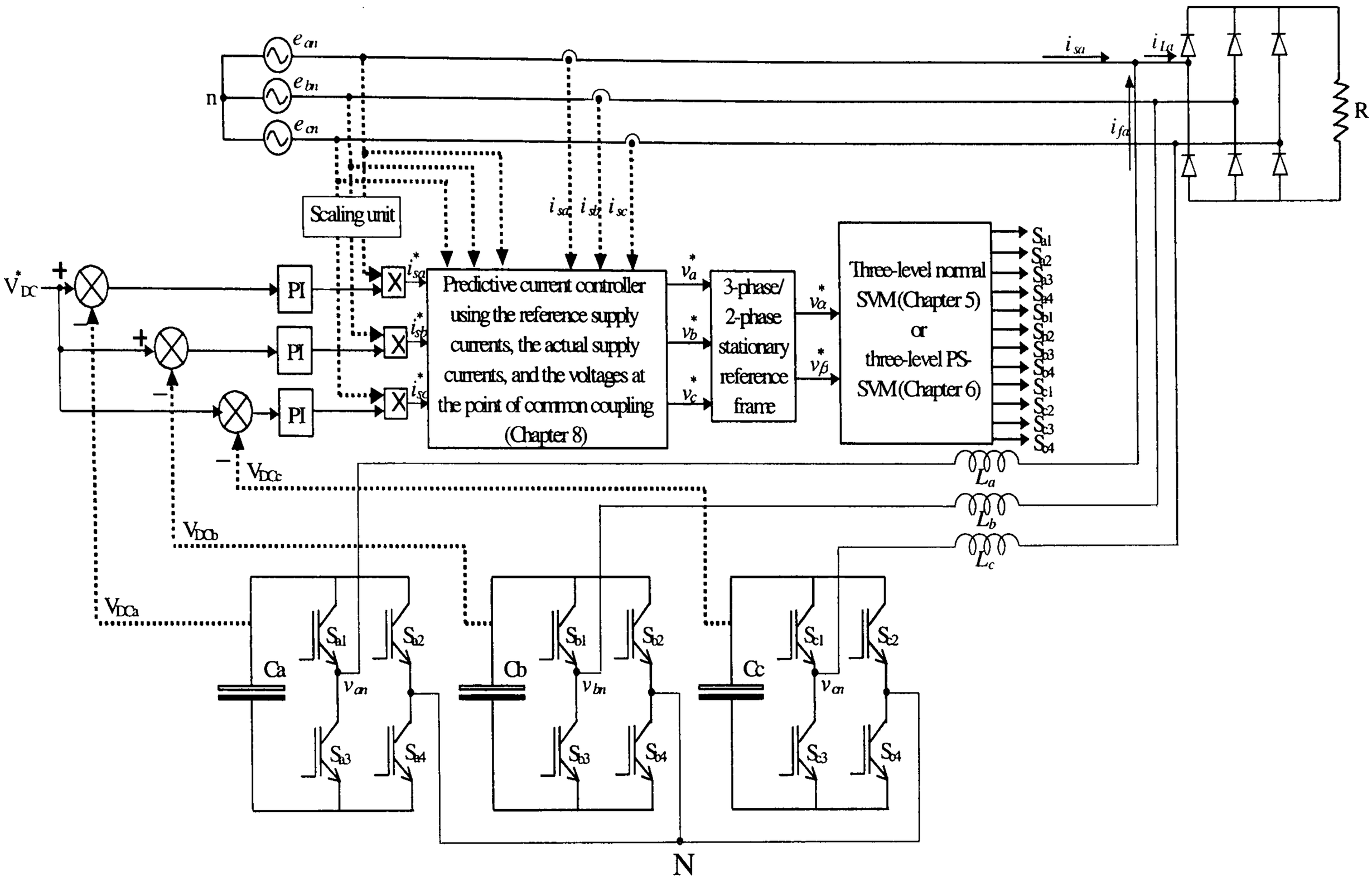


Figure 9.3. Block diagram of the proposed technique
(The dotted lines indicate the measured quantities)

The switching state is '1' for the on-state and '0' for the off-state. The switches in each leg are complementary. v_{dca}(t), v_{dcb}(t), and v_{dcc}(t) are the instantaneous capacitor voltages of the phases a, b, and c respectively. From equation (9.2), the phase-to-neutral voltages can be expressed as:

$$\begin{aligned} v_{an}(t) &= \tfrac{1}{3}\left(2.v_{dca}(t).[s_{a1} - s_{a2}] - v_{dcb}(t).[s_{b1} - s_{b2}] - v_{dcc}(t).[s_{c1} - s_{c2}]\right) \\ v_{bn}(t) &= \tfrac{1}{3}\left(2.v_{dcb}(t).[s_{b1} - s_{b2}] - v_{dca}(t).[s_{a1} - s_{a2}] - v_{dcc}(t).[s_{c1} - s_{c2}]\right) \\ v_{cn}(t) &= \tfrac{1}{3}\left(2.v_{dcc}(t).[s_{c1} - s_{c2}] - v_{dca}(t).[s_{a1} - s_{a2}] - v_{dcb}(t).[s_{b1} - s_{b2}]\right) \end{aligned} \tag{9.3}$$

The active filter currents are:

$$\begin{aligned} L\frac{di_{fa}(t)}{dt} &= v_{an}(t) - e_{an}(t) \\ L\frac{di_{fb}(t)}{dt} &= v_{bn}(t) - e_{bn}(t) \\ L\frac{di_{fc}(t)}{dt} &= v_{cn}(t) - e_{cn}(t) \end{aligned} \tag{9.4}$$

In equation (9.4), the interfacing inductor resistance is neglected. Substituting equation (9.3) into equation (9.4) yields

$$\begin{aligned}
L\frac{di_{fa}(t)}{dt} &= \tfrac{1}{3}\left(2.v_{dca}(t).[s_{a1}-s_{a2}]-v_{dcb}(t).[s_{b1}-s_{b2}]-v_{dcc}(t).[s_{c1}-s_{c2}]\right)-e_{an}(t)\\
L\frac{di_{fb}(t)}{dt} &= \tfrac{1}{3}\left(2.v_{dcb}(t).[s_{b1}-s_{b2}]-v_{dca}(t).[s_{a1}-s_{a2}]-v_{dcc}(t).[s_{c1}-s_{c2}]\right)-e_{bn}(t)\\
L\frac{di_{fc}(t)}{dt} &= \tfrac{1}{3}\left(2.v_{dcc}(t).[s_{c1}-s_{c2}]-v_{dca}(t).[s_{a1}-s_{a2}]-v_{dcb}(t).[s_{b1}-s_{b2}]\right)-e_{cn}(t)
\end{aligned} \tag{9.5}$$

Equation (9.5) shows three independent currents. In simulation, the three currents must be checked to sum to zero. Equation (9.5) cannot be used for either unbalanced supply voltages or unequal interfacing inductances. The three capacitor currents can be expressed in terms of the filter currents i_{fa}, i_{fb} and i_{fc} as:

$$i_{dcx}(t) = [s_{x1}-s_{x2}]i_{fx}(t) \tag{9.6}$$

The three capacitor voltages are

$$i_{dcx}(t) = -C_x.\frac{dv_{dcx}(t)}{dt} \tag{9.7}$$

Substituting equation (9.6) into equation (9.7) yields

$$-C_x.\frac{dv_{dcx}(t)}{dt} = [s_{x1}-s_{x2}]i_{fx}(t) \tag{9.8}$$

Equations (9.5) and (9.8) represent the state-space model in the form

$$\dot{X} = A.X + B.U \tag{9.9}$$

where A, X , B, and U are defined as

$$A = \begin{bmatrix}
0 & 0 & 0 & \frac{2(s_{a1}-s_{a2})}{3L} & \frac{(s_{b2}-s_{b1})}{3L} & \frac{(s_{c2}-s_{c1})}{3L}\\
0 & 0 & 0 & \frac{(s_{a2}-s_{a1})}{3L} & \frac{2(s_{b1}-s_{b2})}{3L} & \frac{(s_{c2}-s_{c1})}{3L}\\
0 & 0 & 0 & \frac{(s_{a2}-s_{a1})}{3L} & \frac{(s_{b2}-s_{b1})}{3L} & \frac{2(s_{c1}-s_{c2})}{3L}\\
\frac{(s_{a2}-s_{a1})}{C_a} & 0 & 0 & 0 & 0 & 0\\
0 & \frac{(s_{b2}-s_{b1})}{C_b} & 0 & 0 & 0 & 0\\
0 & 0 & \frac{(s_{c2}-s_{c1})}{C_c} & 0 & 0 & 0
\end{bmatrix}$$

$$\mathrm{X} = \begin{bmatrix} i_{fa}(t) \\ i_{fb}(t) \\ i_{fc}(t) \\ v_{dca}(t) \\ v_{dcb}(t) \\ v_{dcc}(t) \end{bmatrix}, \ \mathrm{B} = \begin{bmatrix} \frac{-1}{L} & 0 & 0 \\ 0 & \frac{-1}{L} & 0 \\ 0 & 0 & \frac{-1}{L} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \text{ and } U = \begin{bmatrix} e_{an}(t) \\ e_{bn}(t) \\ e_{cn}(t) \end{bmatrix}$$

9.2.2 Simulation results

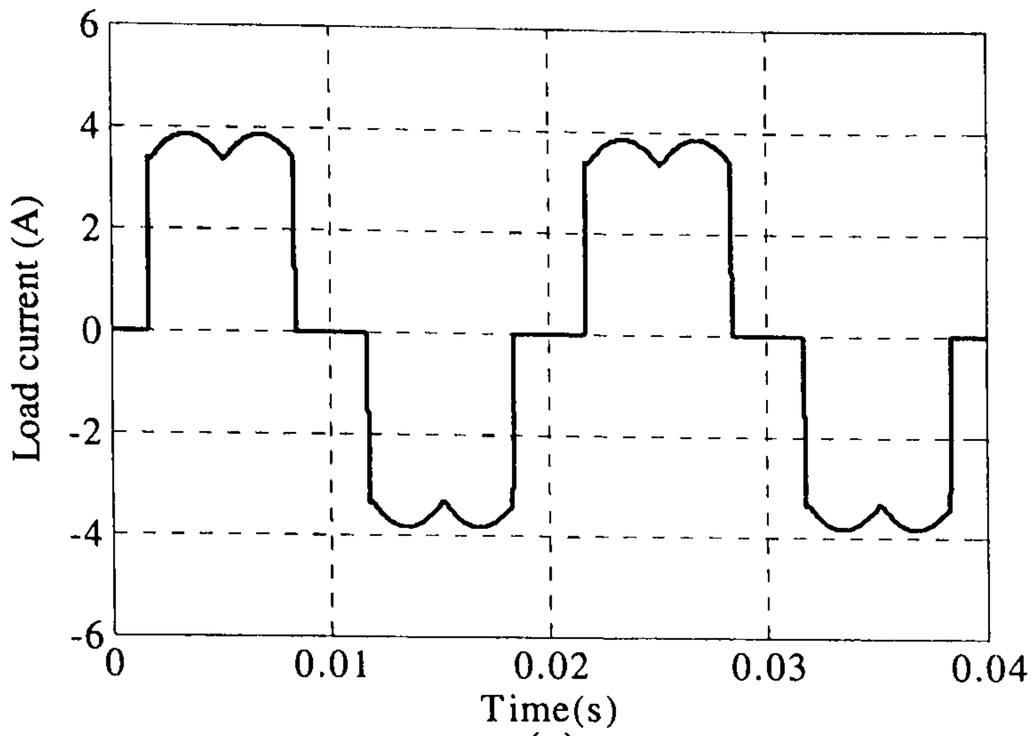
Steady state simulations

The state-space model of the active filter presented in section (9.2.1) is simulated using Matlab/Simulink (see Appendix H.2). Normal three-level SVM is extracted from the generalized approach discussed in chapter five and is programmed using an m-file with an s-function block in Simulink while the three-level PS-SVM is programmed using two m-files with two s-function blocks in Simulink, as in chapter six. The parameters used in simulation (and also practically) are shown in Table 9.1. The nonlinear load is a three-phase uncontrolled bridge rectifier feeding a 70 Ohm resistive load. The sampling frequency is adjusted in simulation to be the same as used practically.

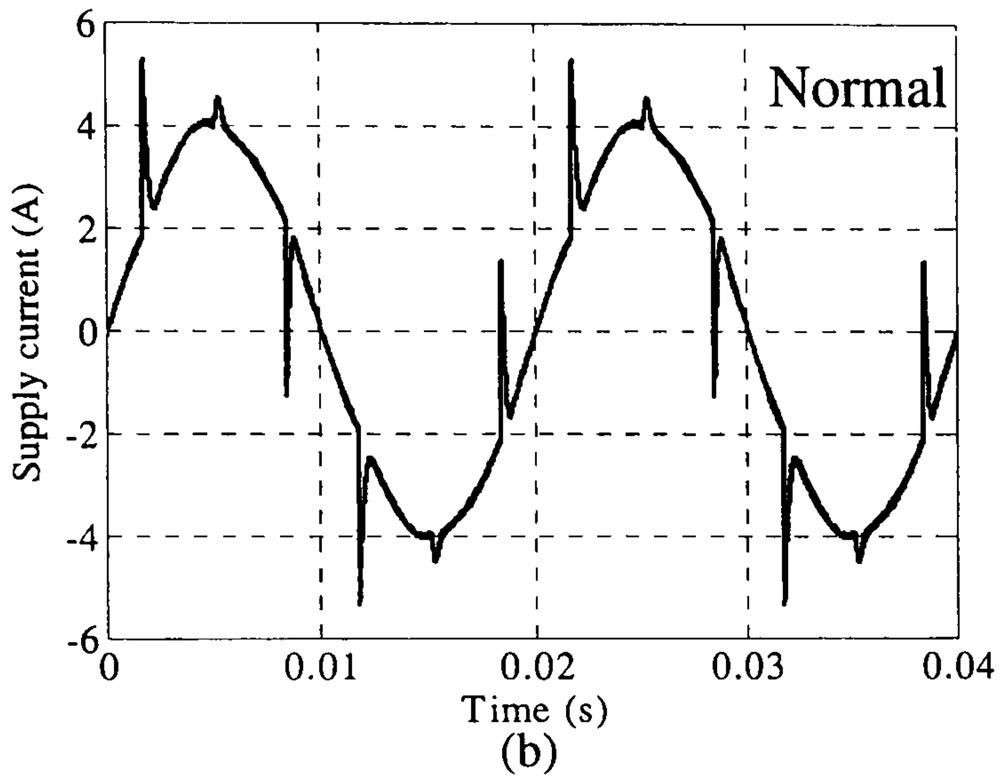
Table 9.1. The three-level APF system parameters

V_{DC}^{*}	160	V
Supply voltage	110	V
C_a, C_b, and C_c	220	μF
L_a, L_b, and L_c	10	mH
Sampling frequency	24.42	kHz
Switching frequency	12.21	kHz

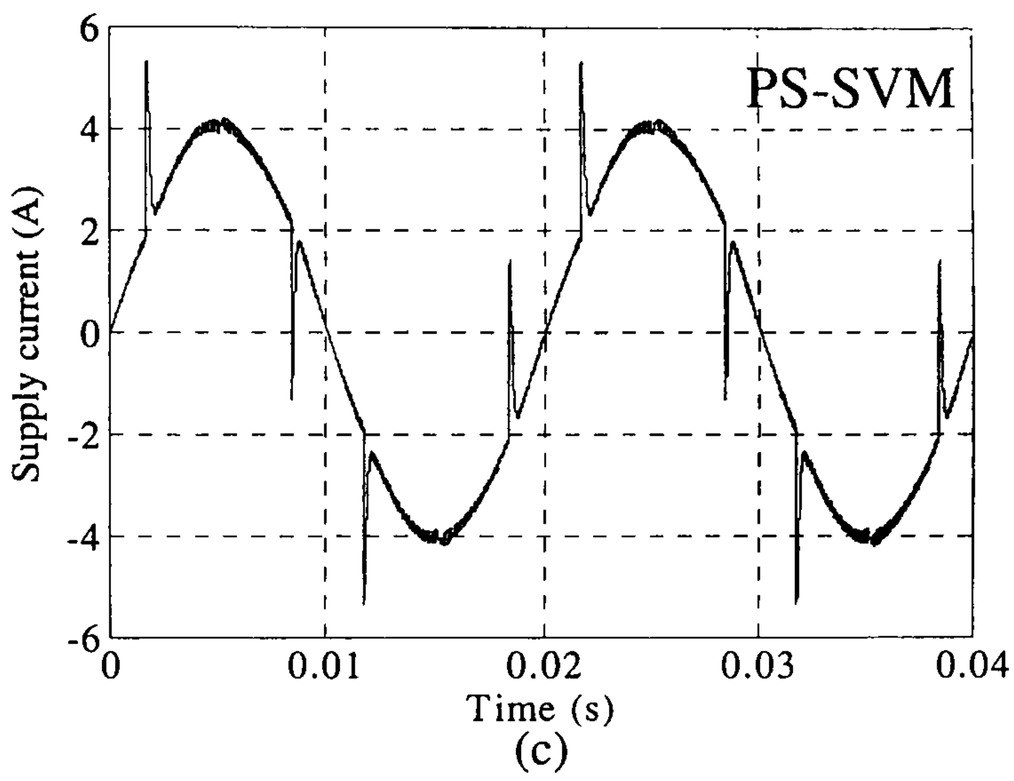
Figure (9.4a) shows the load current in one phase. Parts b and c show the supply current using normal and PS-SVM respectively. Parts d and e of figure (9.4) show the active filter current for each modulation method. Parts f and g show the capacitor voltages while parts h to k show the line voltage and its power spectrum for each modulation method. It is clear from parts j and k that the harmonics concentrate at 12 kHz and its multiples in normal three-level SVM, and at 24 kHz and its multiples in PS-SVM.


Load current (A)
Time(s)

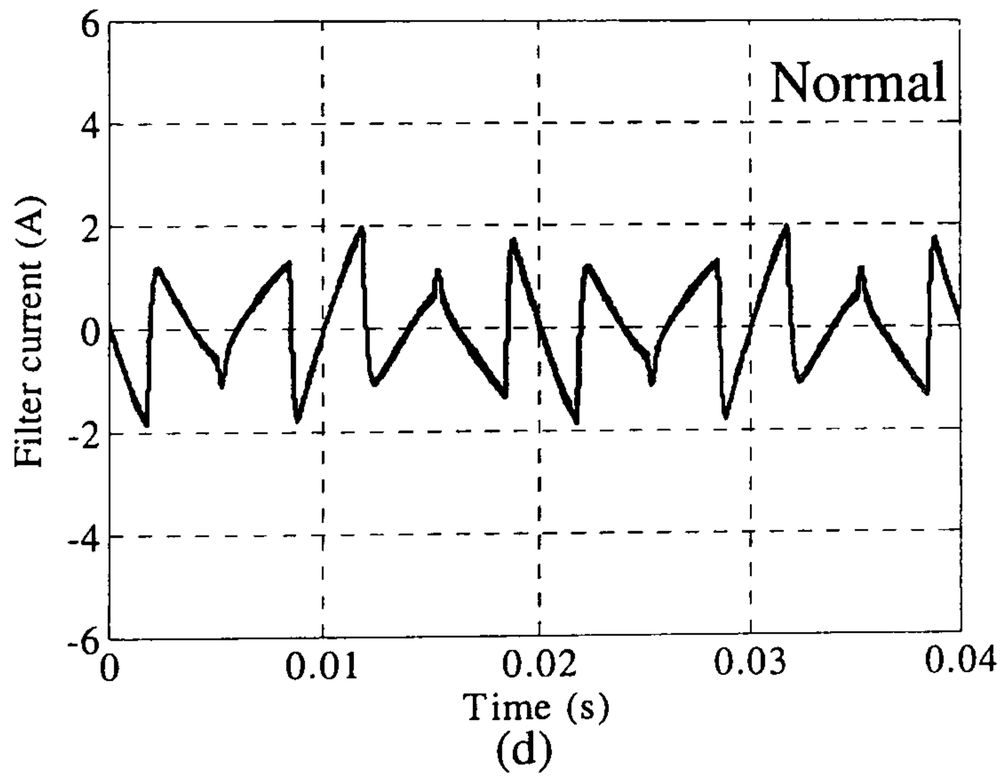
(a)


Normal
Supply current (A)
Time (s)

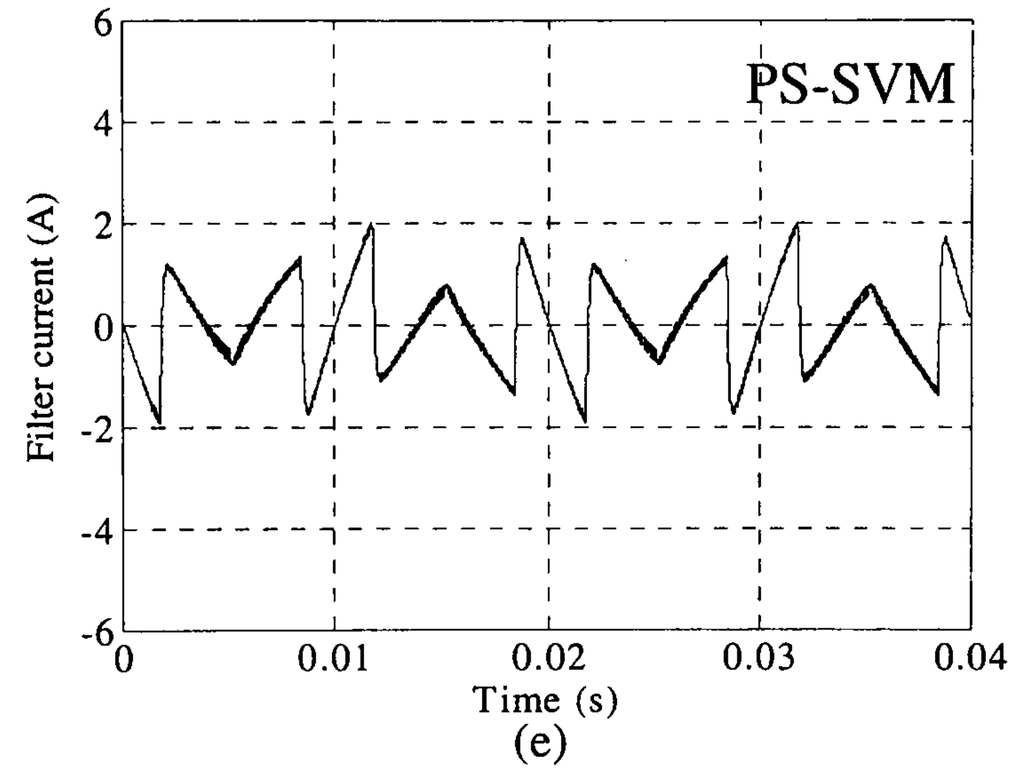
(b)


PS-SVM
Supply current (A)
Time (s)

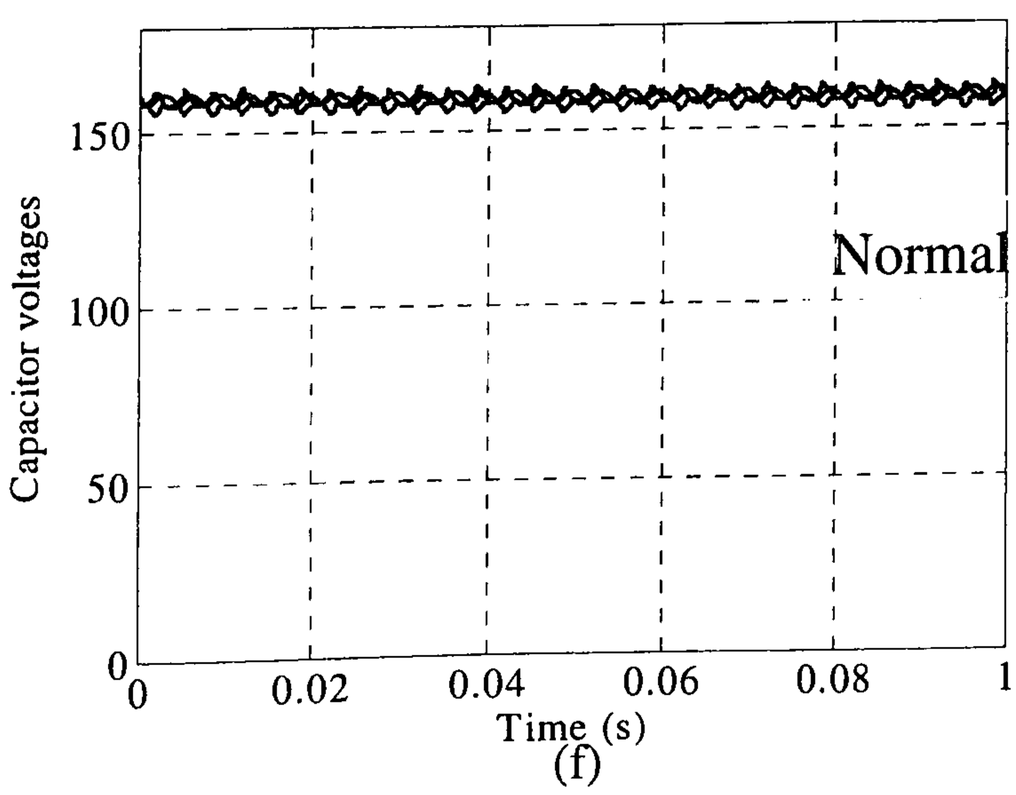
(c)


Normal
Filter current (A)
Time (s)

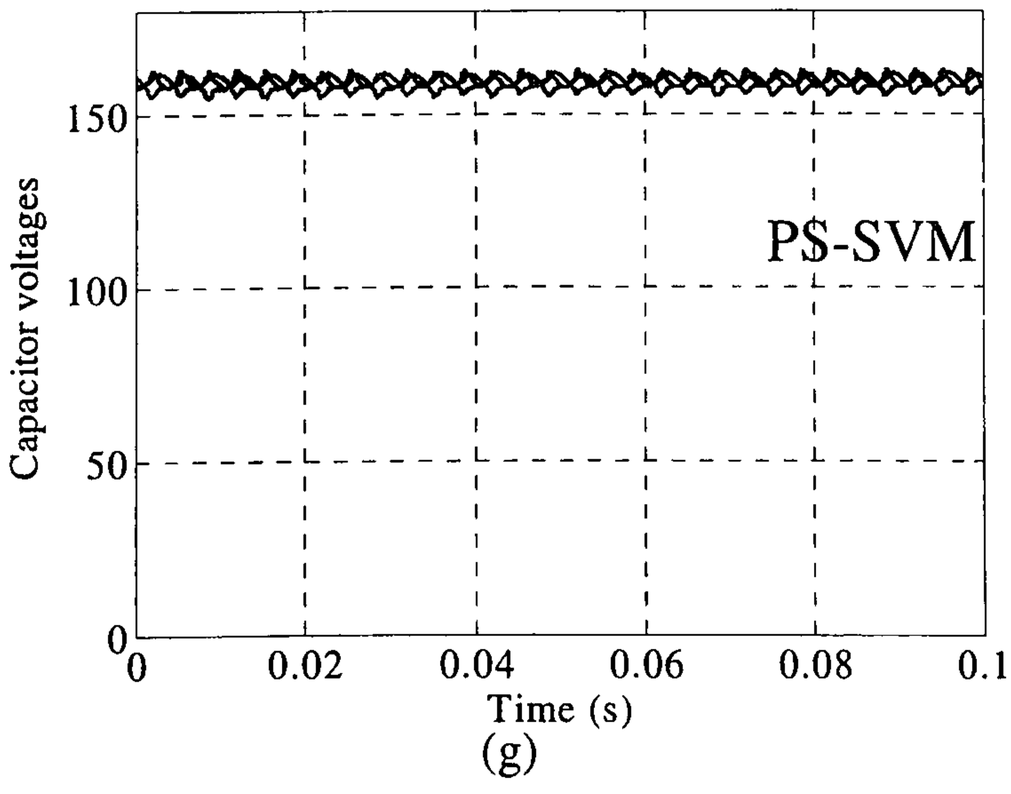
(d)


PS-SVM
Filter current (A)
Time (s)

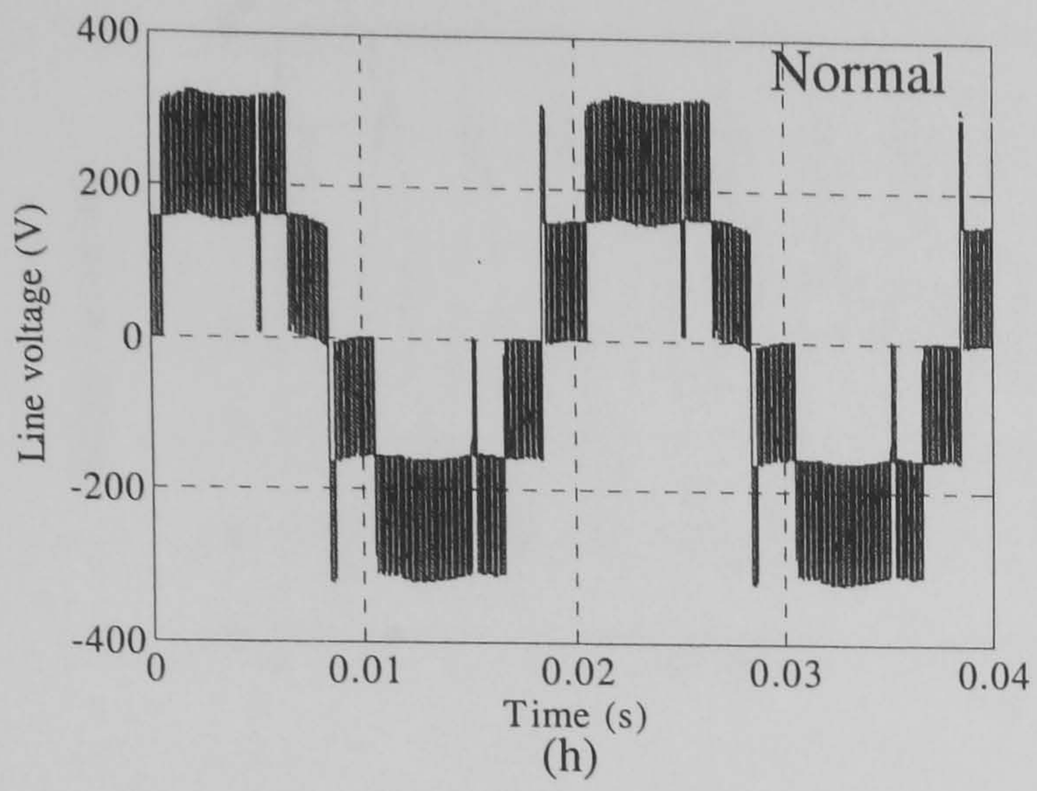
(e)

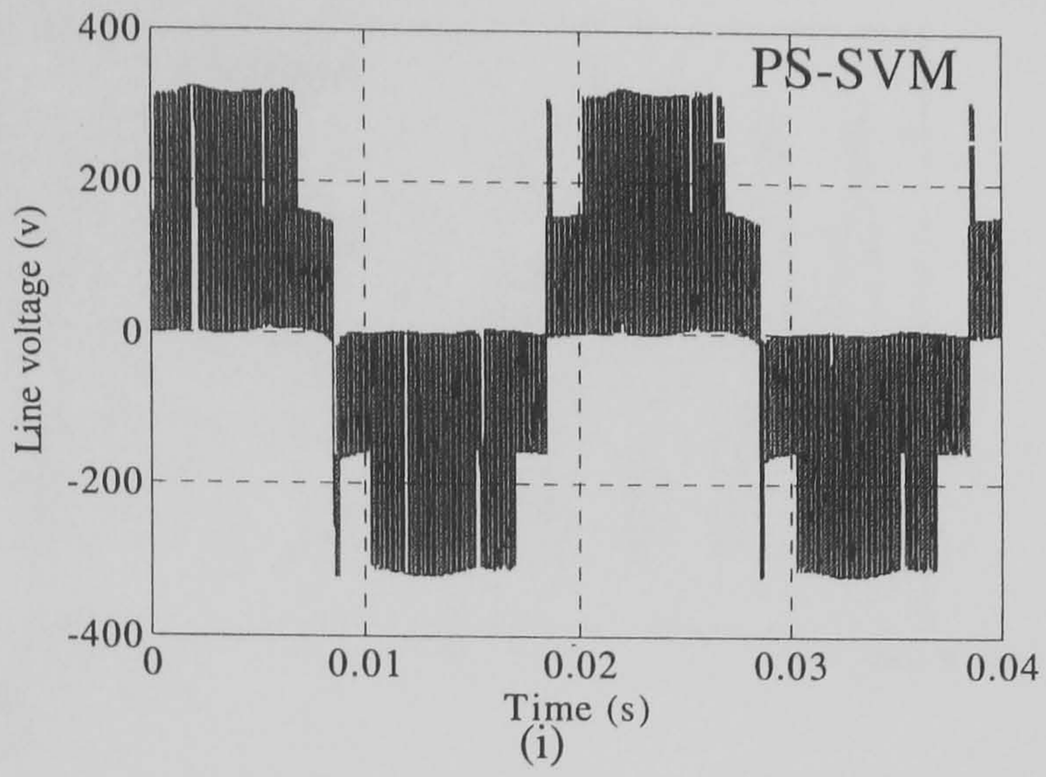

Normal
Capacitor voltages
Time (s)

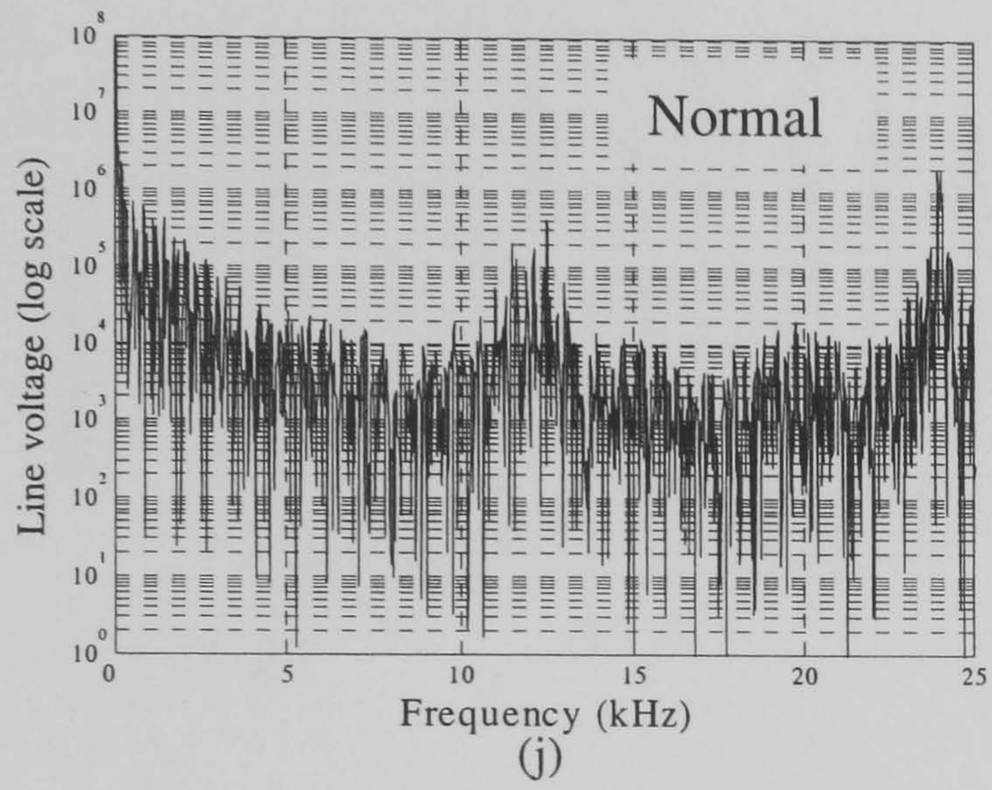
(f)


PS-SVM
Capacitor voltages
Time (s)

(g)







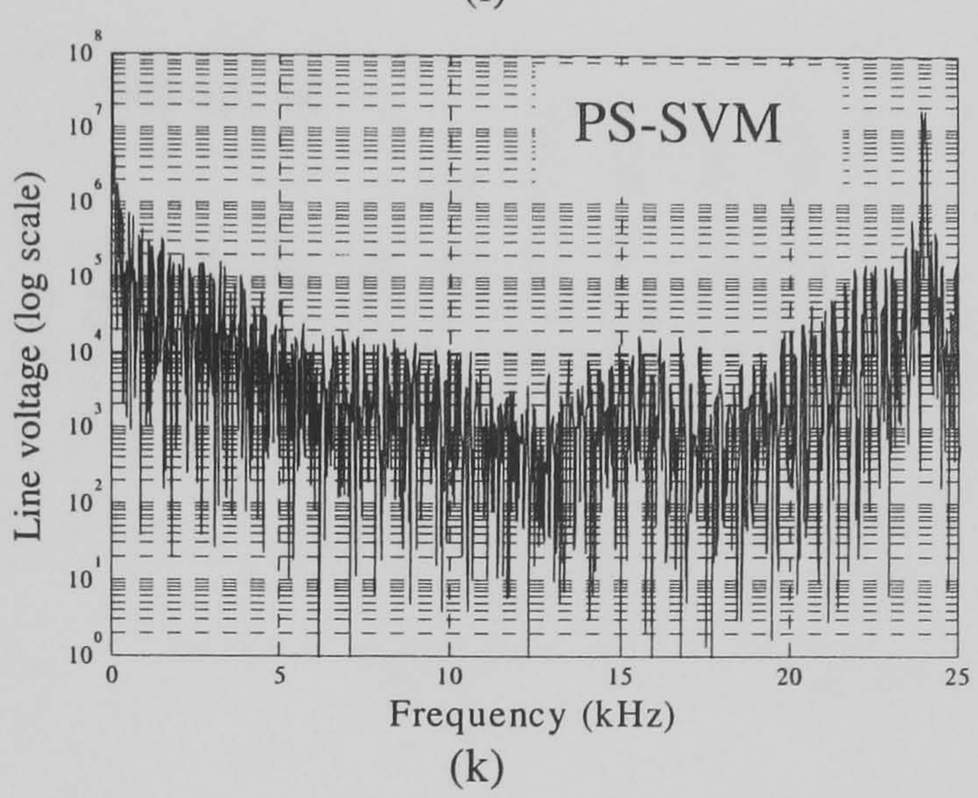


Figure 9.4. Simulation results:
(a) load current, (b) supply current for normal SVM, (c) supply current for PS-SVM, (d) active filter current for normal SVM, (e) active filter current for PS-SVM, (f) capacitor voltages for normal SVM, (g) capacitor voltages for PS-SVM, (h) inverter output line voltage for normal SVM and (j) its power spectrum , (i) inverter output line voltage for PS-SVM, and (k) its power spectrum

Transient simulations

Parts a and b of figure (9.5) show supply current transient responses for both normal SVM and PS-SVM respectively at start up and when the non-linear load resistance is increased from 70 to 140 Ohm in the period 0.2 to 0.3 seconds. Parts c and d of figure (9.5) show the transient response of the three capacitor voltages in each modulation case, under the same conditions as in parts a and b. It can be concluded that the capacitor voltages take 40 ms (2 cycles) to reach the reference voltage at start up and takes 20 ms (one cycle) to reach the reference voltage after a load change for both PWM techniques. These times are mainly dependent on the PI controller parameters and the capacitance, as will be discussed in detail in the following section.

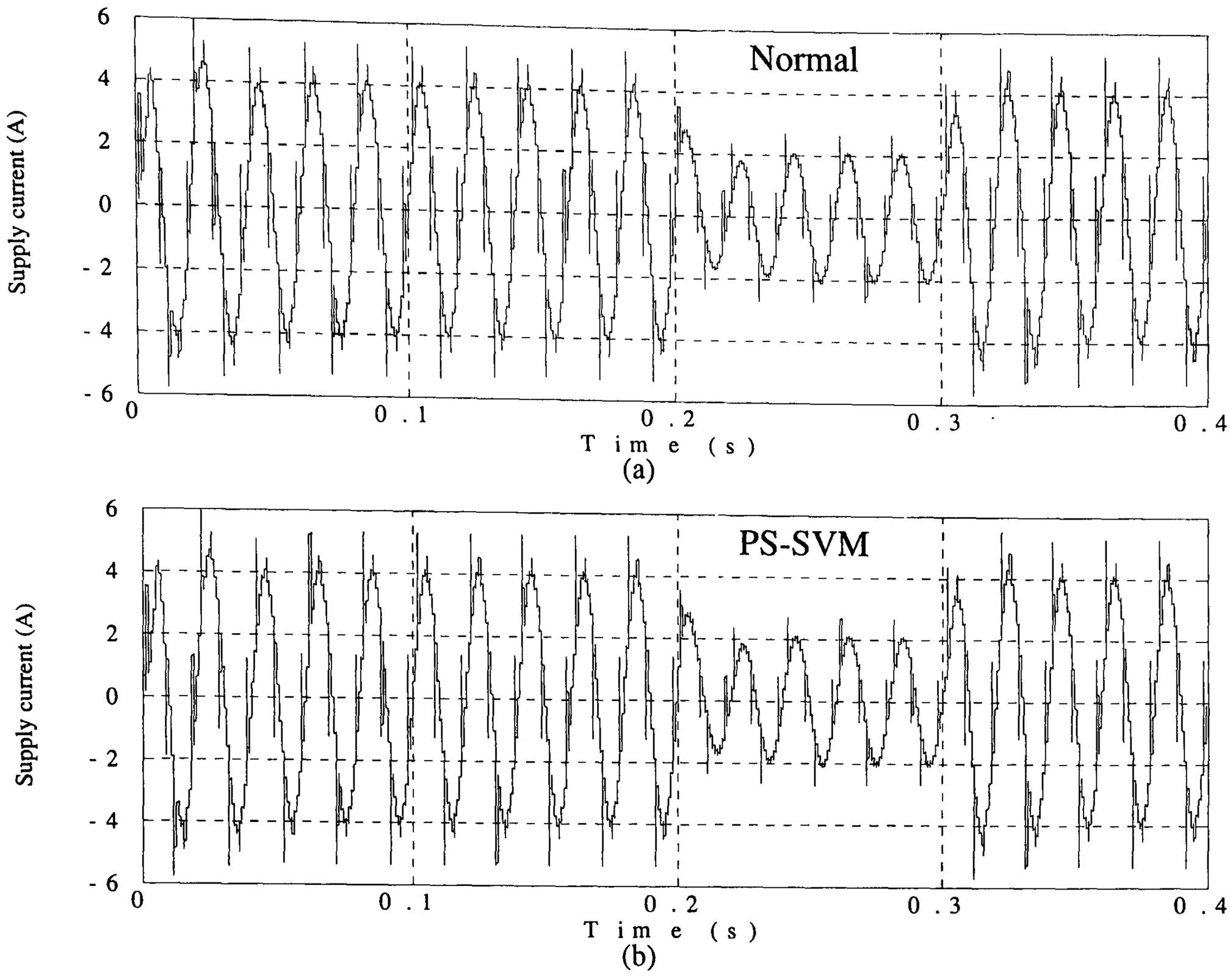


Figure 9.5. The transient response at starting and for load decrease of 50% (for the period 0.2-0.3 s):
(a) supply current for normal SVM, (b) supply current for PS-SVM, (c) capacitor voltages for normal SVM, and (d) capacitor voltages for PS-SVM

9.2.3 System performance

Three terms will be defined as performance indices. These performance indices are related to voltage and time terms, as this application is directed to the medium voltage level where these factors are vital. These terms are defined as in figure (9.6):

1. Maximum overshoot is the maximum increase in capacitor voltage as a ratio of the reference voltage when the load current is decreased by 50%, (V_{max}).
2. Restoration time is the time taken for the capacitor voltage to reach the reference voltage due to a 50% load current reduction, (t_r).
3. Voltage ripple is the voltage variation in steady-state for full-load operation as a ratio of the reference capacitor voltage, (ΔV_c).

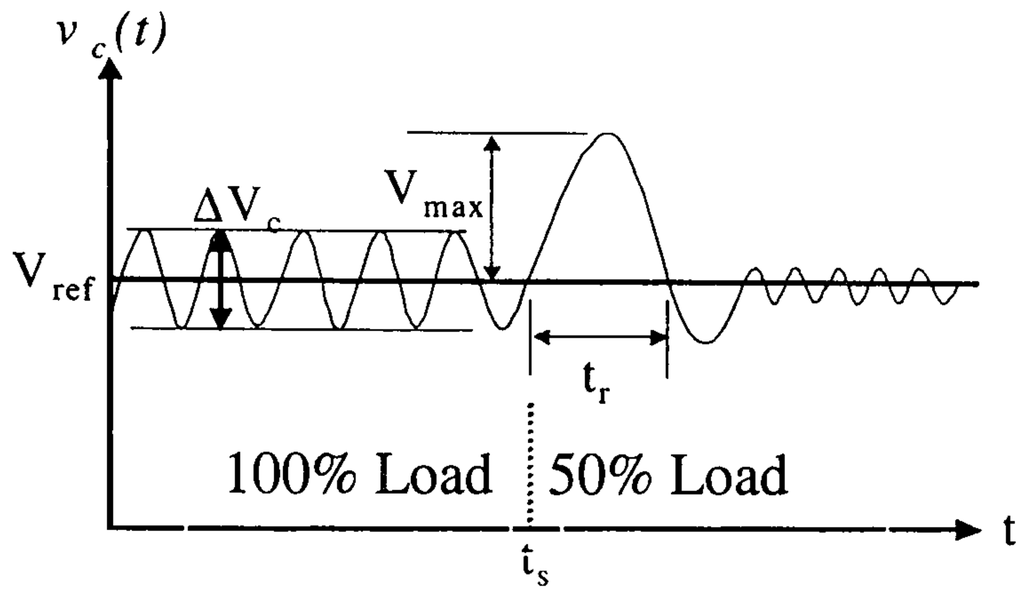


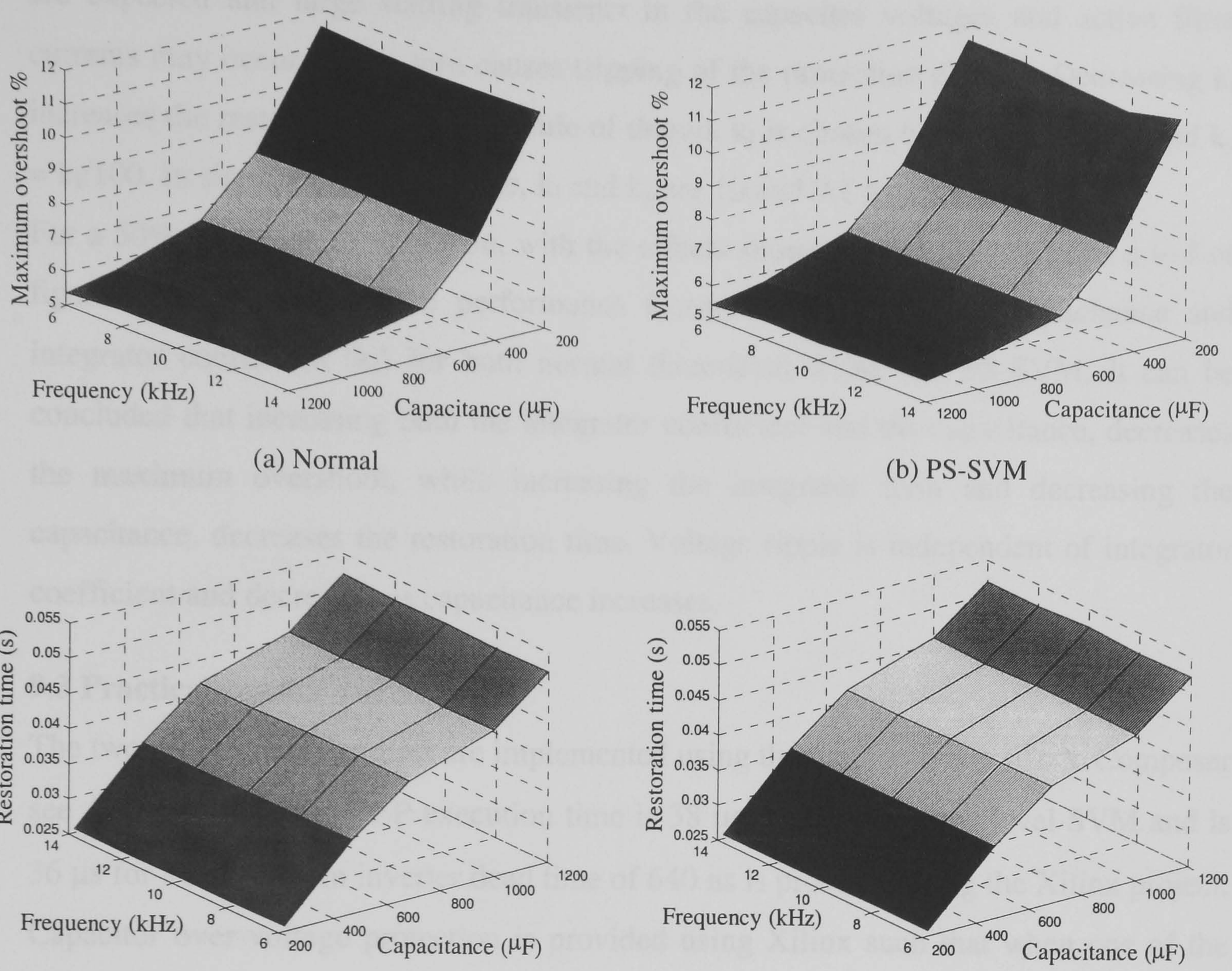
Figure 9.6. Definition of performance indices

Better shunt active power filter performance can be obtained by increasing the switching frequency, sampling frequency, and capacitance but there are limitations.

i. Increasing the switching frequency increases the semiconductor switching losses.
ii. The sampling frequency depends on the execution time of the control algorithm.
iii. Increasing capacitance increases the size and cost of the capacitors.

Therefore the lowest capacitance and switching frequency for acceptable filtering operation (to meet the IEEE-519 standards) is the main goal.

As a function of capacitance and switching frequency (the sampling frequency is assumed to be equal to the switching frequency), parts a and b of figure (9.7) show the maximum overshoot, parts c and d show the restoration time, while parts e and f show the voltage ripple for normal three-level SVM and PS-SVM in each case, respectively. It can be concluded that the switching frequency does not affect the three performance measures. Also increasing the capacitance increases the restoration time and reduces the maximum overshoot and voltage ripple.



(a) Normal (b) PS-SVM

(c) Normal (d) PS-SVM

(e) Normal (f) PS-SVM

Figure 9.7. The effect of the switching frequency and capacitance on: (a) maximum overshoot using normal SVM, (b) maximum overshoot using PS-SVM, (c) restoration time using normal SVM, (d) restoration time using PS-SVM, (e) voltage ripple using normal SVM, and (f) voltage ripple using PS-SVM

9.2.4 Proportional-integral (PI) controller design

Three identical PI controllers are used for capacitor voltage control. Increasing the proportional term (k_p) increases the noise pick-up which in turn degrades reference current extraction. Increasing the integrator term (k_I) improves the reference current waveform but for higher k_I, under damped oscillations for a sudden load current change

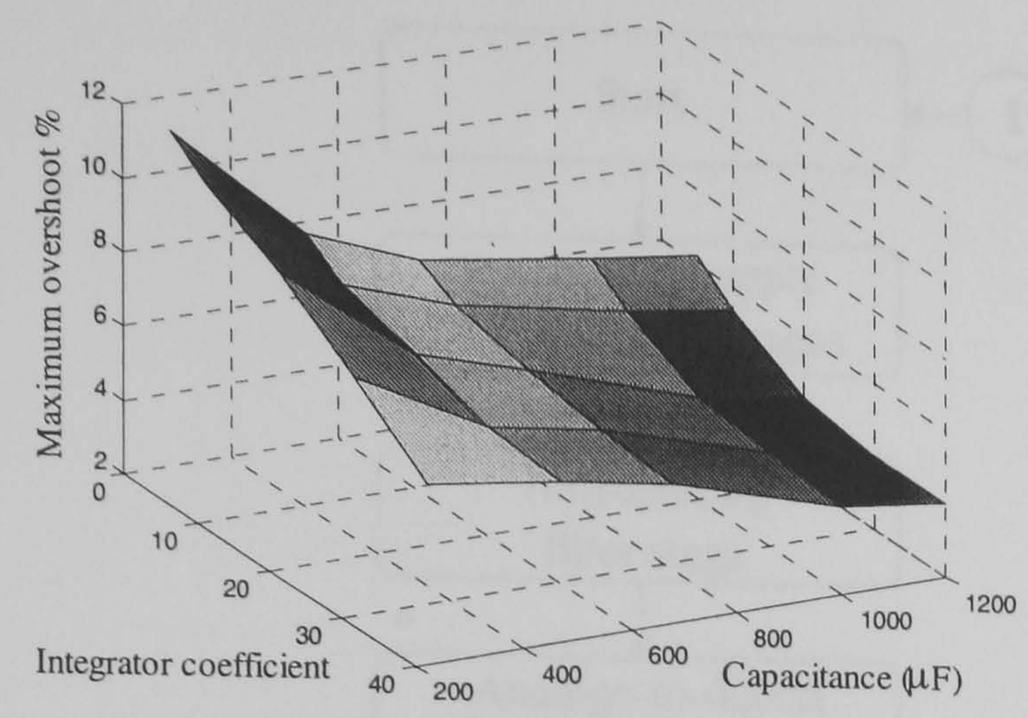
are expected and large starting transients in the capacitor voltages and active filter currents may occur that in turn causes tripping of the protection devices. Decreasing k_I increases the restoration time. As a rule of thumb, k_I is chosen between 5 and 20 and $k_p = k_I/100$. In simulation and practice, k_I and k_p are 10 and 0.1 respectively.

For a 50% load current reduction, with the effects shown in figure (9.5), parts a to f of figure (9.8) show the three performance factors as a function of capacitance and integrator coefficient (k_I) for both normal three-level SVM and PS-SVM. It can be concluded that increasing both the integrator coefficient and the capacitance, decreases the maximum overshoot, while increasing the integrator term and decreasing the capacitance, decreases the restoration time. Voltage ripple is independent of integrator coefficient and decreases as capacitance increases.

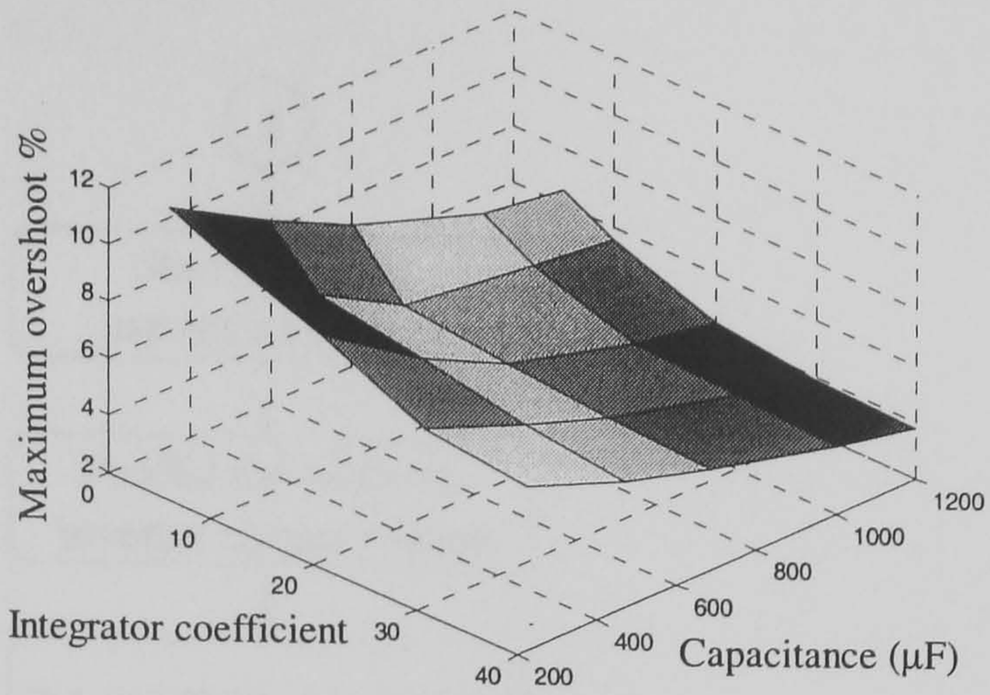
9.3 Practical results

The two proposed algorithms are implemented using the DSP software (Code Composer see Appendix E). The DSP execution time is 38 μs for normal three-level SVM and is 36 μs for PS-SVM. An inverter dead time of 640 ns is provided using the Xilinx project. Capacitor over-voltage protection is provided using Xilinx such that when one of the three capacitors is over charged, all 12 inverter switches are commutated. Figure (9.9) shows the flow chart procedure for the practical system.

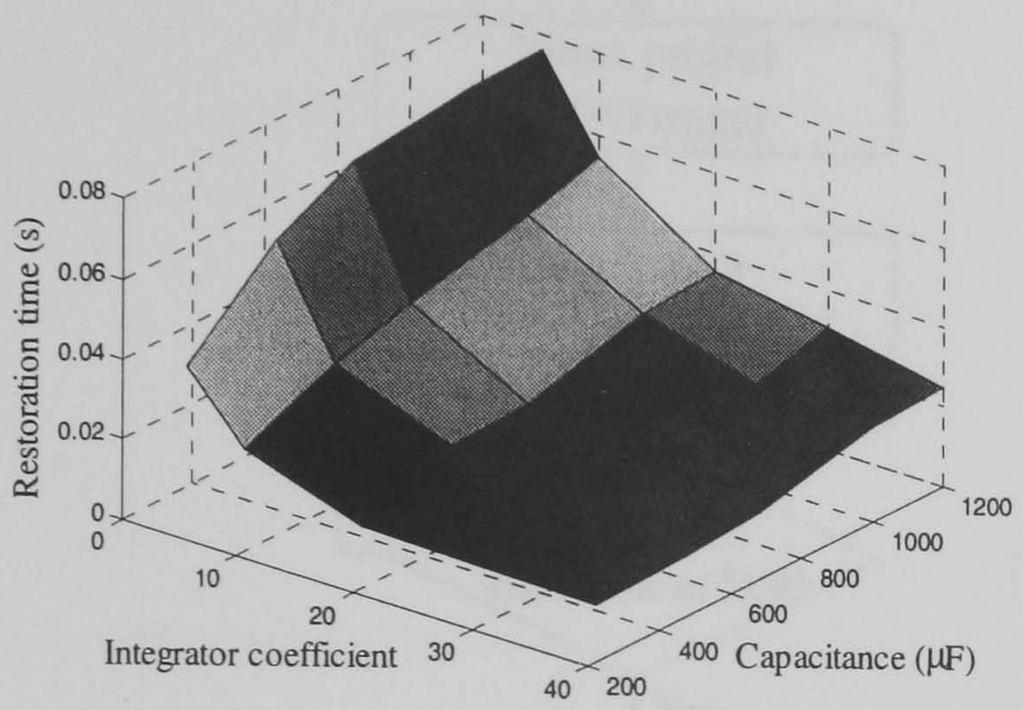
Figure (9.10a) shows the load current and its spectrum. Parts b and c of figure (9.10) show the supply current and its spectrum using normal SVM and PS-SVM respectively. Parts d and e show the active filter current and its spectrum for both modulation schemes. Parts f and g show the capacitor voltages in each modulation case while parts h and i show the line voltage and its spectrum for normal SVM and PS-SVM respectively. It is clear from the parts of figure (9.10) that the voltage harmonic spectrum in the case of PS-SVM appears at 24 kHz and its multiples, while it appears at 12 kHz for normal SVM, which agrees with the simulation results. See appendices G.1. and G.2 for R-L and R-C loads.



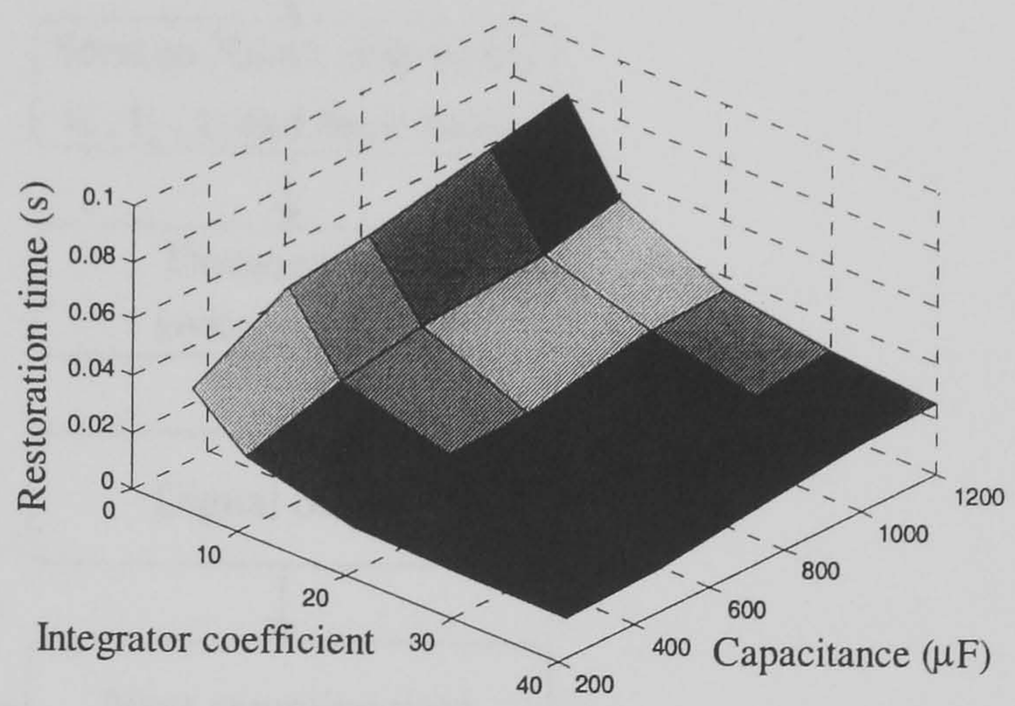
(a) Normal



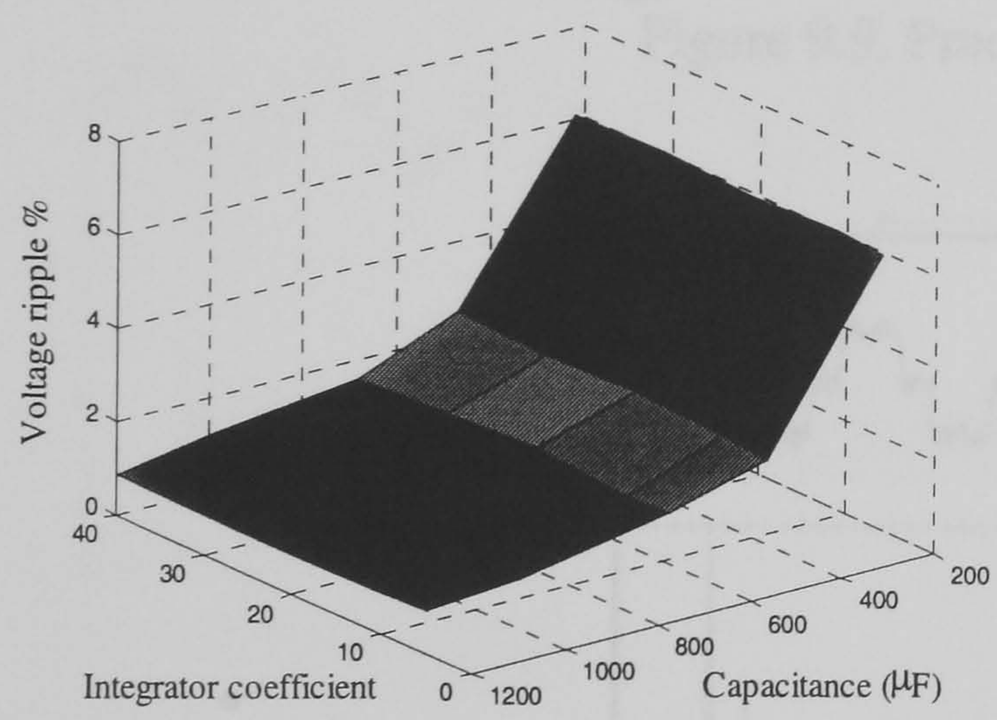
(b) PS-SVM



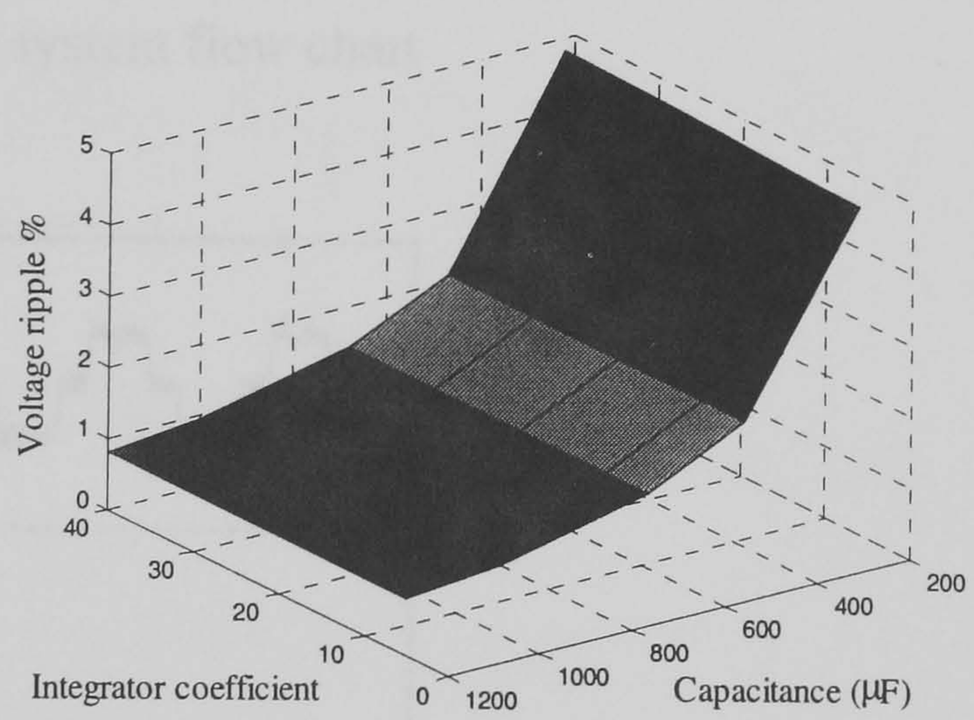
(c) Normal



(d) PS-SVM



(e) Normal



(f) PS-SVM

Figure 9.8. The effect of the integrator coefficient and capacitance on: (a) maximum overshoot using normal SVM, (b) maximum overshoot using PS-SVM, (c) restoration time using normal SVM, (d) restoration time using PS-SVM, (e) voltage ripple using normal SVM, and (f) voltage ripple using PS-SVM

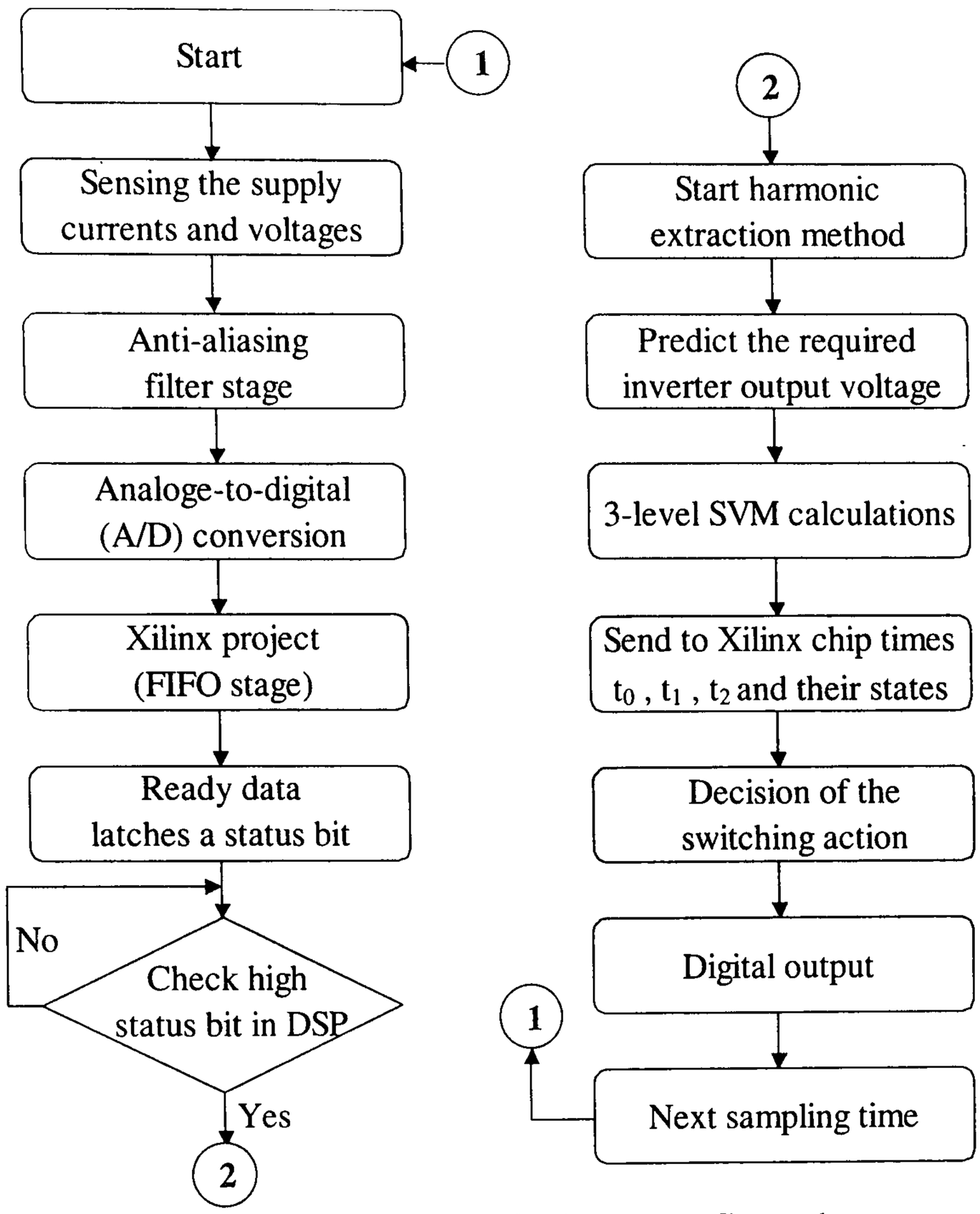
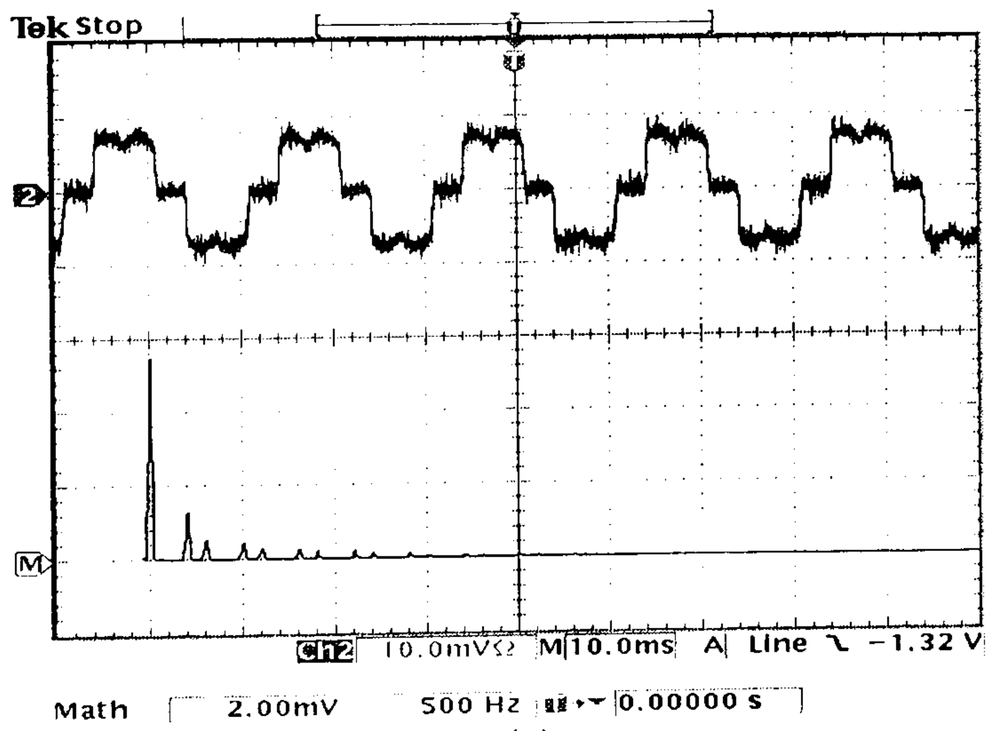
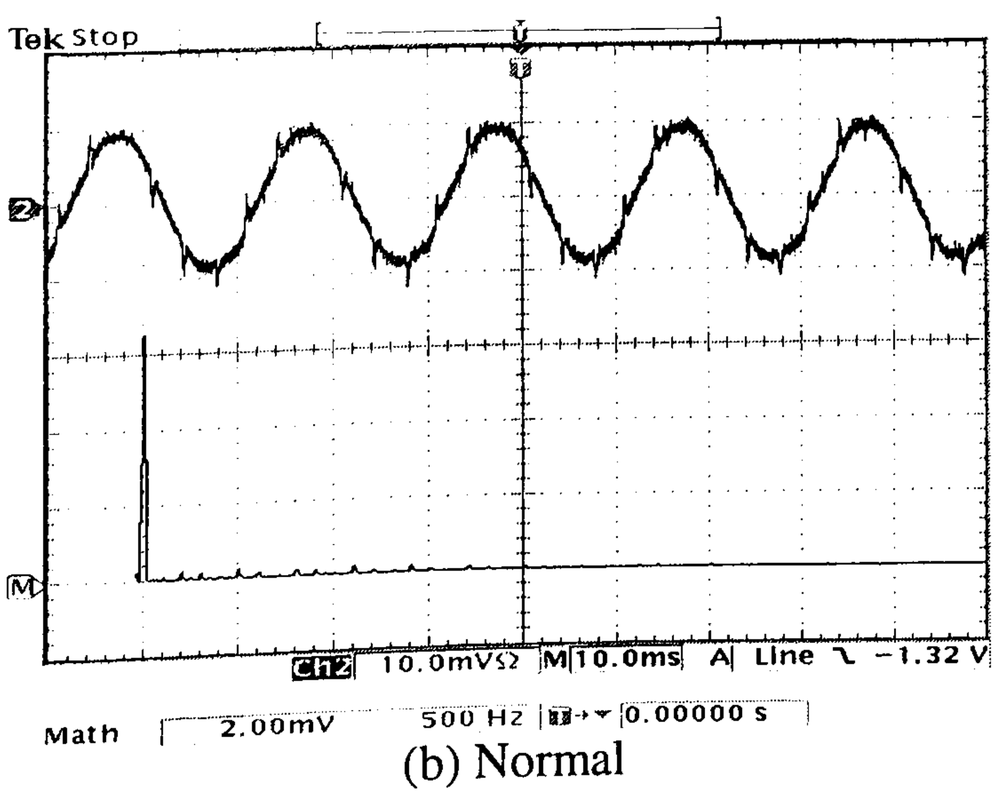


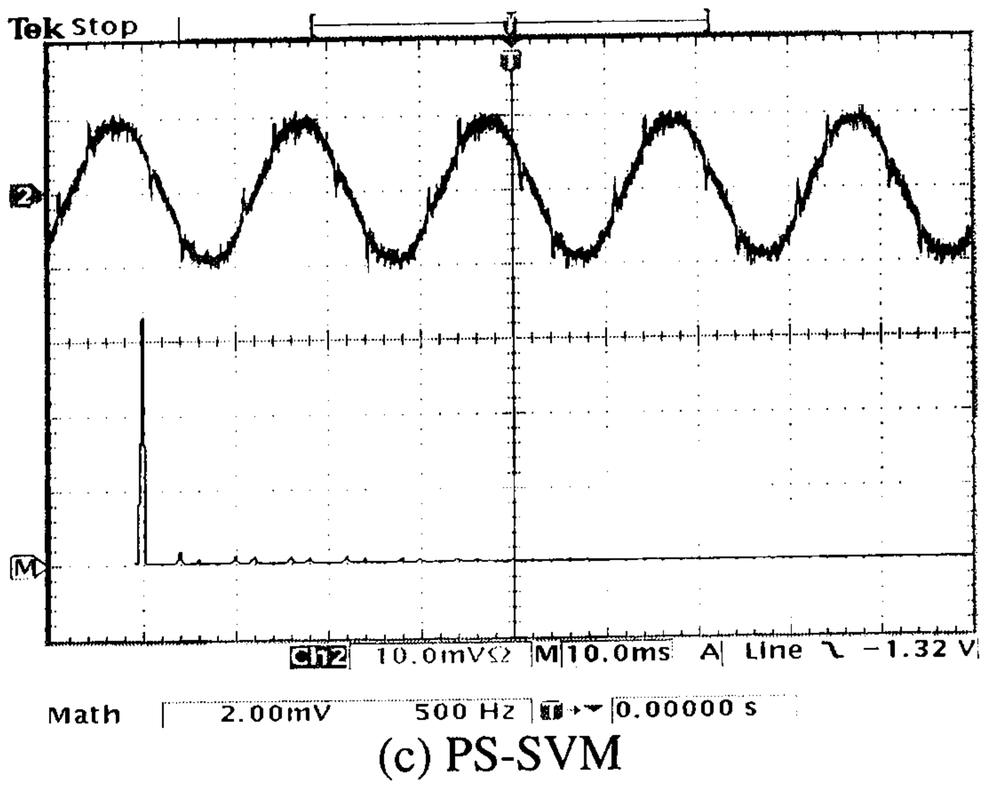
Figure 9.9. Practical system flow chart



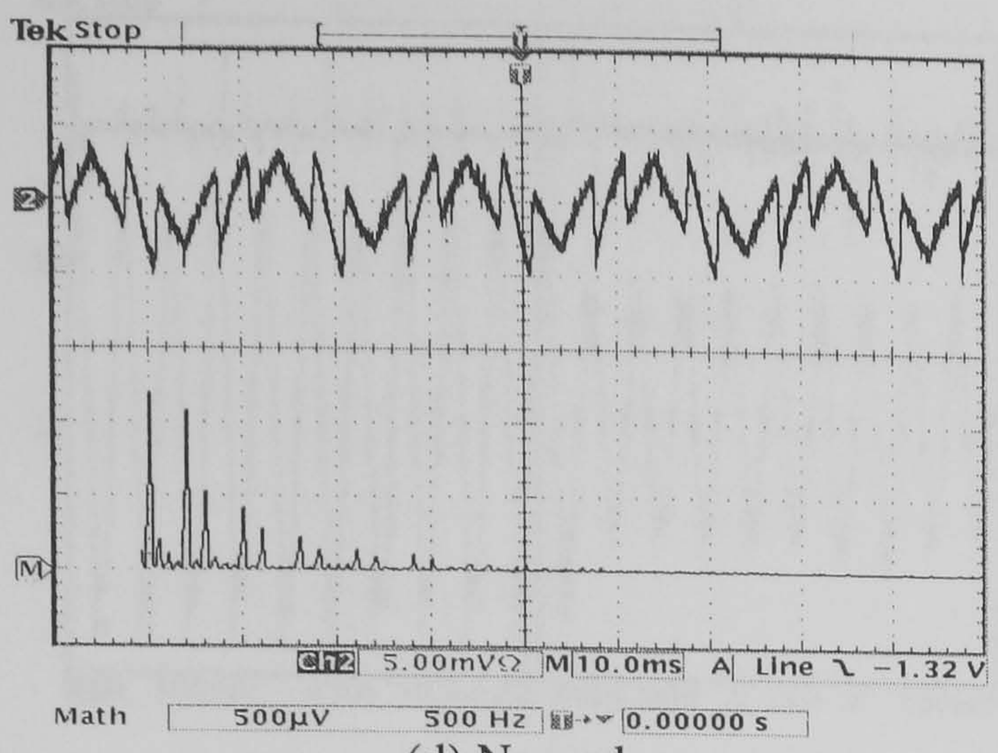
(a)



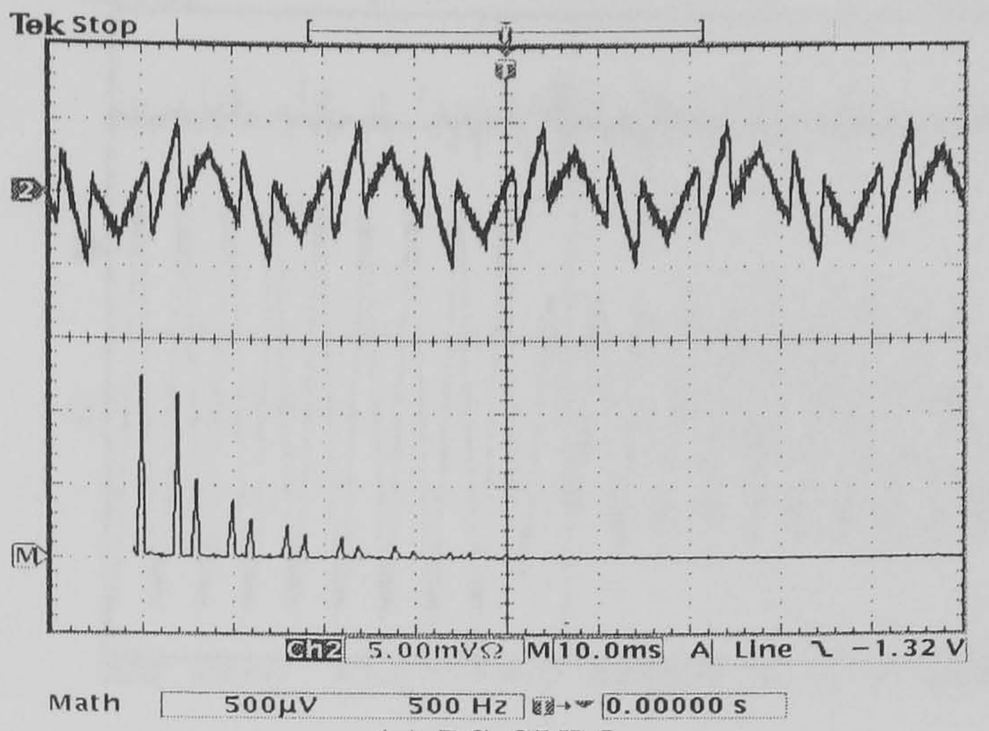
(b) Normal



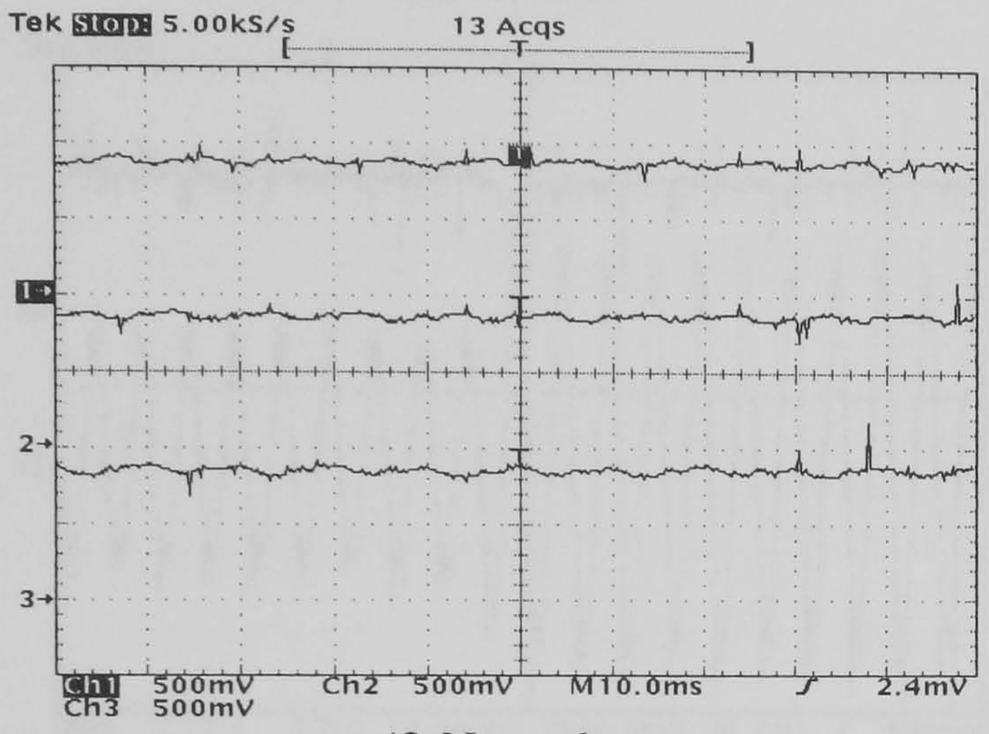
(c) PS-SVM



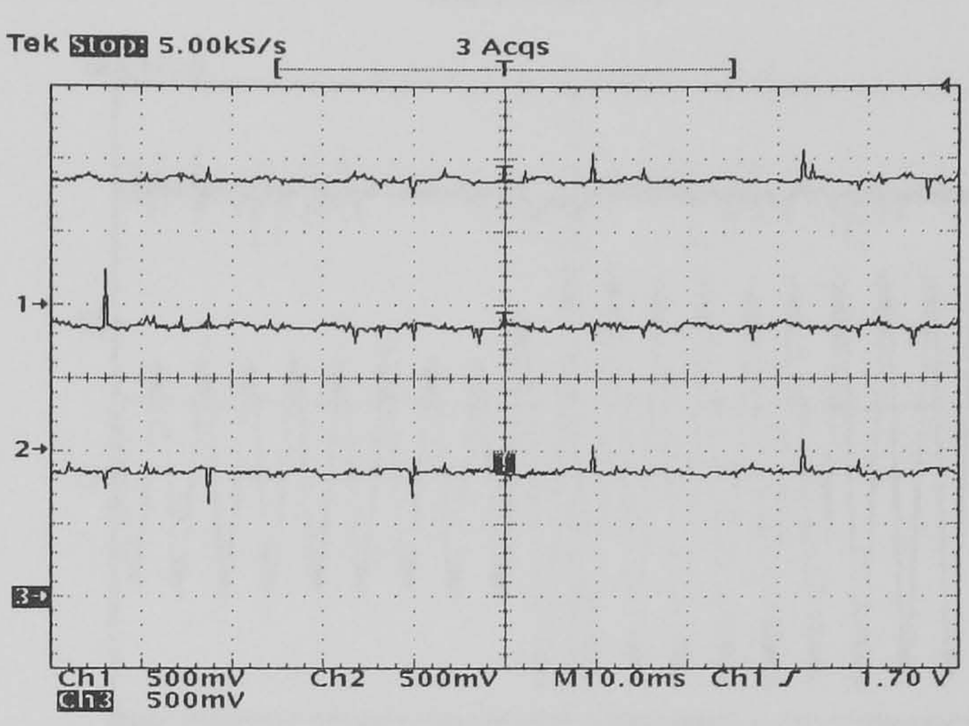
(d) Normal



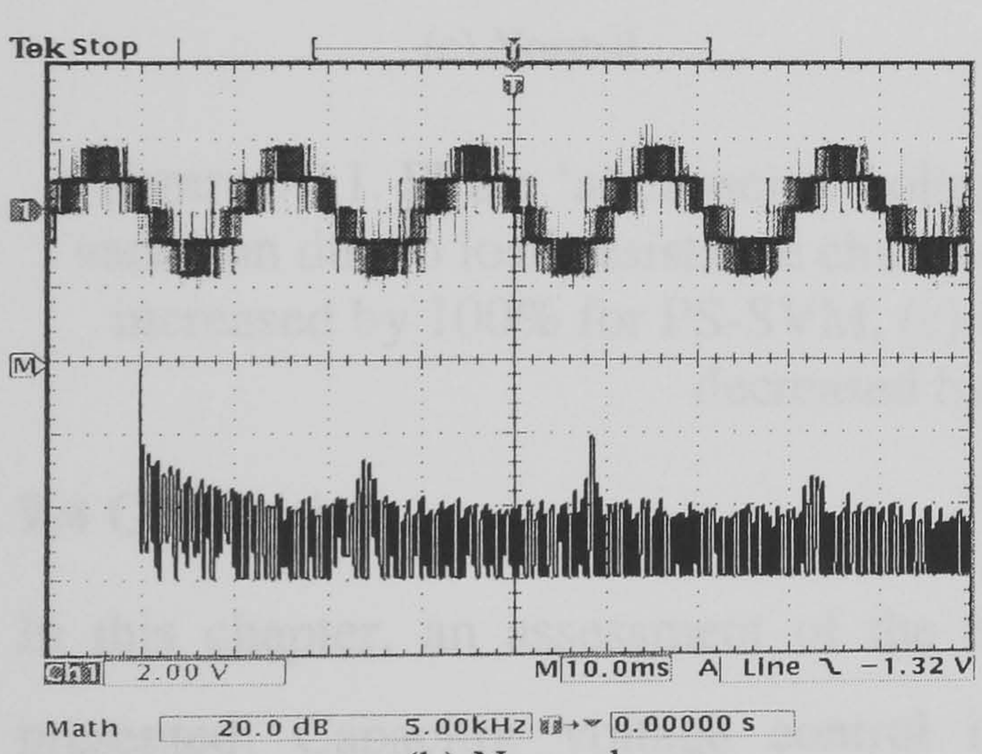
(e) PS-SVM



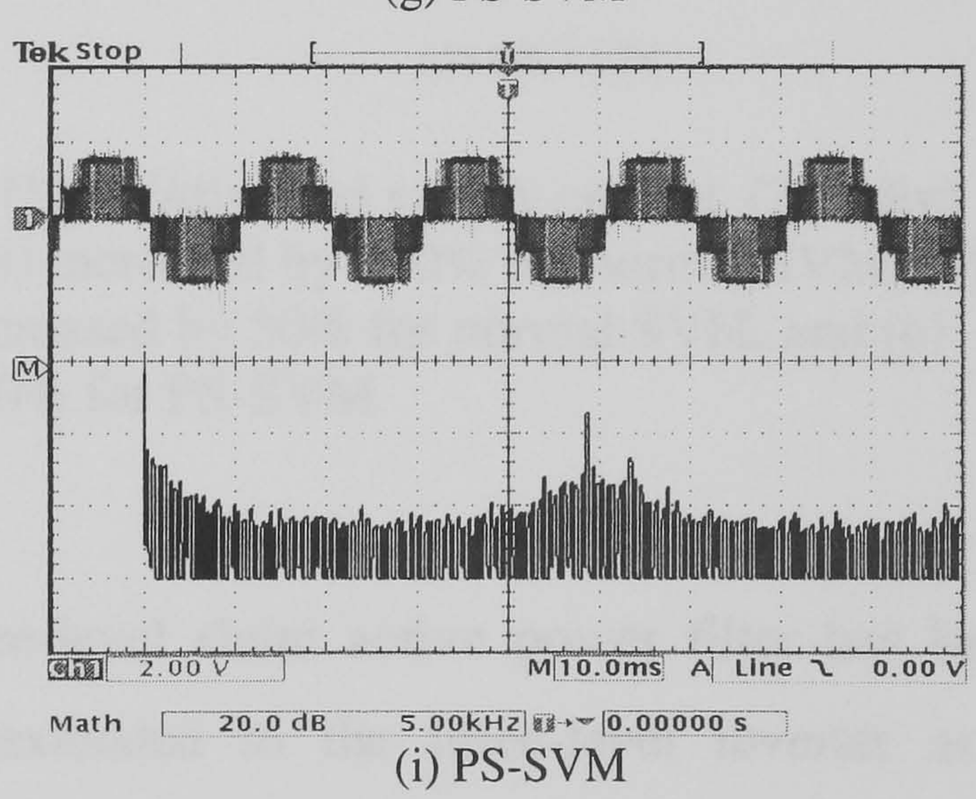
(f) Normal



(g) PS-SVM



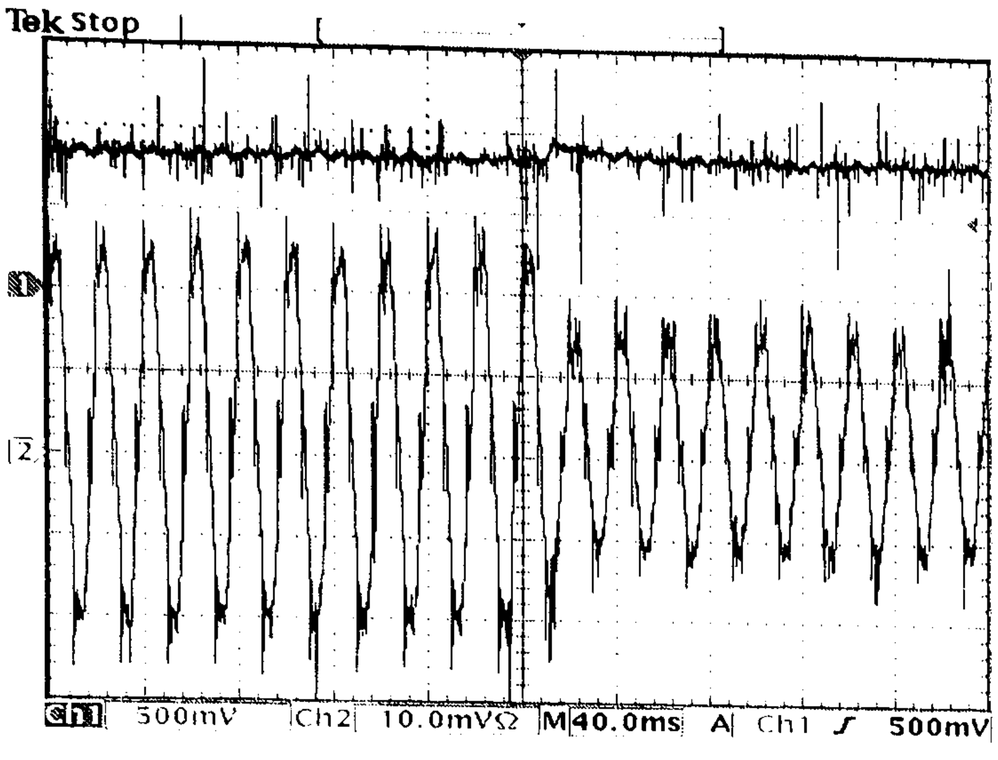
(h) Normal



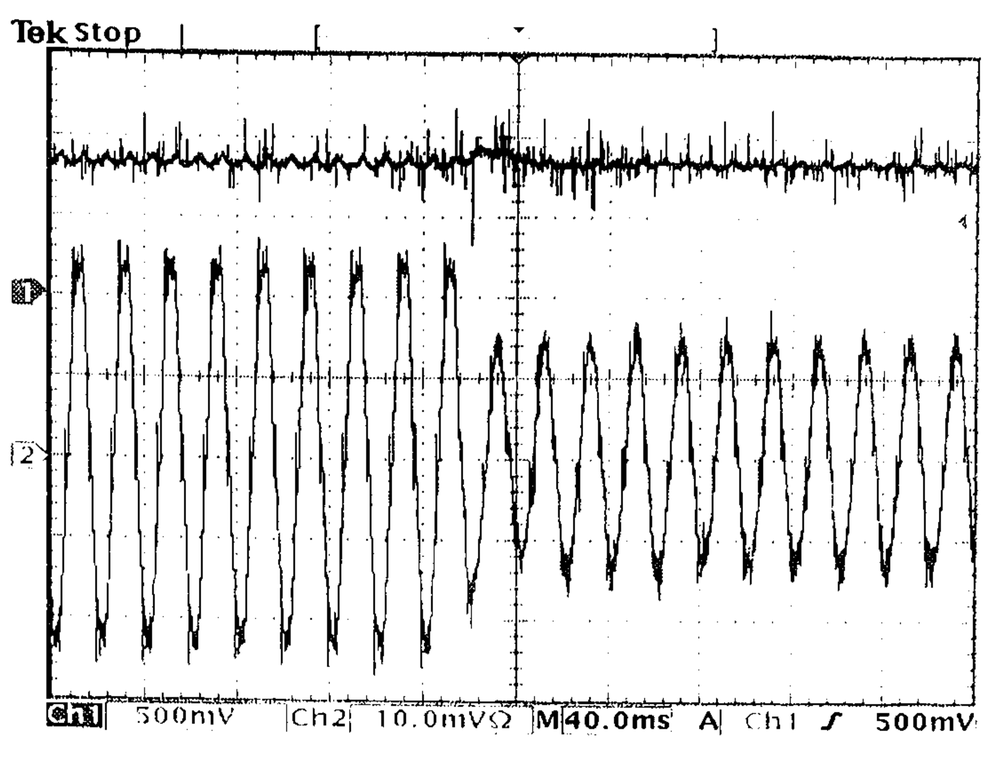
(i) PS-SVM

Figure 9.10. Practical results:
(a) the load current and spectrum (5A/div), (b) the supply current and spectrum for normal SVM (5A/div), (c) the supply current and spectrum for PS-SVM (5A/div), (d) the active filter current and spectrum for normal SVM (2.5A/div), (e) the active filter current and spectrum for PS-SVM (2.5A/div), (f) the capacitor voltages for normal SVM (100 V/div), (g) the capacitor voltages for PS-SVM (100 V/div), (h) the inverter output line voltage for normal SVM (400 V/div), and (i) the inverter output line voltage for PS-SVM (400 V/div)

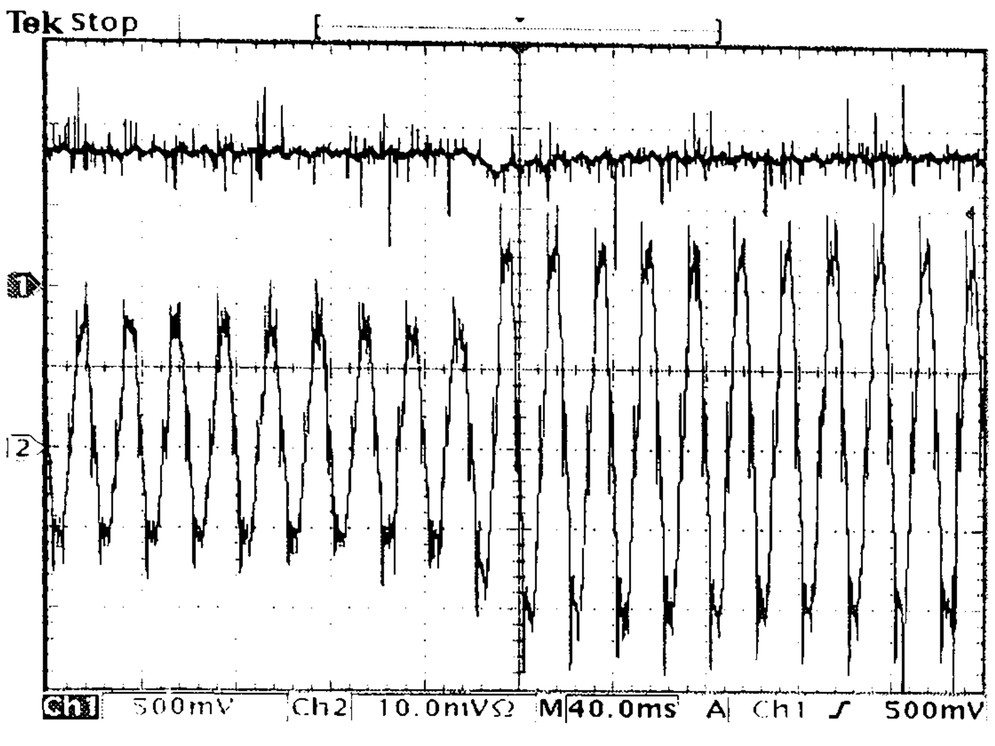
Parts a and b of figure (9.11) show the capacitor voltage of phase 'a' for normal SVM and PS-SVM respectively, due to a load resistance increase of 100% and then a 50% decrease. Parts c and d show the corresponding supply current of phase 'a' for each modulation case. It is clear that the practical results agree with the simulation results.



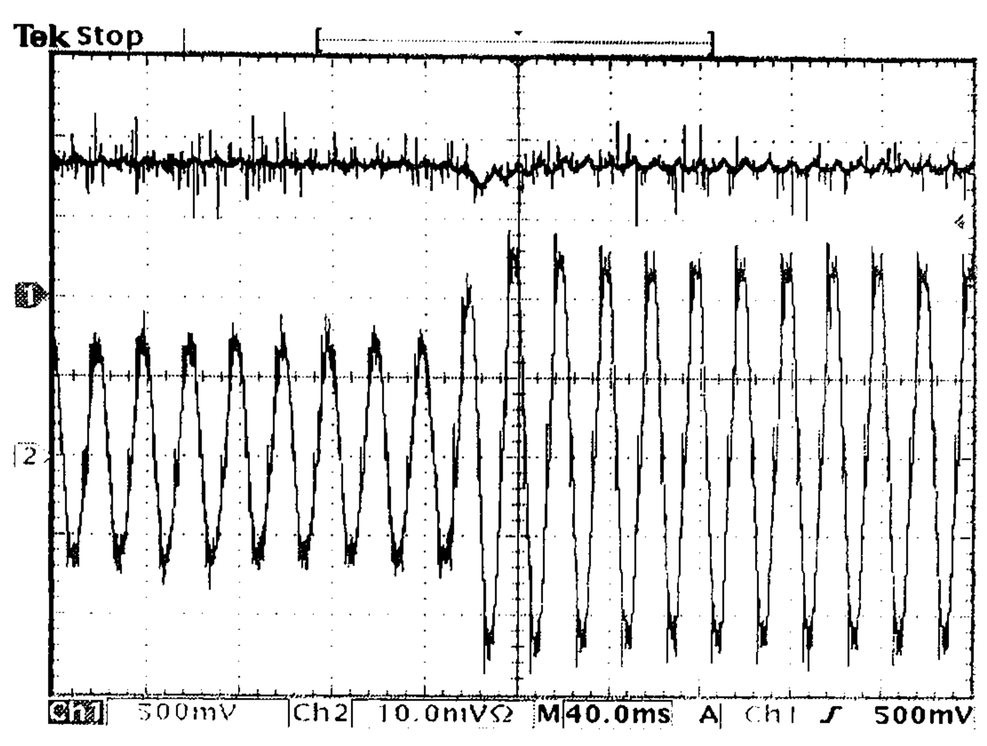
(a) Normal



(b) PS-SVM



(c) Normal



(d) PS-SVM

Figure 9.11. Phase 'a' capacitor voltage (100 V/div) and supply current (2 A/div) variation due to load resistance change: (a) increased by 100% for normal SVM, (b) increased by 100% for PS-SVM, (c) decreased by 50% for normal SVM, and (c) decreased by 50% for PS-SVM

9.4 Conclusion

In this chapter, an assessment of the three-level shunt active power filter has been presented. Capacitor voltage control is extended to the three-level inverter as a harmonic current extraction technique and predictive current control is used as the current control technique. The multilevel configuration extends the voltage rating of the active filter for the same switch voltage rating. The execution time of the developed algorithm, when using the conventional three-level SVM or phase shifted SVM, provides a high bandwidth active power filter displaying good filtering performance.

References

[9.1] B. Singh, Anuradha, and D. P. Kothari, 'Analysis of a novel active filter for balancing and reactive power compensation', Power Electronics and Variable Speed Drives, 1998, Conference Publication No. 456, IEE, pp. 57-62.

[9.2] T. Furuhashi, S. Okuma, and Y. Uchikawa, 'A study on the theory of instantaneous reactive power', Indust. Elect. Trans., IEEE, 1990, Vol. 37, pp. 86-90.

[9.3] N. Bruyant and M. Machmoum, 'Simplified digital-analogical control for shunt active power filters under unbalanced conditions', Power Electronics and Variable Speed Drives, 1998. Seventh International Conference on (IEE Conf. Publ. No. 456), 21-23 Sep 1998, pp. 11-16.

[9.4] S. J. Huang and J. C. Wu, 'A control algorithm for three-phase three-wired active power filters under non-ideal mains voltages', Power Electronics Trans., IEEE, Vol. 14, Jul 1999, pp. 753-760.

[9.5] A. M. Massoud, S. J. Finney, and B .W. Williams, 'Control Techniques for Multilevel Voltage Source Inverters', Power Electronics Specialists Conference, 2003. PESC03. IEEE 34rd Annual, Vol. 1, pp. 171-176.

Chapter 10

The five-level Shunt Active Power Filter

In this chapter, the five-level cascaded type inverter is used as a shunt active power filter. The capacitor voltage control technique used in chapters eight and nine as a harmonic current extraction technique is extended to the five-level shunt active power filter with a technique proposed for balancing the capacitor voltages. The predictive current controller used in chapters eight and nine is used. Phase-shifted space vector modulation (PS-SVM) and hybrid space vector modulation (H-SVM) are used. The proposed five-level shunt active power filter is validated by simulation and practically for both the modulation techniques. A simulation validation for the seven-level shunt active power filter is presented to prove the applicability of the approach to higher level numbers.

10.1 Five-level shunt active power filter

There are two ways of applying the shunt APF in the medium voltage range, either by using a transformer or by extending the semiconductor switch ratings (via a multilevel inverter or series connection of semiconductor devices). For the transformer approach, the problem is in the high cost of medium voltage transformers and also as the voltage decreases at the secondary side, the current is increased by the inverse ratio, which means parallel operated inverters may be needed.

The cascaded type multilevel inverter is suitable for use in a shunt active power filter. Shunt active power filters have been reported for all the three multilevel inverter types [10.1-10.8]. This previous research has concentrated on three-level inverters. For levels higher than three, there is the problem of maintaining the capacitor balance while maintaining good current tracking performance. Static VAR compensation is introduced in [10.6] for the eleven-level cascaded type inverter but for only a single pulse per half cycle for each cell, which gives a low control bandwidth, a crucial limitation in active filter applications. In this chapter the cascaded five-level inverter shown in figure (10.1) is used as a shunt active power filter. For a given semiconductor voltage rating, the five-level inverter gives a higher inverter output voltage than two and three level inverters.

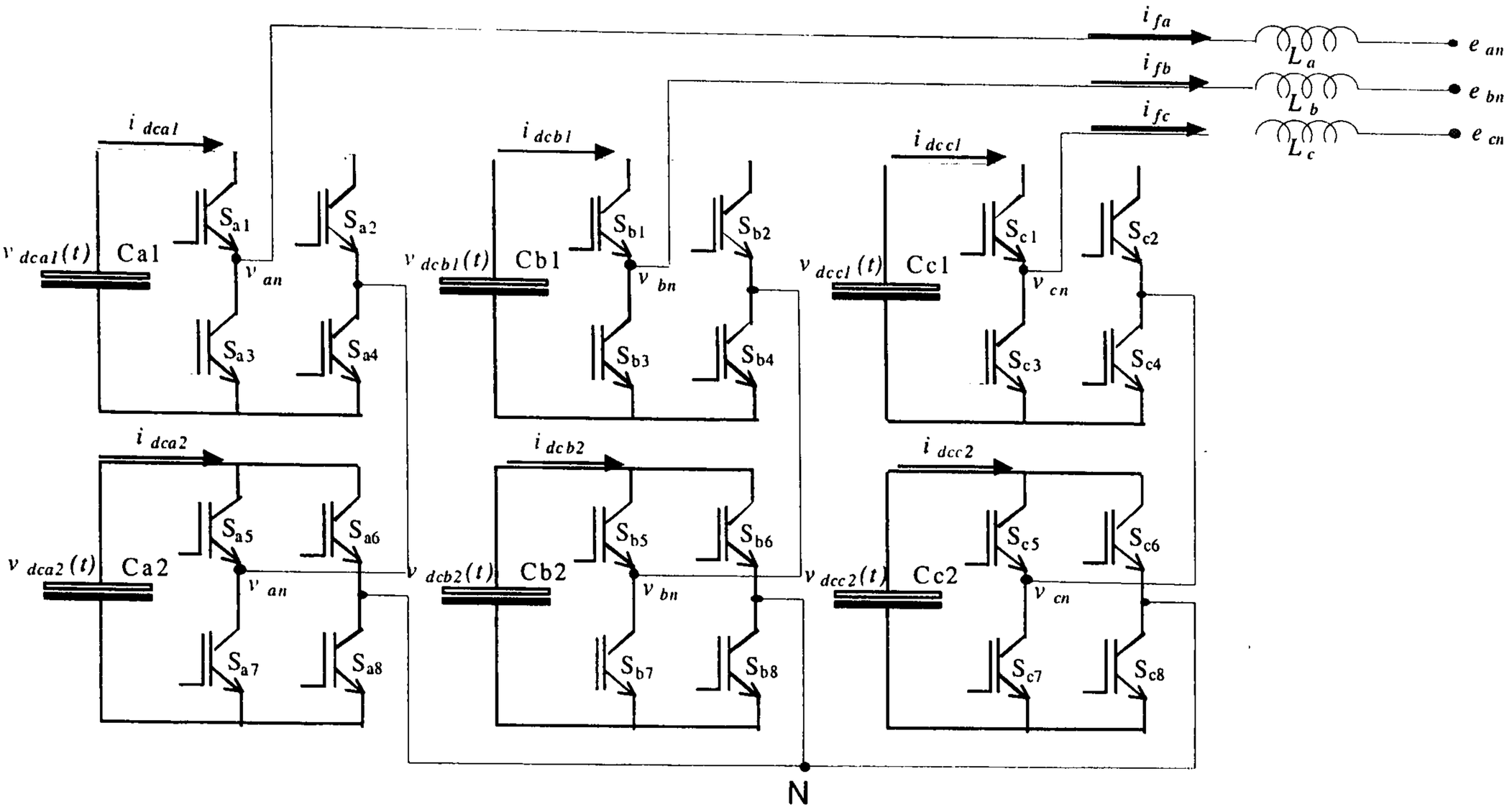


Figure 10.1. The five-level inverter used as a shunt active power filter

10.2 Proposed Active Power Filter

The proposed five-level shunt active power filter combines harmonic current extraction, current control, and capacitor voltage balancing. As a harmonic current extraction technique, capacitor voltage control [10.9]-[10.12] is extended to a five-level active power filter. Predictive current control introduced in chapters eight and nine is used. Five-level phase-shifted SVM (PS-SVM) and hybrid SVM (H-SVM), discussed in chapter six, are used as a PWM technique and to maintain the symmetrical loading of the capacitors, aiding capacitor voltage balancing.

10.2.1 Capacitor voltage control for harmonic extraction

The capacitor voltage control technique has many advantages, viz., the number of sensors is minimized (the measured quantities are the supply currents, voltages of the PCC, and three of the six capacitor voltages) and also the computational burden is reduced. The capacitor voltage control technique from chapters eight and nine is extended to five-level operation. To maintain the power balance, the capacitor must instantaneously compensate for the difference between the supply and the load power. So controlling three capacitor voltages (v_{dca1}, v_{dcb1}, and v_{dcc1}) using three proportional-integral (PI) controllers results in outputs which are proportional to the instantaneous changes in power balance. Multiplying each of these outputs by the corresponding per unit voltage of the PCC, results in the corresponding reference supply currents.

10.2.2 Capacitor voltage balance

There are three aspects to maintain the balance of the six capacitor voltages. The first aspect is to maintain the balance of three capacitors using the capacitor voltage control technique, as explained in section (10.2.1)The second aspect is the symmetrical loading of capacitors which is achieved by five-level PS-SVM or five-level H-SVM, which will be explained later. The third aspect is to interchange the digital control signals to the gate drives between one cell and the second cell in each phase, cycle-by-cycle to maintain the symmetry of pulses in a similar manner to that in [10.15]. A digital cycle detector is used for cycle-by-cycle digital exchange giving robust performance in the presence of noise introduced by the measurement feedback devices. Figure (10.2) shows the proposed system block diagram.

10.3 Phase-shifted SVM for multilevel inverters

In PS-SVM, superposition theory is applied to the multilevel inverter switches as discussed in chapter six. The use of five-level, PS-SVM allows a fast DSP execution time, since only simple two-level SVM calculations are carried out. Conventional two-level space vector modulation is applied to each three semiconductor switch groups of the three-phases and their complementary groups in the multilevel inverter. A pre-calculated time shift is introduced into the up-down counter of each switch group, then the output is summed and the required output voltage is obtained. For the *m*-level inverter, *m-1* up-down counters are used, with a phase shift of $T_{sw}/(m-1)$ introduced between the counters. The main advantage of using PS-SVM in the five-level shunt APF is that symmetrical capacitor loading can be achieved, as all the switches are turned on and off once each switching cycle.

SVM gives constant switching frequency and a 15% gain over sinusoidal PWM operation. The penalty of using this PWM technique is the switching loss is increased relative to conventional multilevel SVM. But conventional multilevel SVM can not be modified to symmetrically load the capacitors to maintain capacitor voltage sharing. Compared with series connected semiconductor devices, the switching loss is theoretically the same for a given inverter rating and in practice is lower since dynamic voltage sharing is not an issue. Also the output voltage *dv/dt* is lower than with the series connection. Five-level phase-shifted SVM (PS-SVM) has been discussed in detail in chapter six.

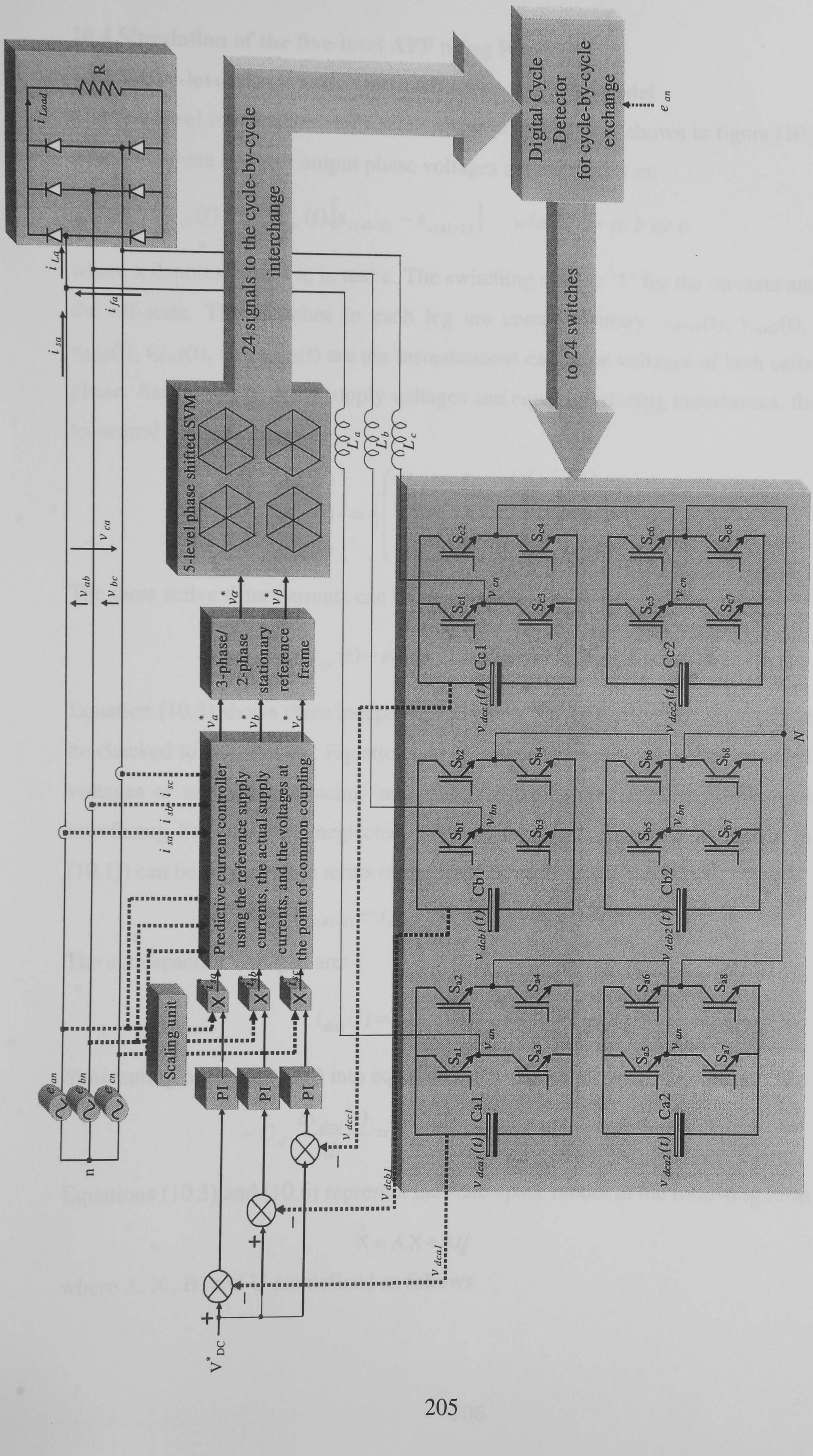


Figure 10.2. Block diagram of the proposed technique for the five-level shunt APF (The dotted lines indicate measured quantities)

10.4 Simulation of the five-level APF using PS-SVM

10.4.1 Five-level shunt active power filter state-space model

The five-level inverter used as a shunt active power filter is shown in figure (10.1), from which the three inverter output phase voltages are expressed as:

$$v_{x0}(t) = \sum_{i=1}^{2} v_{dcxi}(t).\left[s_{x(4i-3)} - s_{x(4i-2)}\right] \quad \textit{where } x = a, b \textit{ or } c \tag{10.1}$$

where x denotes phases a, b, and c. The switching state is '1' for the on-state and '0' for the off-state. The switches in each leg are complementary. v_{dca1}(t), v_{dca2}(t), v_{dcb1}(t), v_{dcb2}(t), v_{dcc1}(t), and v_{dcc2}(t) are the instantaneous capacitor voltages of both cells in each phase. Assuming balanced supply voltages and equal interfacing inductances, the phase-to-neutral voltages are:

$$\begin{pmatrix} v_{an}(t) \\ v_{bn}(t) \\ v_{cn}(t) \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}\begin{pmatrix} v_{a0}(t) \\ v_{b0}(t) \\ v_{c0}(t) \end{pmatrix} \tag{10.2}$$

The three active filter currents can be expressed as:

$$L\frac{di_{fx}(t)}{dt} = v_{xn}(t) - e_x(t) \qquad \textit{where } x = \textit{ a, b or c} \tag{10.3}$$

Equation (10.3) shows three independent currents. In simulation, the three currents must be checked to sum to zero. Equation (10.3) cannot be used for either unbalanced supply voltages or unequal interfacing inductances. In equation (10.3), the resistances of the interfacing inductors are neglected. The six capacitors currents (as shown in figure (10.1)) can be expressed in terms of the filter currents i_{fa}, i_{fb}, and i_{fc} as:

$$i_{dcxi}(t) = \left[s_{a(4i-3)} - s_{a(4i-2)}\right] i_{fx}(t) \qquad \text{for } i = 1,\ 2 \tag{10.4}$$

The six capacitor voltages are:

$$i_{dcxi}(t) = -C_{xi}.\frac{dv_{dcxi}(t)}{dt} \tag{10.5}$$

Substituting equation (10.4) into equation (10.5) yields

$$-C_{xi}.\frac{dv_{dcxi}(t)}{dt} = \left[s_{x(4i-3)} - s_{x(4i-2)}\right] i_{fx}(t) \tag{10.6}$$

Equations (10.3) and (10.6) represent the state-space model in the following form

$$\dot{X} = A.X + B.U \tag{10.7}$$

where A, X , B, and U are defined as follows

$$A = \begin{bmatrix} 0 & A_{12} & A_{13} \\ A_{21} & 0 & 0 \\ A_{31} & 0 & 0 \end{bmatrix} \tag{10.8}$$

and the 3-by-3 sub matrices are defined as follows.

$$A_{12} = \begin{bmatrix} \frac{2(s_{a1} - s_{a2})}{3L} & \frac{2(s_{a5} - s_{a6})}{3L} & \frac{(s_{b2} - s_{b1})}{3L} \\ \frac{(s_{a2} - s_{a1})}{3L} & \frac{(s_{a6} - s_{a5})}{3L} & \frac{2(s_{b1} - s_{b2})}{3L} \\ \frac{(s_{a2} - s_{a1})}{3L} & \frac{(s_{a6} - s_{a5})}{3L} & \frac{(s_{b2} - s_{b1})}{3L} \end{bmatrix},$$

$$A_{13} = \begin{bmatrix} \frac{(s_{b6} - s_{b5})}{3L} & \frac{(s_{c2} - s_{c1})}{3L} & \frac{(s_{c6} - s_{c5})}{3L} \\ \frac{2(s_{b5} - s_{b6})}{3L} & \frac{(s_{c2} - s_{c1})}{3L} & \frac{(s_{c6} - s_{c5})}{3L} \\ \frac{(s_{b6} - s_{b5})}{3L} & \frac{2(s_{c1} - s_{c2})}{3L} & \frac{2(s_{c5} - s_{c6})}{3L} \end{bmatrix}, \tag{10.9}$$

$$A_{21} = \begin{bmatrix} \frac{(s_{a2} - s_{a1})}{C_{a1}} & 0 & 0 \\ \frac{(s_{a6} - s_{a5})}{C_{a2}} & 0 & 0 \\ 0 & \frac{(s_{b2} - s_{b1})}{C_{b1}} & 0 \end{bmatrix}, \text{ and } A_{31} = \begin{bmatrix} 0 & \frac{(s_{b6} - s_{b5})}{C_{b2}} & 0 \\ 0 & 0 & \frac{(s_{c2} - s_{c1})}{C_{c1}} \\ 0 & 0 & \frac{(s_{c6} - s_{c5})}{C_{c2}} \end{bmatrix}$$

X, B, and U are defined as

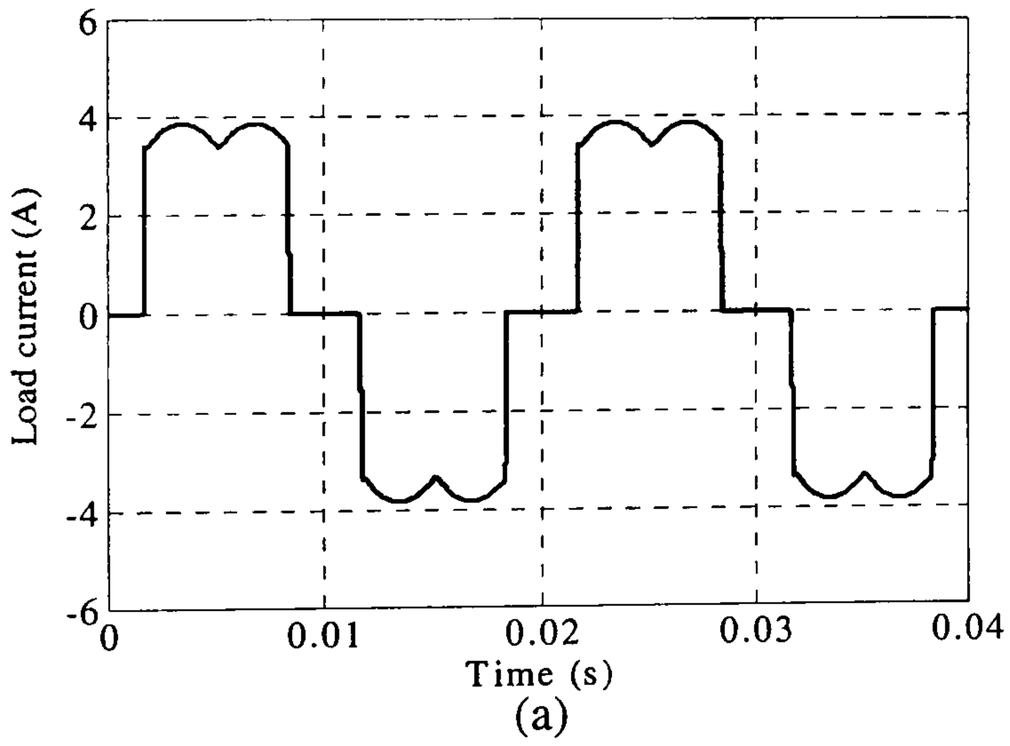
$$\mathrm{X} = \begin{bmatrix} i_{fa}(t) \\ i_{fb}(t) \\ i_{fc}(t) \\ v_{dca1}(t) \\ v_{dca2}(t) \\ v_{dcb1}(t) \\ v_{dcb2}(t) \\ v_{dcc1}(t) \\ v_{dcc2}(t) \end{bmatrix}, \mathrm{B} = \begin{bmatrix} \frac{-1}{L_a} & 0 & 0 \\ 0 & \frac{-1}{L_b} & 0 \\ 0 & 0 & \frac{-1}{L_c} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \text{ and } U = \begin{bmatrix} e_a(t) \\ e_b(t) \\ e_c(t) \end{bmatrix} \tag{10.10}$$

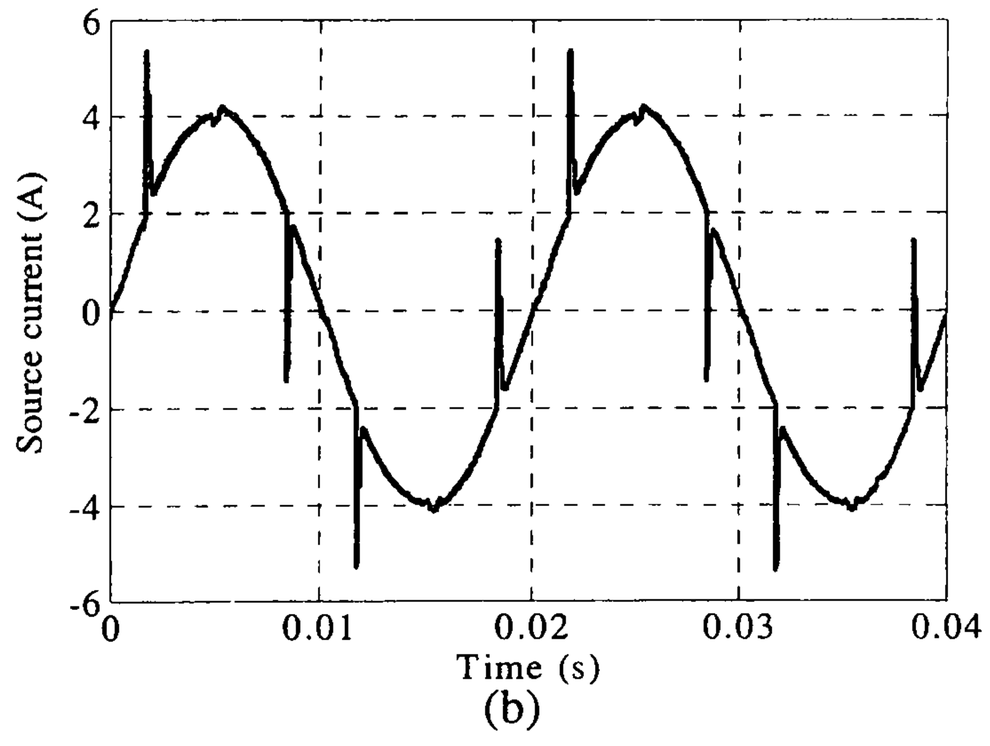
10.4.2 Simulation results

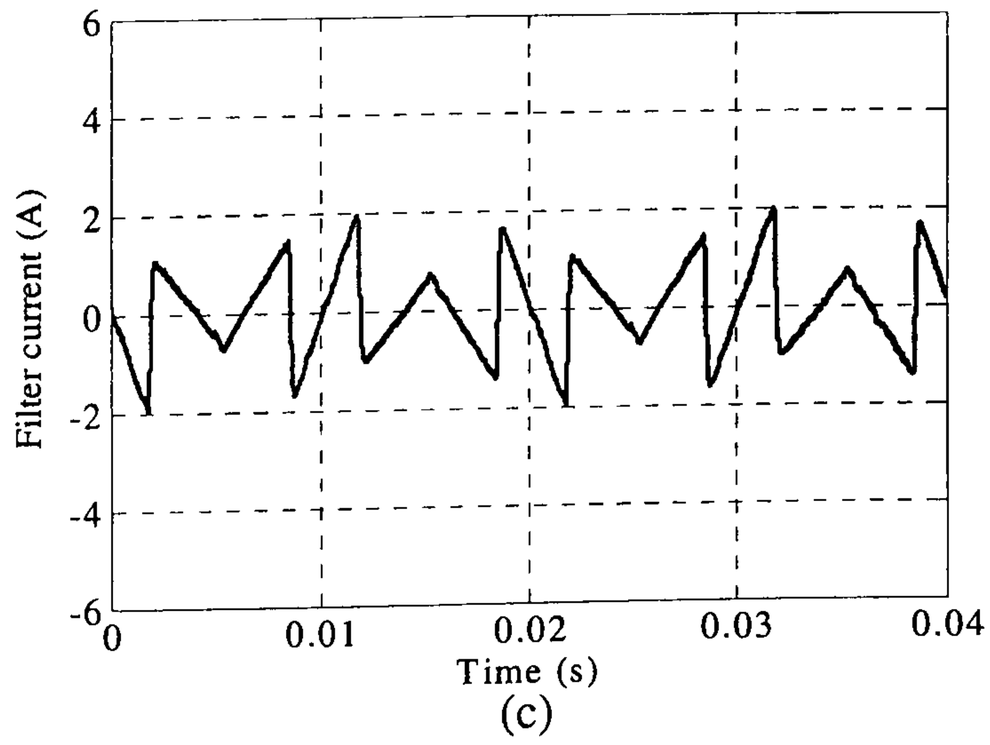
The state-space model of the active filter presented in section (10.4.1) is simulated using Matlab/Simulink (see Appendix H.3). The SVM is programmed using four m-files with an s-function block in Simulink, representing the SVM for each leg. The parameters used in simulation (and also the practical) are shown in Table 10.1. The non-linear load is a three-phase uncontrolled bridge rectifier feeding a 70 Ohm resistive load. Parts a to f of figure (10.3) show the load current, supply current, active filter current, and inverter output line voltage and its spectrum respectively. Parts a to f of figure (10.4) show the six capacitor voltages.

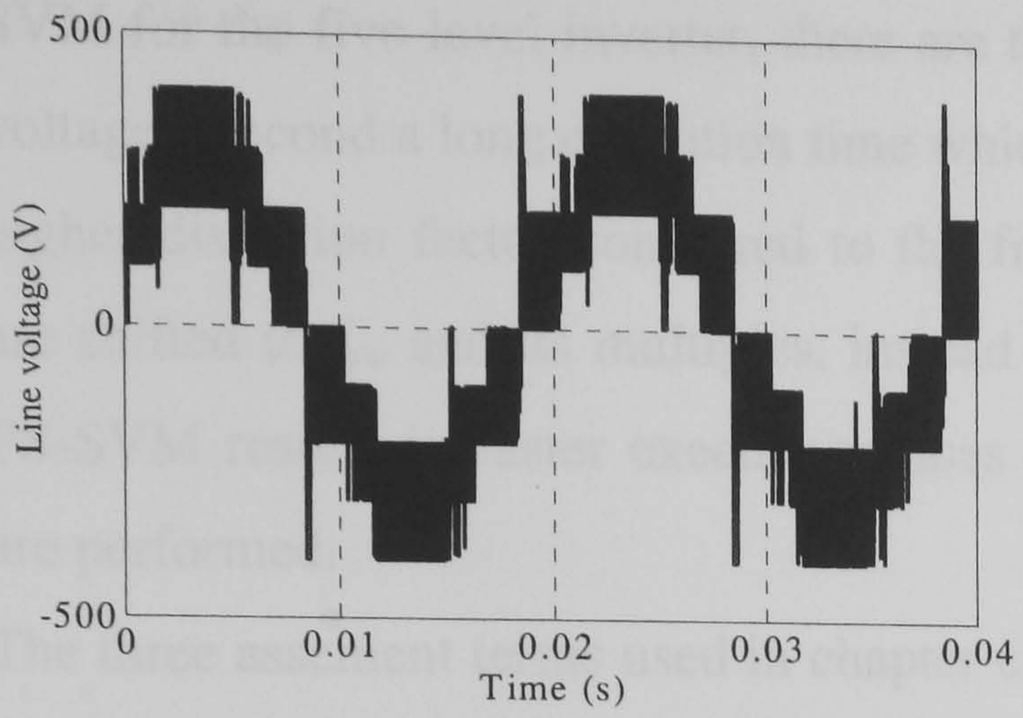
Table 10.1. The five-level (and seven-level) system parameters

V_{DC}^{*}	100	V
Supply voltage	110	V
C	2200	μF
L	10	mH
Sampling frequency	24.42	kHz
Switching frequency	12.21	kHz

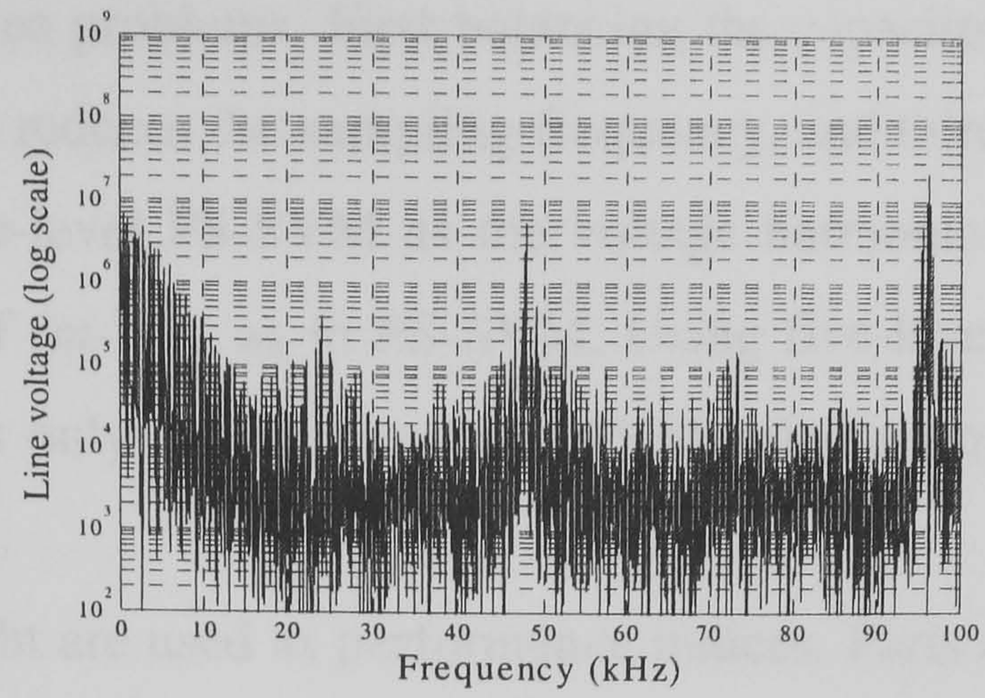






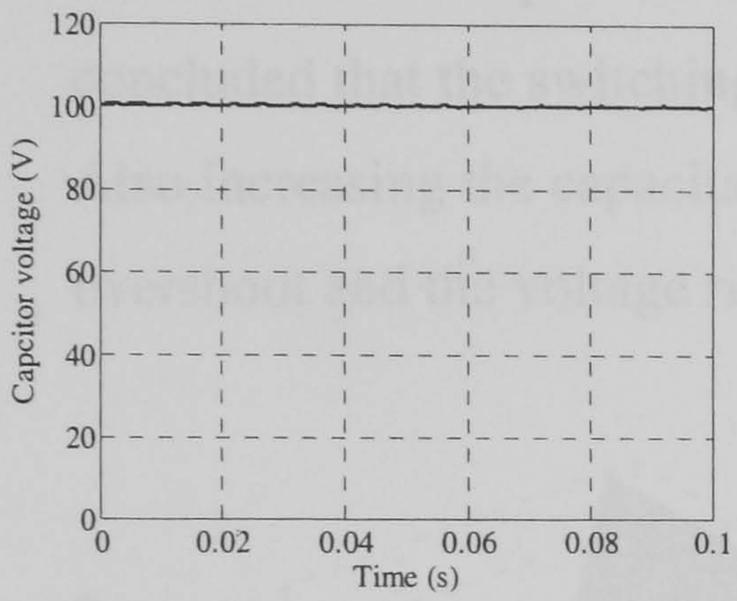


(d)

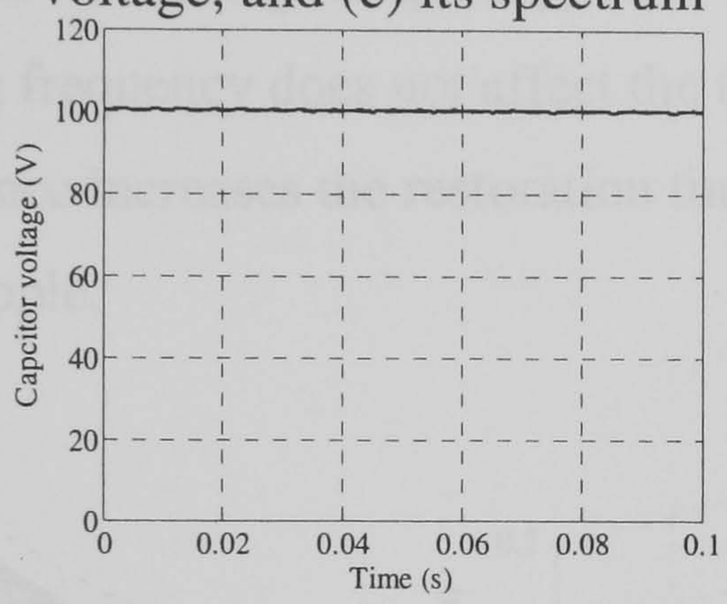


(e)

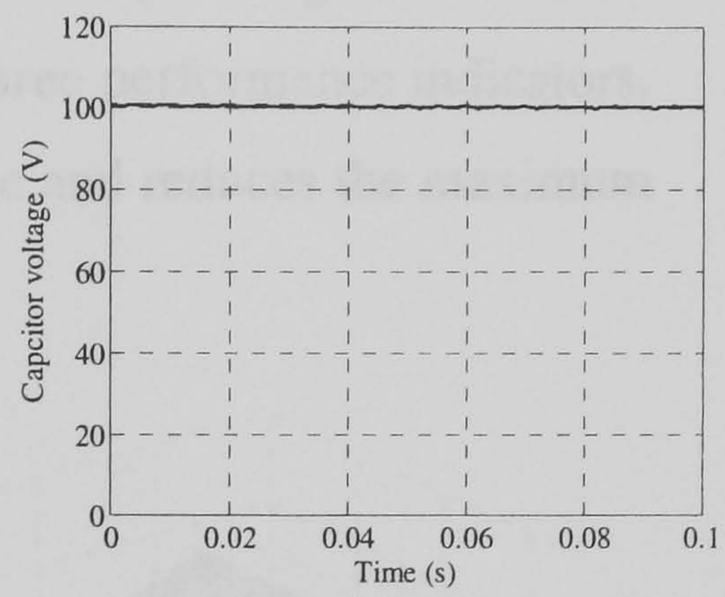
Figure 10.3. Simulation results:
(a) load current, (b) supply current, (c) active filter current, (d) inverter output line voltage, and (e) its spectrum



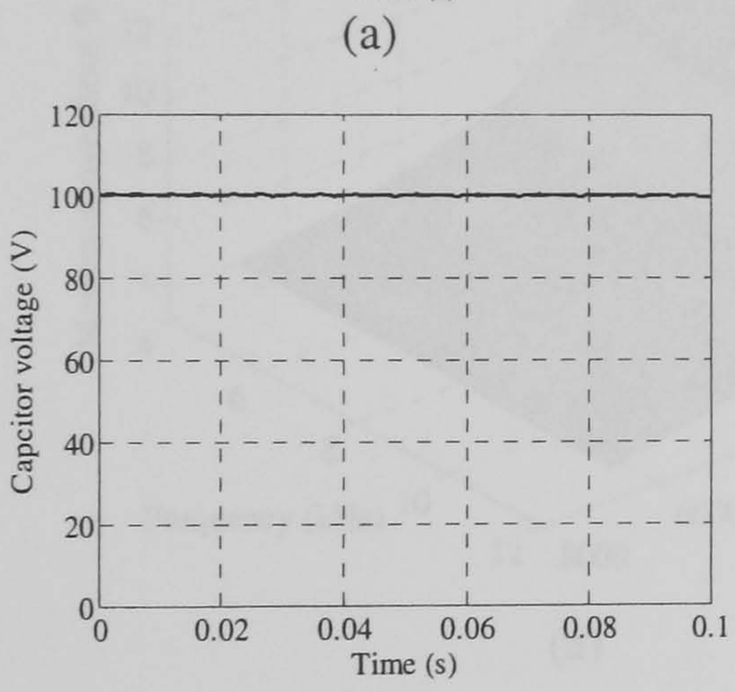
(a)



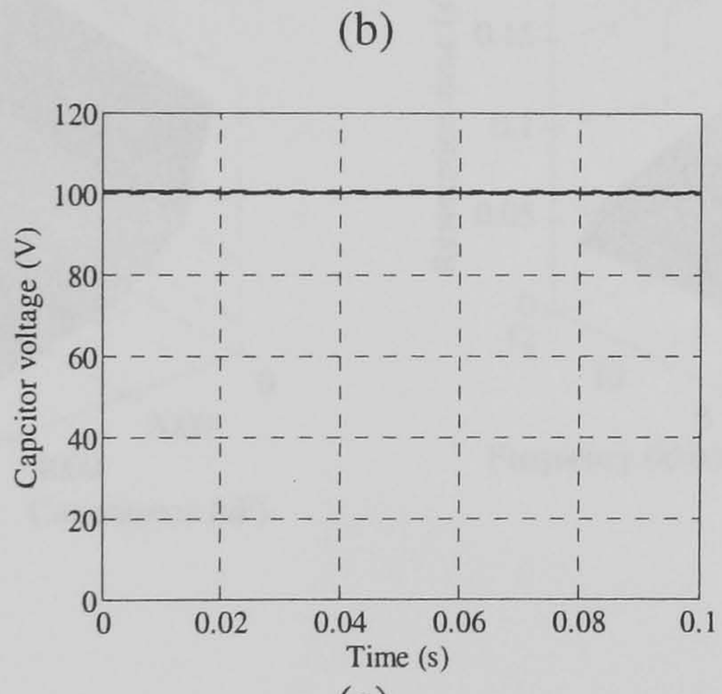
(b)



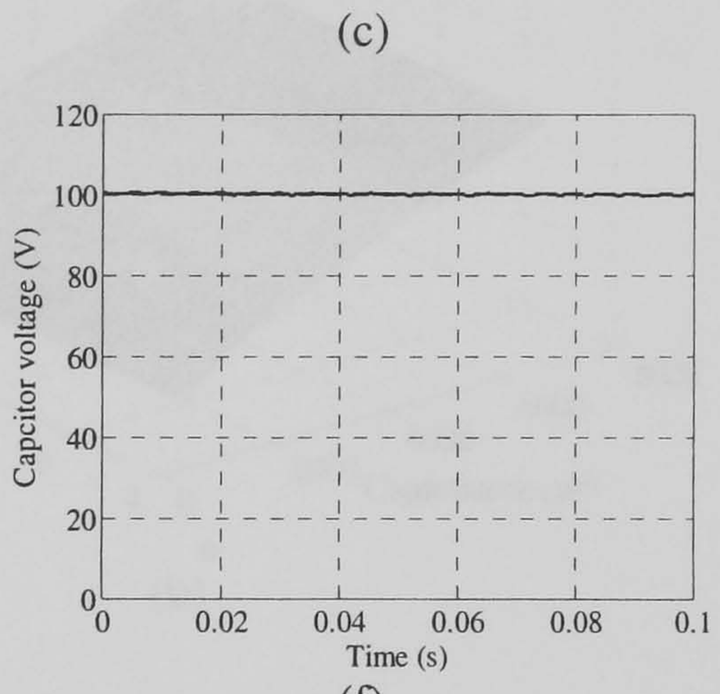
(c)



(d)



(e)



(f)

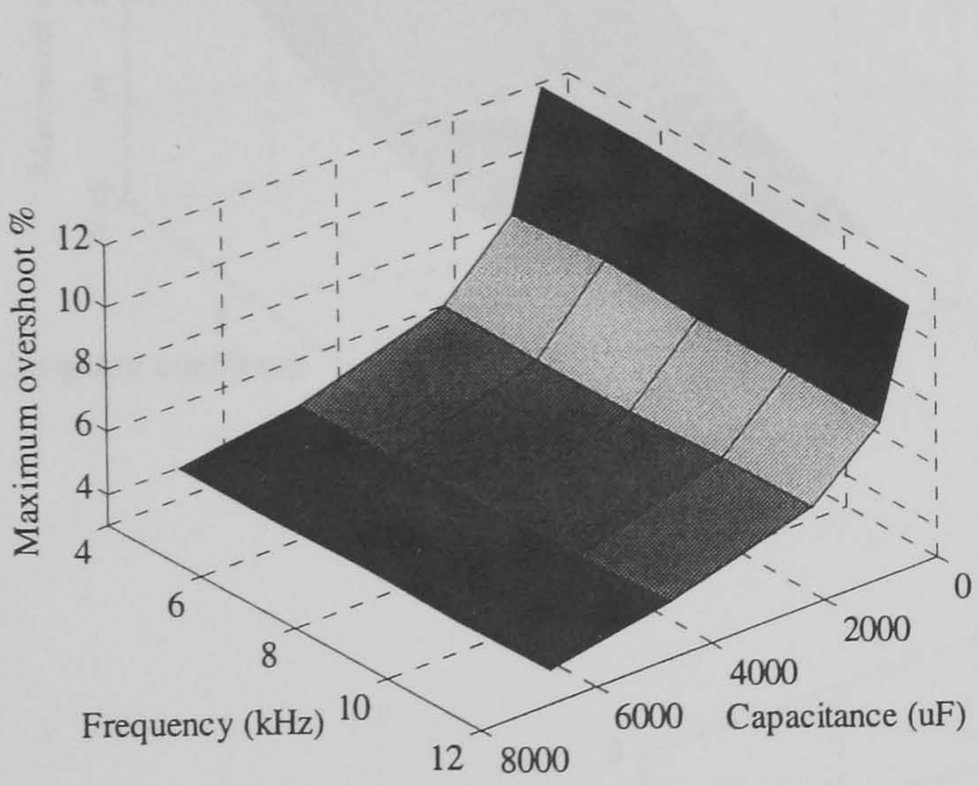
Figure 10.4. Simulation results of the six capacitor voltages:
(a) v_{dca1}, (b) v_{dcb1}, (c) v_{dcc1}, (d) v_{dca2} (e) v_{dcb2}, and (f) v_{dcc2}

10.4.3 System performance

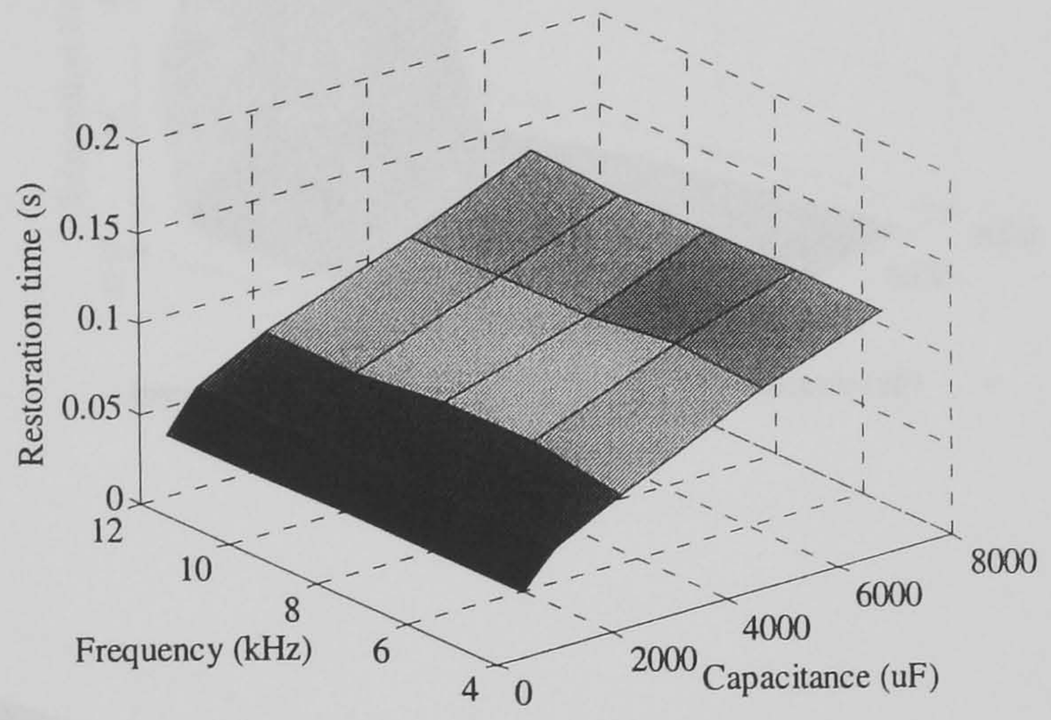
The five-level shunt APF inverter avoids using the transformer usually necessary with the two-level shunt APF in the medium voltage range. Five-level PS-SVM moves the harmonics to $4f_{sw}$ (and its multiples) which in turn eases filtering characteristics and enables better performance with a lower interfacing inductance, compared to the two-level shunt APF plus transformer. There is the problem of increased switching losses as all the switches are turning on and off once in the switching cycle. The capacitance needed will be higher than the two-level equivalent to overcome the ripple summation in each cell in the same phase leg. (Electrically the two capacitors can be considered as series connected which reduces the effective capacitance). When using conventional

SVM for the five-level inverter, there are three problems. First balancing the capacitor voltages, second a long execution time which reduces the sampling frequency, and third higher distortion factor compared to the five-level PS-SVM as the voltage harmonics are shifted to f_{sw} and its multiples, instead of $(m-1)f_{sw}$ as in PS-SVM. Using five-level PS-SVM results in faster execution times as only simple two-level SVM calculations are performed.

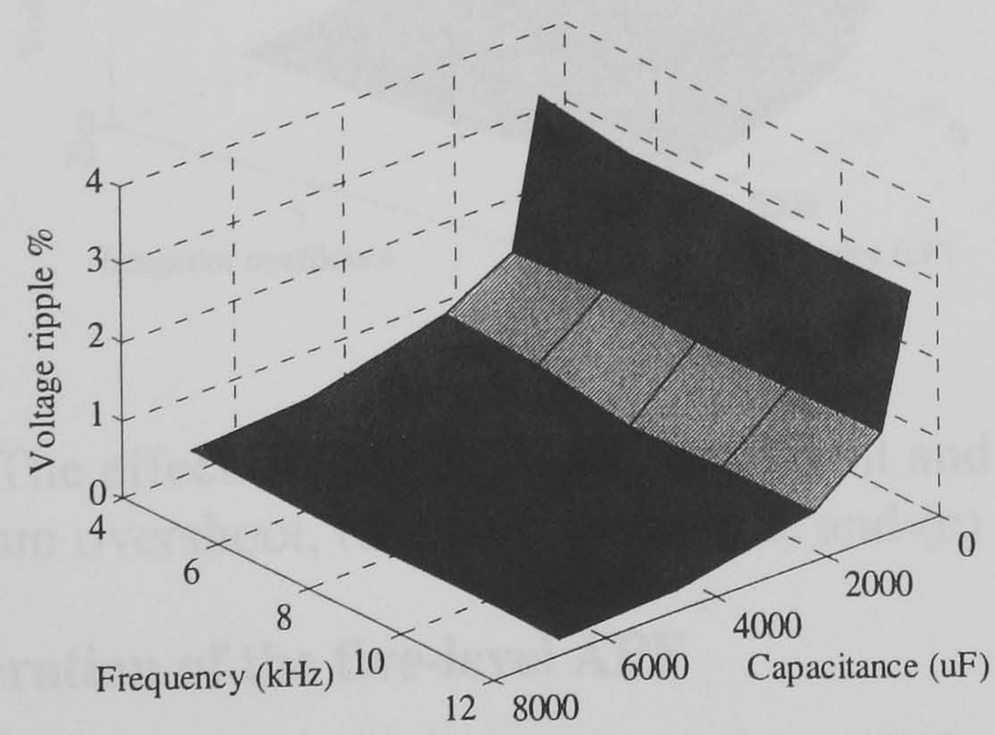
The three assement terms used in chapter eight are used as performance indices. Parts a to c of figure (10.5) show the maximum overshoot, restoration time, and voltage ripple as a function of capacitance and switching frequency (the sampling frequency is assumed to be equal to the switching frequency). As in chapter eight, it can be concluded that the switching frequency does not affect the three performance indicators. Also increasing the capacitance increases the restoration time and reduces the maximum overshoot and the voltage ripple.



(a)



(b)



(c)

Figure 10.5. The effect of the switching frequency and capacitance on:
(a) maximum overshoot, (b) restoration time, and (c) voltage ripple

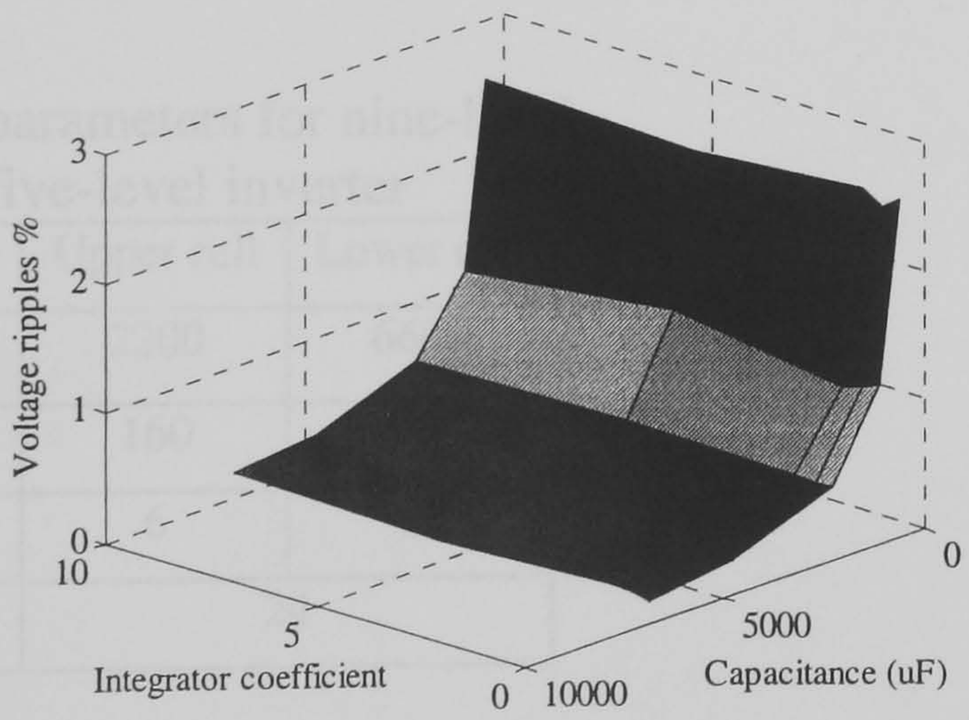
10.4.4 Proportional-integral (PI) controller design

Three identical PI controllers are used for capacitor voltage control. In simulation and practice, k_I and k_p are both 0.1

For a 50% load current reduction, parts a to c of figure (10.6) show the maximum overshoot, the restoration time, and the voltage ripple as a function of capacitance and integrator coefficient (k_I). It can be concluded that increasing both the integrator coefficient and the capacitance decreases the maximum overshoot, while increasing the integrator part and decreasing the capacitance, decreases the restoration time. The voltage ripple is independent of the integrator coefficient and decreases as capacitance increases.

(a)

(b)



(c)

Figure 10.6. The effect of the integrator coefficient and capacitance on:
(a) maximum overshoot, (b) restoration time, and (c) voltage ripple

10.4.5 Nine-level operation of the five-level APF

Nine-level operation of the five-level APF can be achieved if capacitor values of C and 3C are used for the two cells in each phase, whence each cell voltage will be V_{DC} and $V_{DC}/3$, respectively. The nine-levels obtained are 0, $\pm\frac{1}{3}V_{DC}$, $\pm\frac{2}{3}V_{DC}$, $\pm V_{DC}$, $\pm\frac{4}{3}V_{DC}$.

Figure (10.7) shows a phase leg of the five-level inverter for nine-level operation. The modulation index for the upper cell in figure (10.7) is

$$m_a = \frac{V_{ref}^*}{4V_{DC}\cos\left(\frac{\pi}{6}\right)} \tag{10.11}$$

and for the lower cell:

$$m_a = \frac{V_{ref}^*}{4\frac{V_{DC}}{3}\cos\left(\frac{\pi}{6}\right)} \tag{10.12}$$

The definitions of these two modulation indices (equation (10.11) and (10.12)) rotate cycle-by-cycle on the two cells as the PWM signals rotate on the two cells. To equate switching losses in each cell, the upper cell has a lower switching frequency with higher rated semiconductor devices (the semiconductor switch sustains V_{dc}). The lower cell has a higher switching frequency and a lower semiconductor ratings ($V_{dc}/3$). Table 10.2 indicates the main parameters used for the simulations. Parts a and b of figure (10.8) show the active filter current and supply current. Parts c and d show the output line voltage and the power spectrum in which the line voltage has 17 level (2×9 levels - 1) while the harmonics are shifted to $2f_1$ and $2f_2$ and their multiples (2×6 kHz and 2×12 kHz and their multiples). Parts e to g of figure (10.8) show the six capacitor voltages.

Table 10.2. System parameters for nine-level operation of five-level inverter

	Upper cell	Lower cell
Capacitance (μF)	2200	6600
DC voltage (V)	160	160/3
f_{sw} (kHz)	6	12
f_s (kHz)	24	

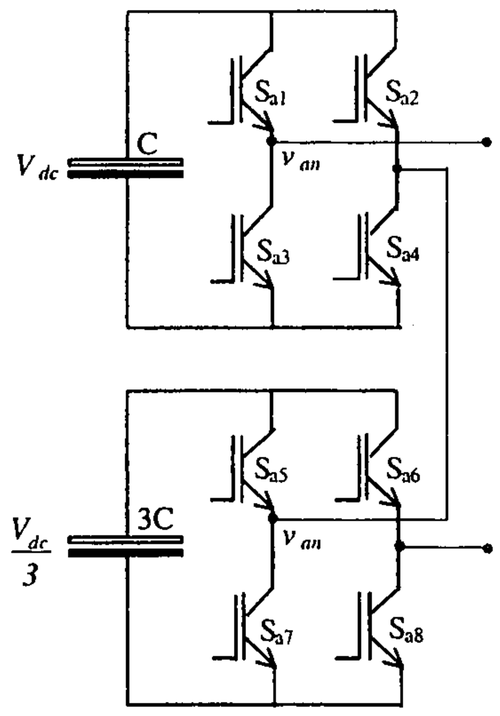
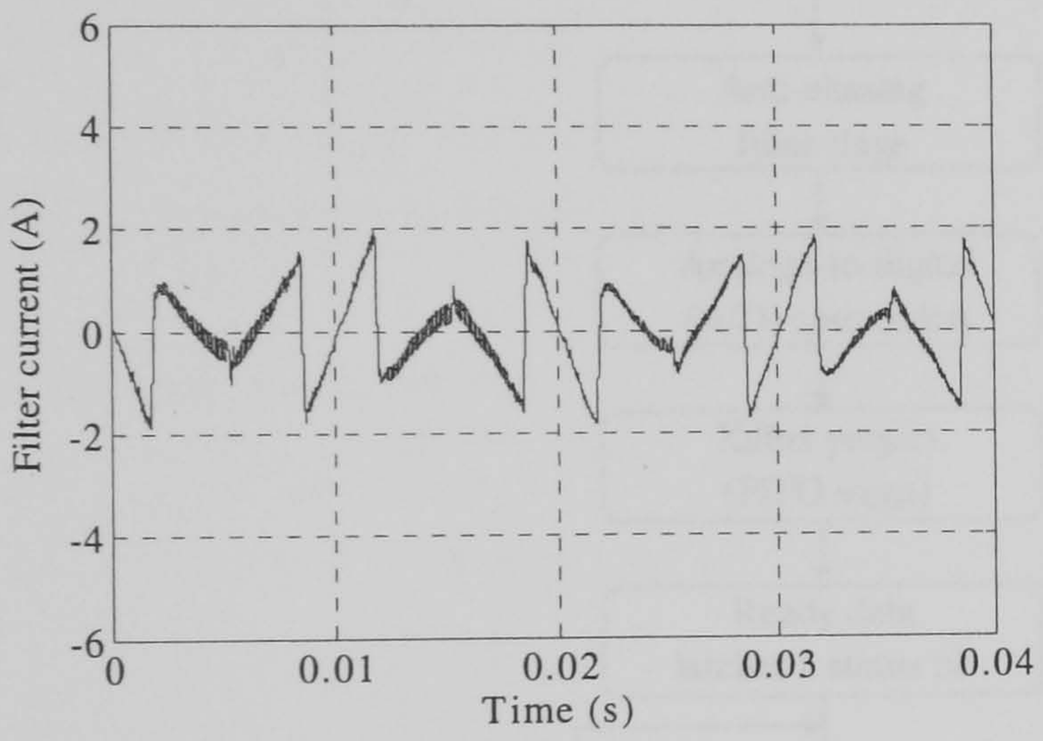


Figure 10.7. A phase leg of the five-level inverter for nine-level operation

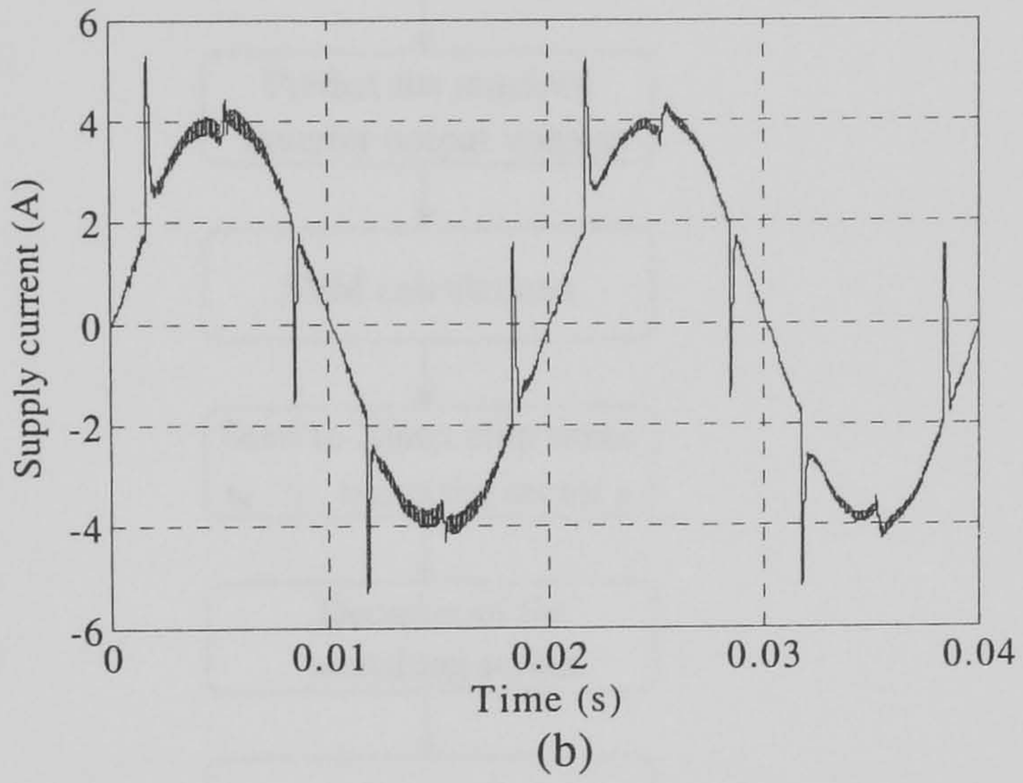
10.5 Practical results using PS-SVM

The execution time of the DSP program is 37 μs. In the DSP program (see Appendix F.1), the reference and measured capacitor voltages are compared, the reference active filter current is extracted, and then the reference voltages are predicted. The sampling frequency (24.42 kHz) is twice the switching frequency (12.21 kHz). A signal is sent

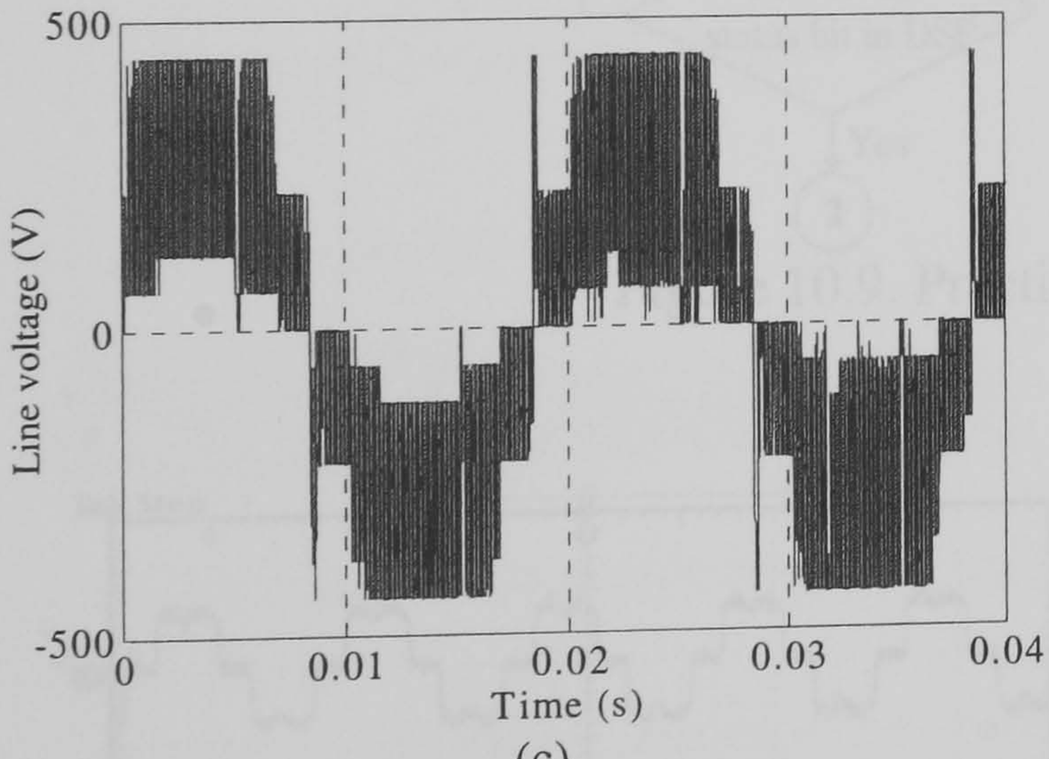
from the DSP to the AED-106 for the cycle-by-cycle exchange performed within Xilinx. Then the Xilinx project produces the switching decision from the known sector and time periods (t_0, t_1, t_2, and t_7). A switching dead time of 640 ns is introduced by the Xilinx project. Figure (10.9) shows the flow chart of the practical system procedures. Parts a to d of figure (10.10) show the load current, supply current, active filter current, and the inverter output line voltage and their spectra in each case, respectively. Parts a to c of figure (10.11) show the six capacitor voltages. The imbalance on the lower capacitor voltages occurs because these voltages are indirectly controlled. Figure (10.12) shows the capacitor voltage and supply current of phase 'a' due to a load resistance increase of 100% (part (a)) and then a 50% decrease (part (b)). See Appendix G.3 for R-L and R-C loads.



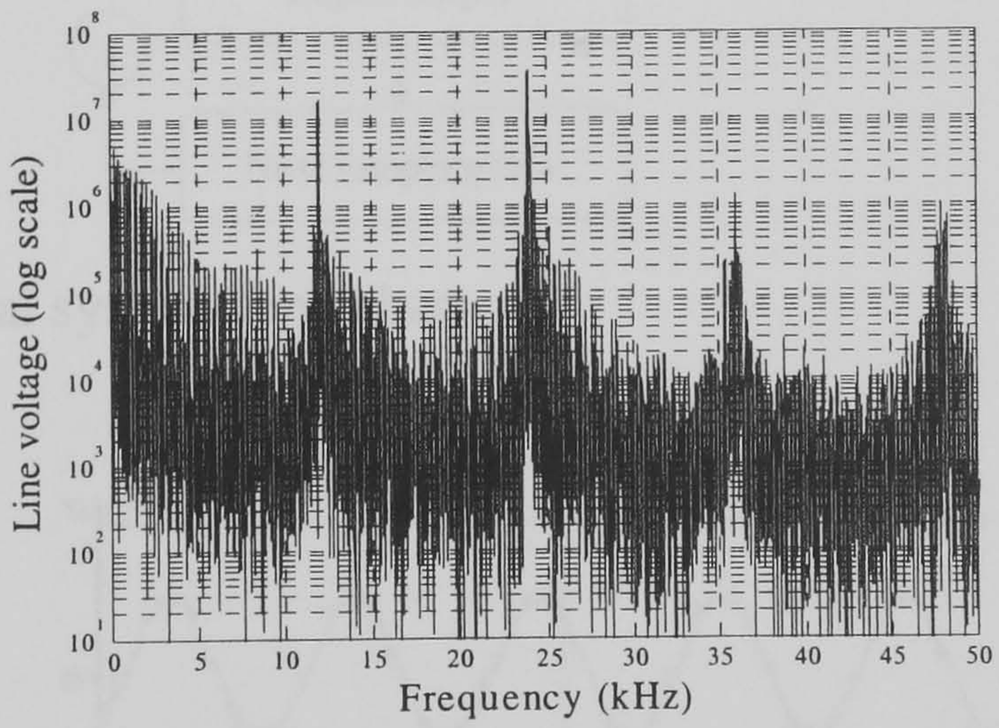
(a)



(b)



(c)



(d)

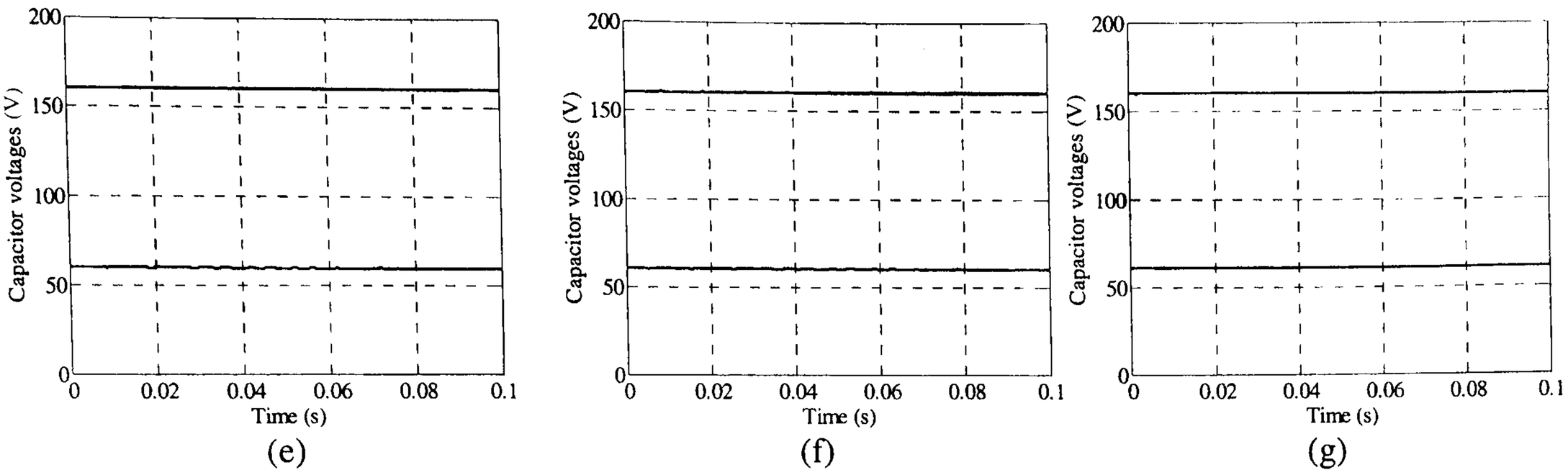


Figure 10.8. Simulation results:
(a) active filter current, (b) supply current, (c) inverter output line voltage, (d) its spectrum, (e) v_{dca1} and v_{dca2}, (f) v_{dcb1} and v_{dcb2}, and (g) v_{dcc1} and v_{dcc2}

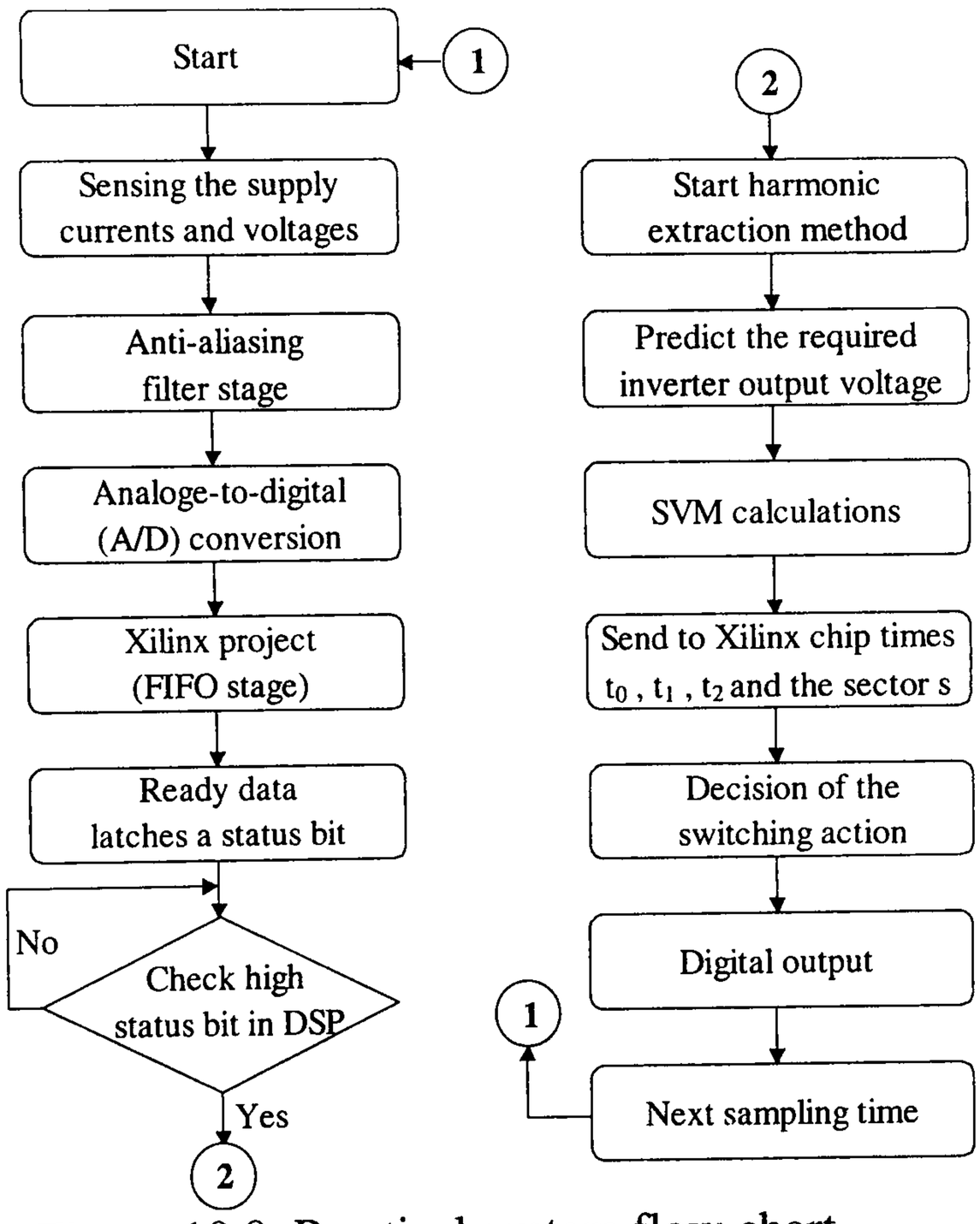
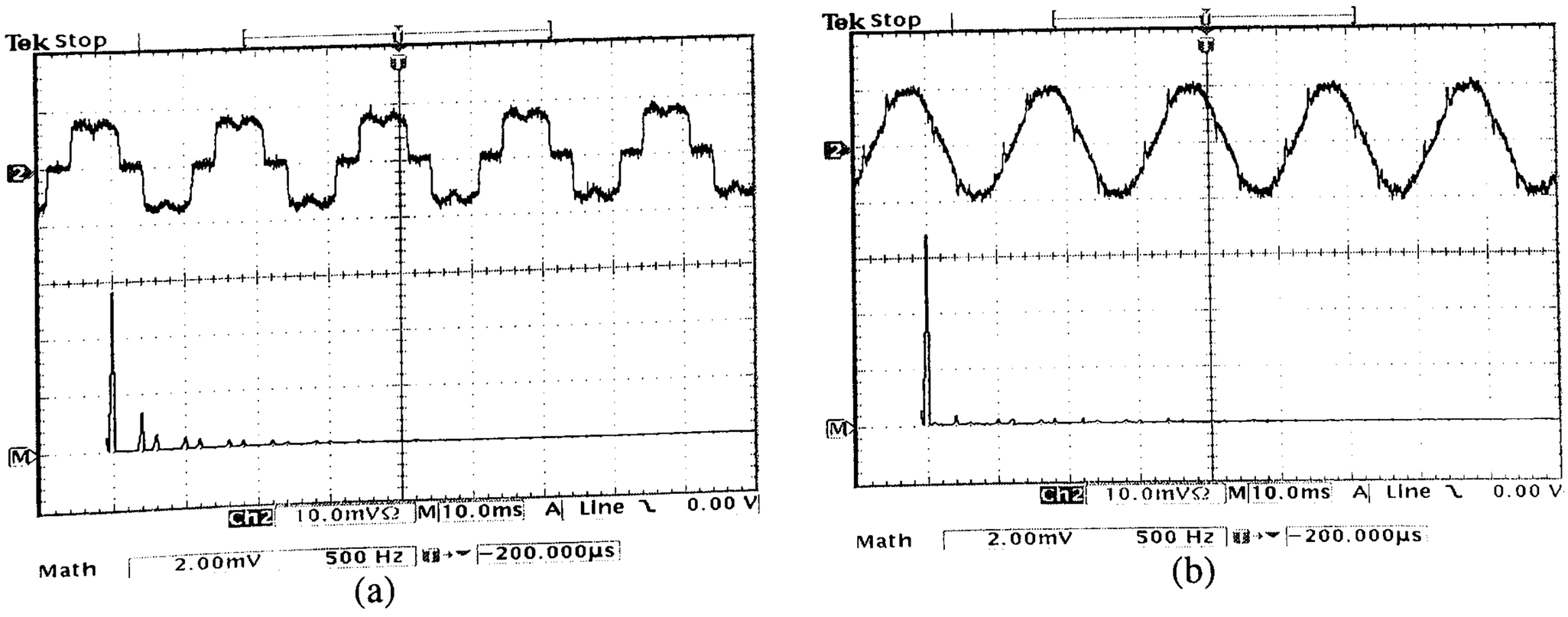


Figure 10.9. Practical system flow chart



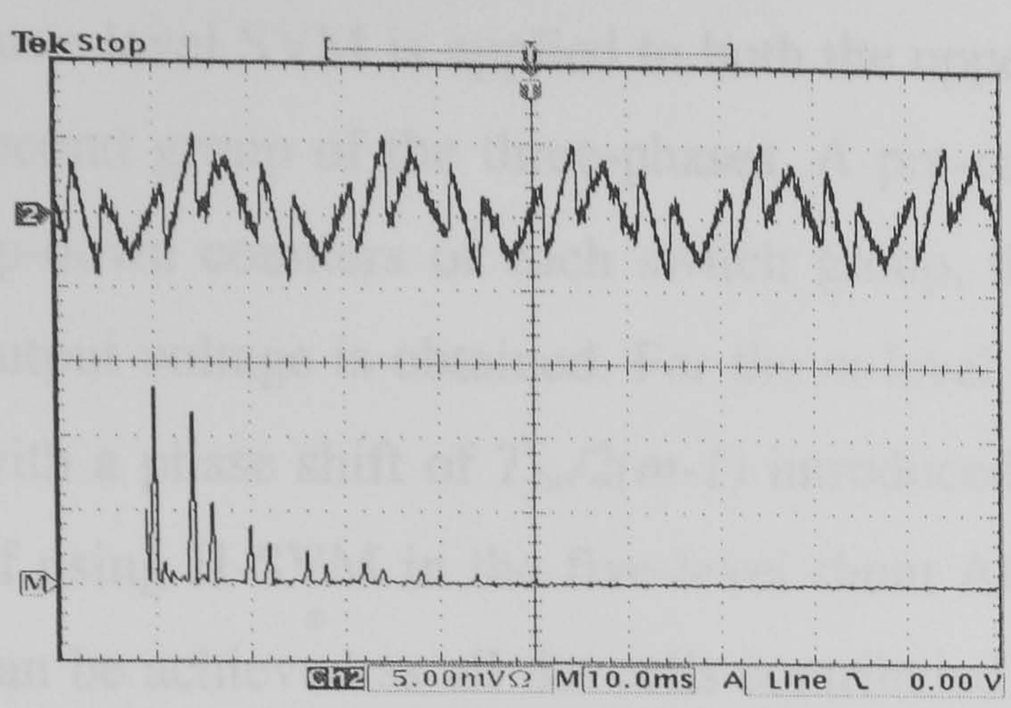


Figure 10.10. Practical results:
(a) the load current and its spectrum (5A/div), (b) the supply current and its spectrum (5A/div), (c) the active filter current and its spectrum (2.5A/div), and (d) the inverter output line voltage (400 V/div)

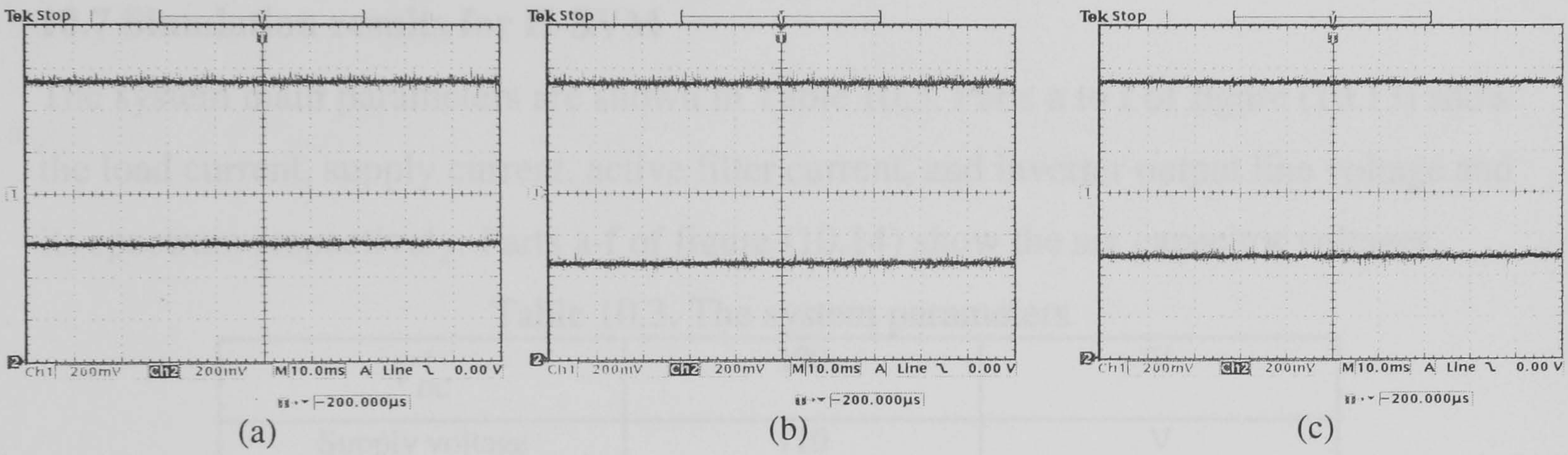


Figure 10.11. Practical capacitor voltages (40 V/div):
(a) v_{dca1} and v_{dca2}, (b) v_{dcb1} and v_{dcb2}, and (c) v_{dcc1} and v_{dcc2}

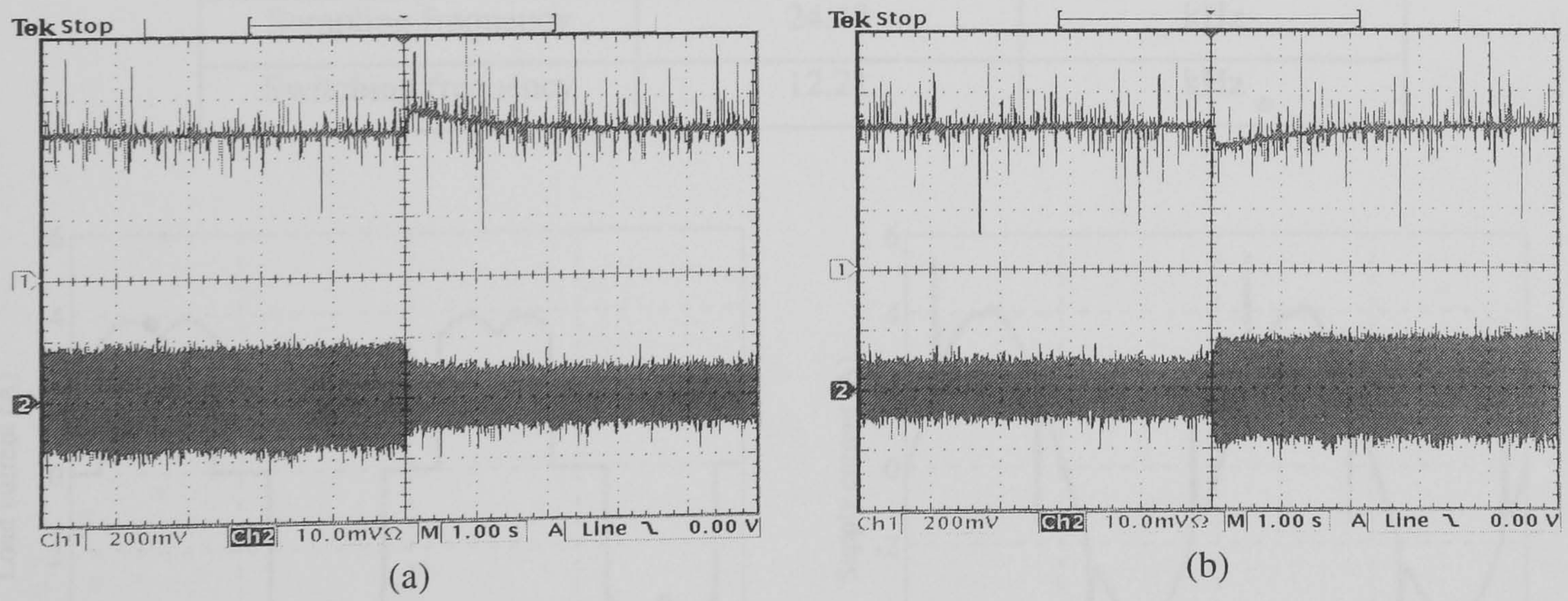


Figure 10.12. Phase 'a' capacitor voltage (40 V/div) and supply current (2 A/div) variation due to load resistance change (a) increase of 100% (b) decrease of 50%

10.6 Hybrid SVM for multilevel inverters

An alternative PWM technique is the hybrid SVM. In H-SVM, superposition theory is applied to the multilevel inverter semiconductor switches as discussed in chapter six. Five-level H-SVM is less complex and has a faster execution time than conventional multilevel SVM, as only the three-level SVM calculations are performed. Conventional

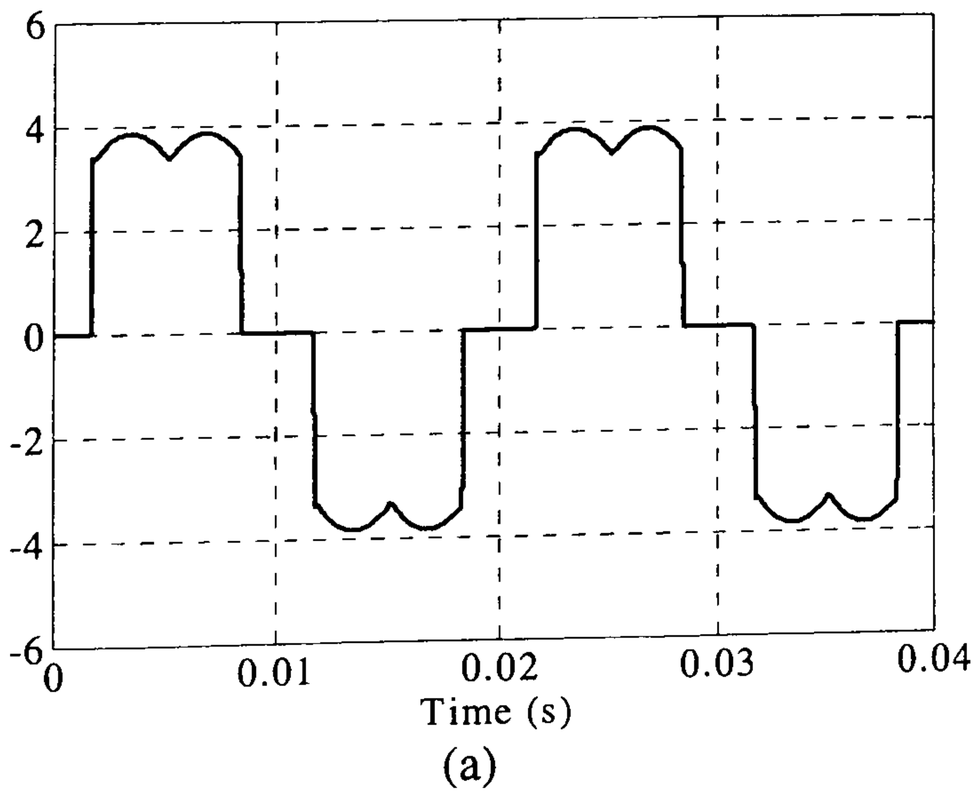
three-level SVM is applied to both the upper three cells as a group and the lower as the second group of the three-phases. A pre-calculated shift in time is introduced into the up-down counters of each switch group, then the output is summed and the required output voltage is obtained. For the *m*-level inverter, *(m-1)/2* up-down counters are used with a phase shift of $T_{sw}/2(m-1)$ introduced between the counters. The main advantage of using H-SVM in the five-level shunt APF is that symmetrical loading of capacitors can be achieved as all the cells contributed to the active filter current in each switching cycle. The penalty of using this PWM technique is the switching loss and output *dv/dt* are increased relative to conventional multilevel SVM. Five-level H-SVM has been discussed in detail in chapter six.

10.7 Simulation results for H-SVM

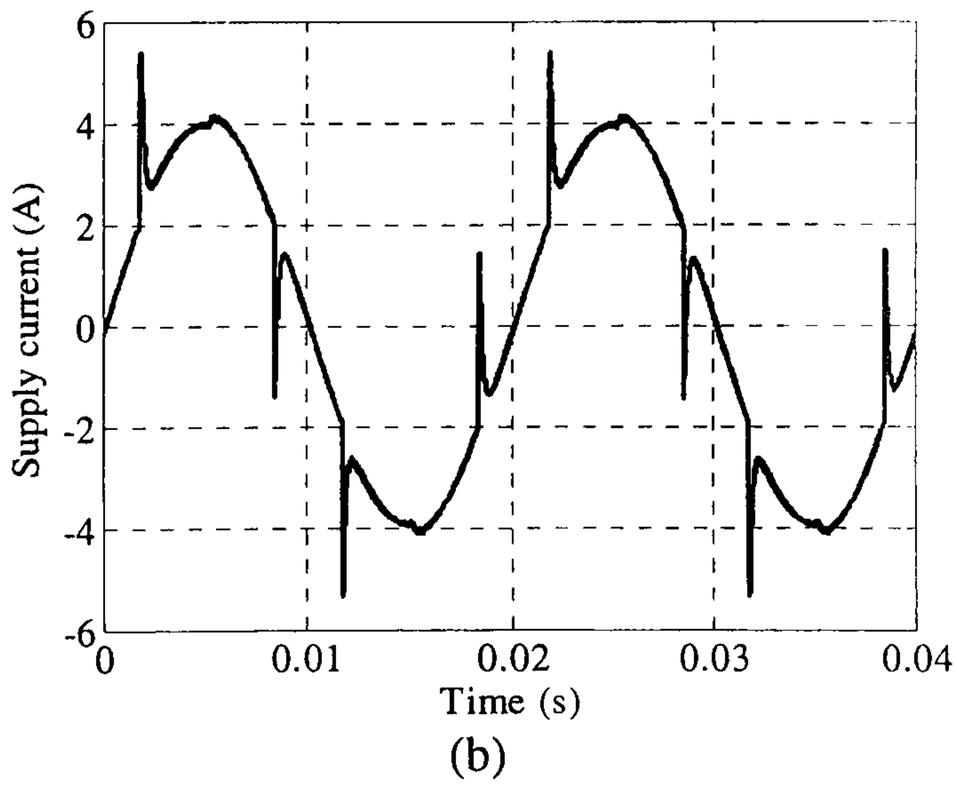
The system main parameters are shown in Table 10.3. Parts a to f of figure (10.13) show the load current, supply current, active filter current, and inverter output line voltage and its spectrum respectively. Parts a-f of figure (10.14) show the six capacitor voltages.

Table 10.3. The system parameters

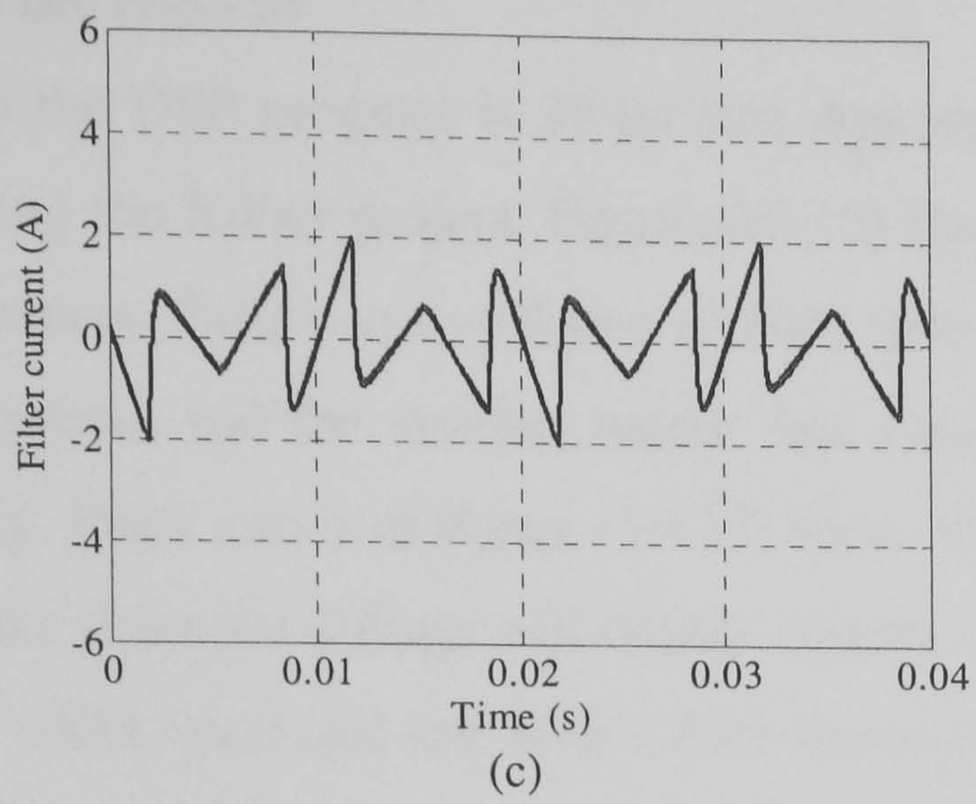
V_{DC}^{*}	100	V
Supply voltage	110	V
C	2200	μF
L	10	mH
Sampling frequency	24.42	kHz
Switching frequency	12.21	kHz



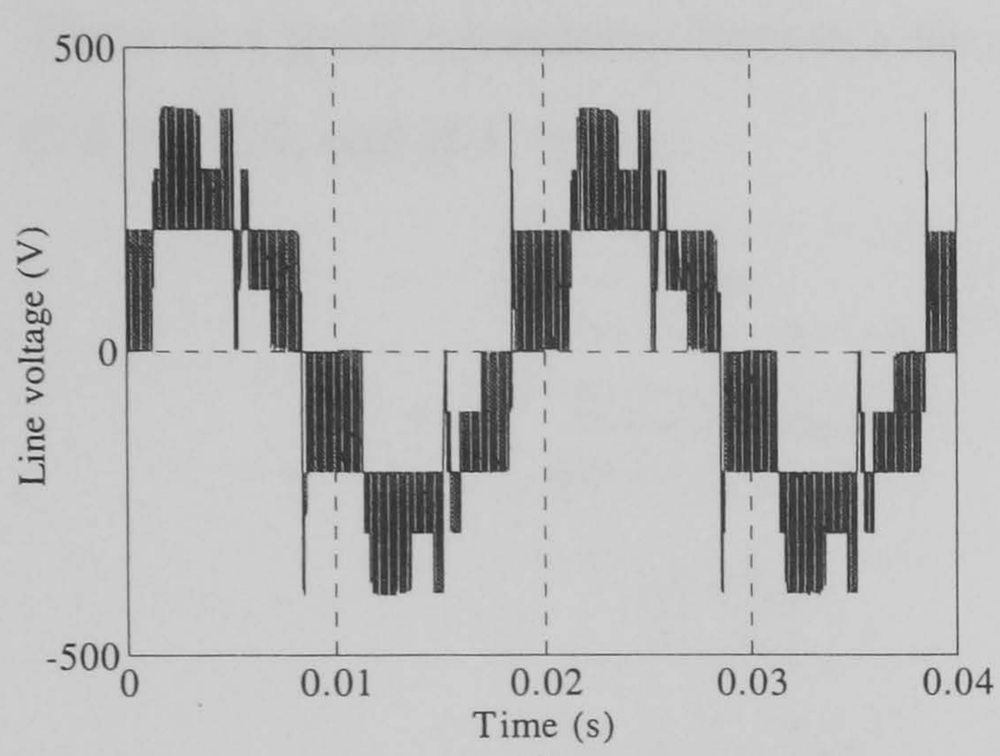
(a)



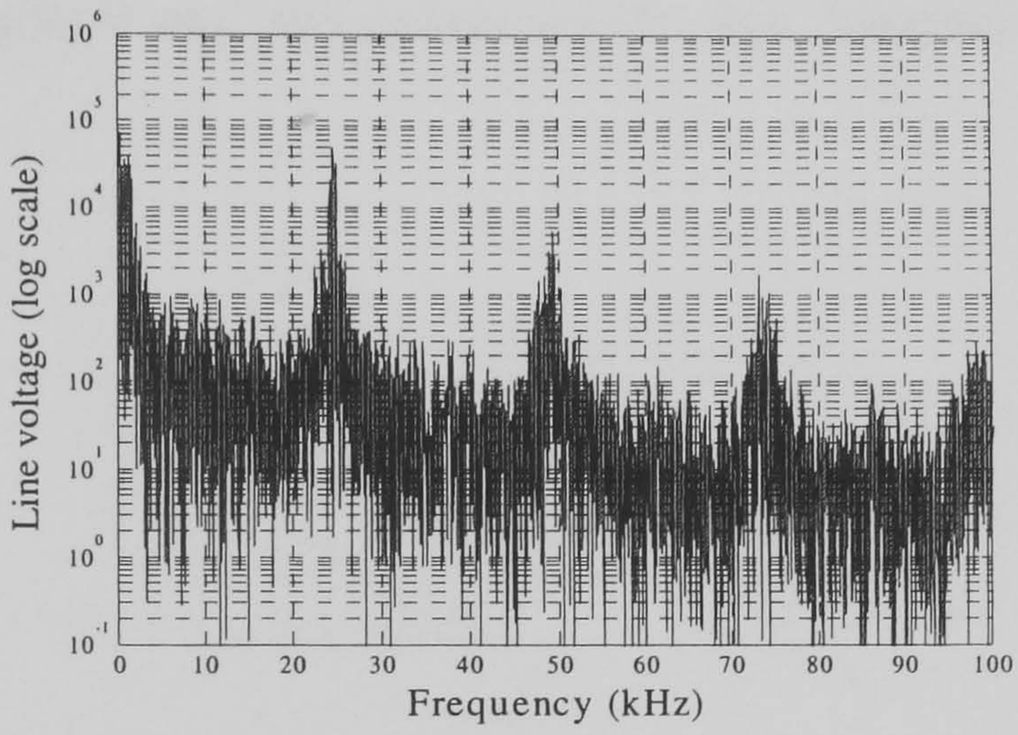
(b)



(c)

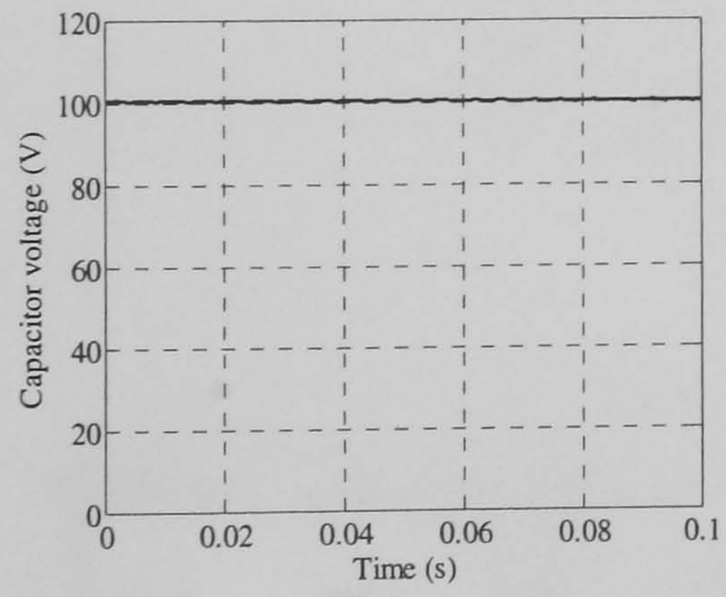


(d)

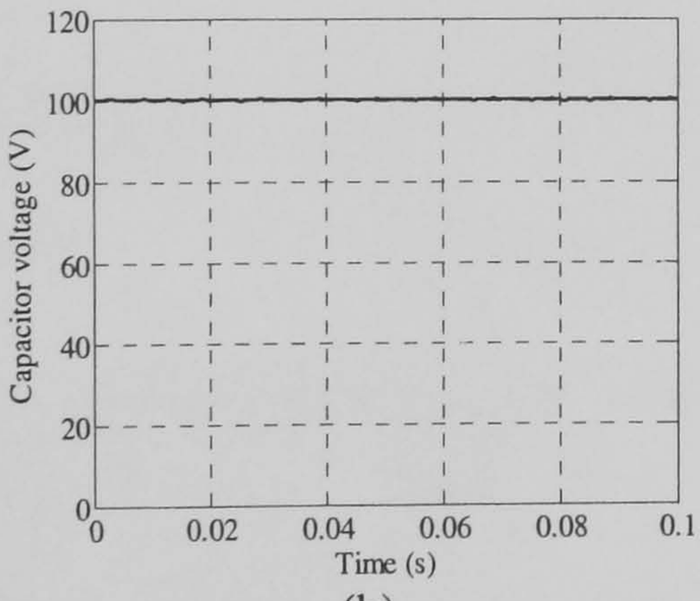


(e)

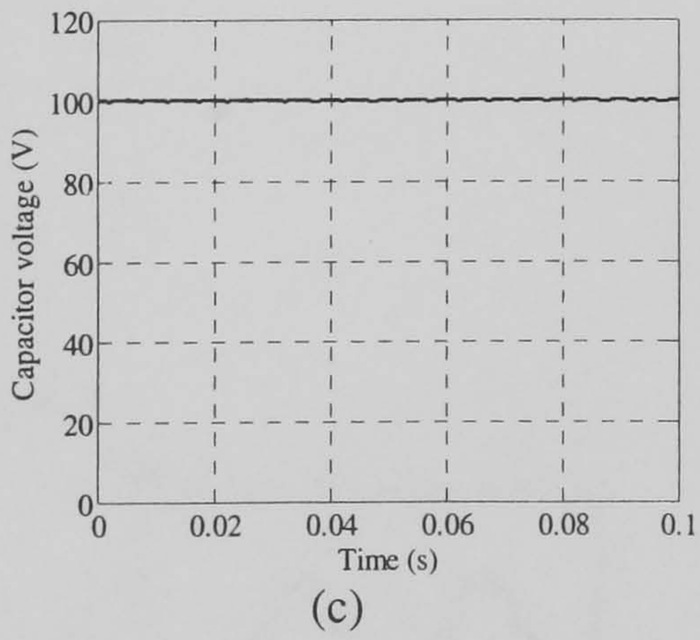
Figure 10.13. Five-level H-SVM simulation results:
(a) load current, (b) supply current, (c) active filter current, (d) inverter output line voltage, and (e) its spectrum



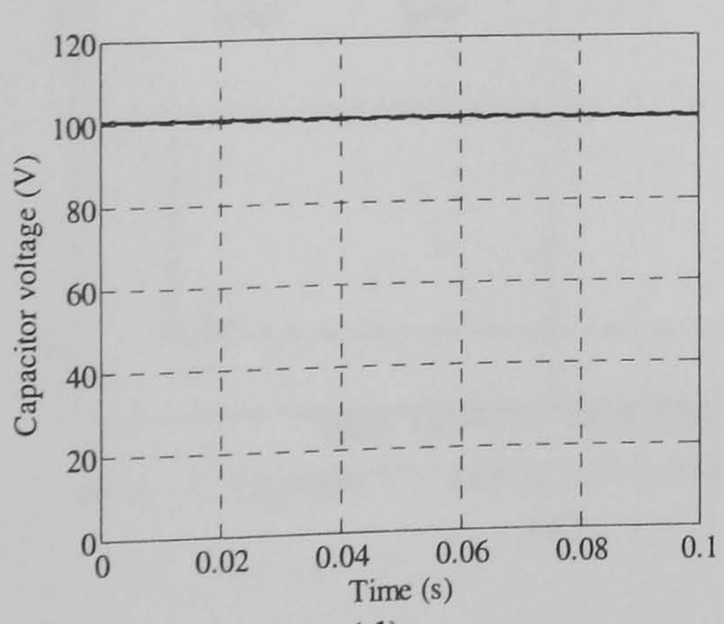
(a)



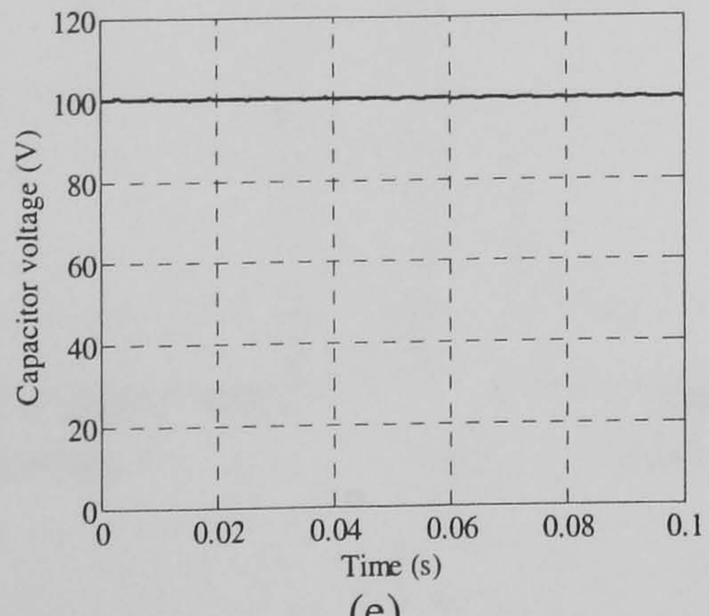
(b)



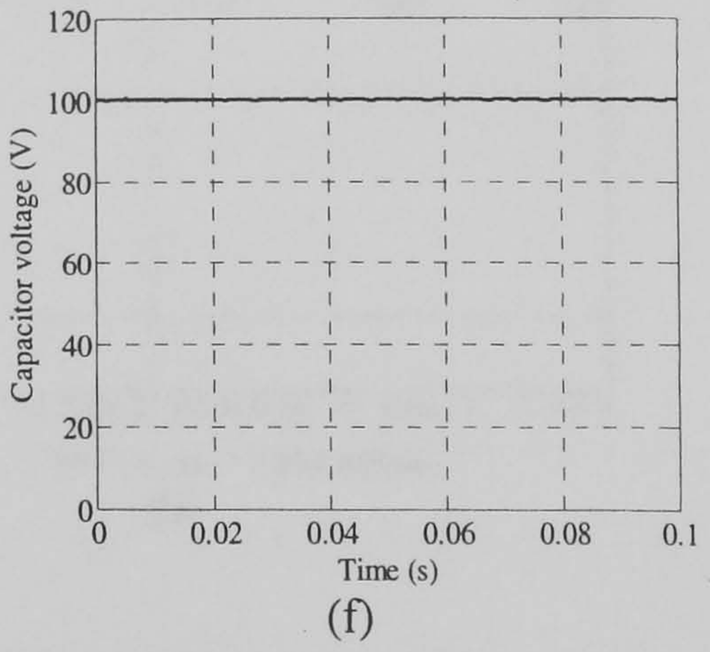
(c)



(d)



(e)



(f)

Figure 10.14. Five-level H-SVM simulation results for the capacitor voltages:
(a) v_{dca1}, (b) v_{dcb1}, (c) v_{dcc1}, (d) v_{dca2} (e) v_{dcb2}, and (f) v_{dcc2}

10.8 Practical results for H-SVM

The execution time of the DSP program is 39 μs (see Appendix F.2). A dead time of 640 ns is provided using the Xilinx project. Figure (10.15) shows the flow chart of the practical system procedures. Parts a to d of figure (10.16) show the load current, supply current, active filter current and the inverter output line voltage and the spectrum in each case, respectively. Parts a to c of figure (10.17) show the six capacitor voltages. Figure (10.18) show the capacitor voltage and supply current of phase 'a' due to a load resistance increase of 100% (part (a)) and then a 50% decrease (part (b)), respectively. There is a good agreement between the practical and simulation results. See Appendix G.4 for R-L and R-C loads.

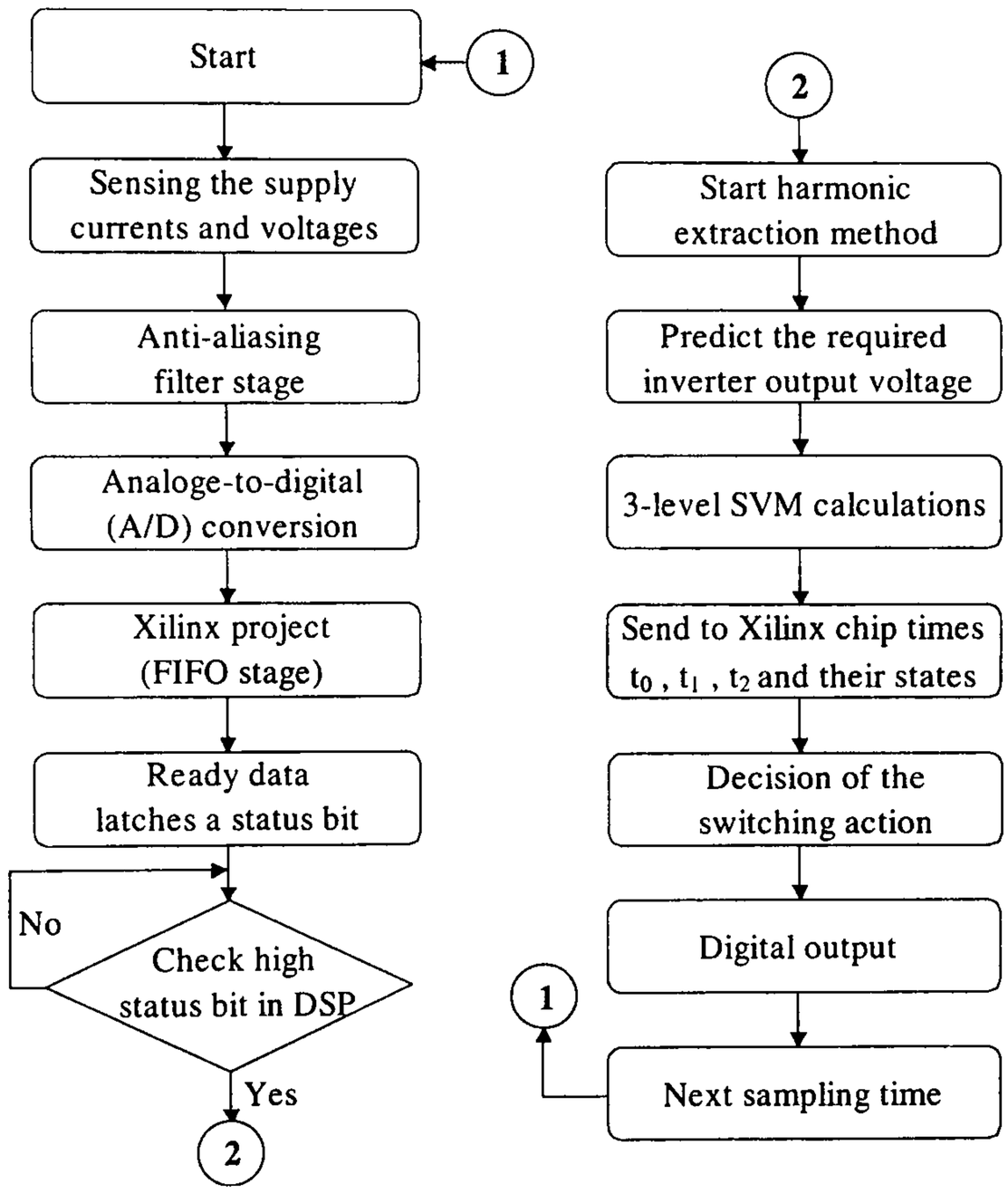
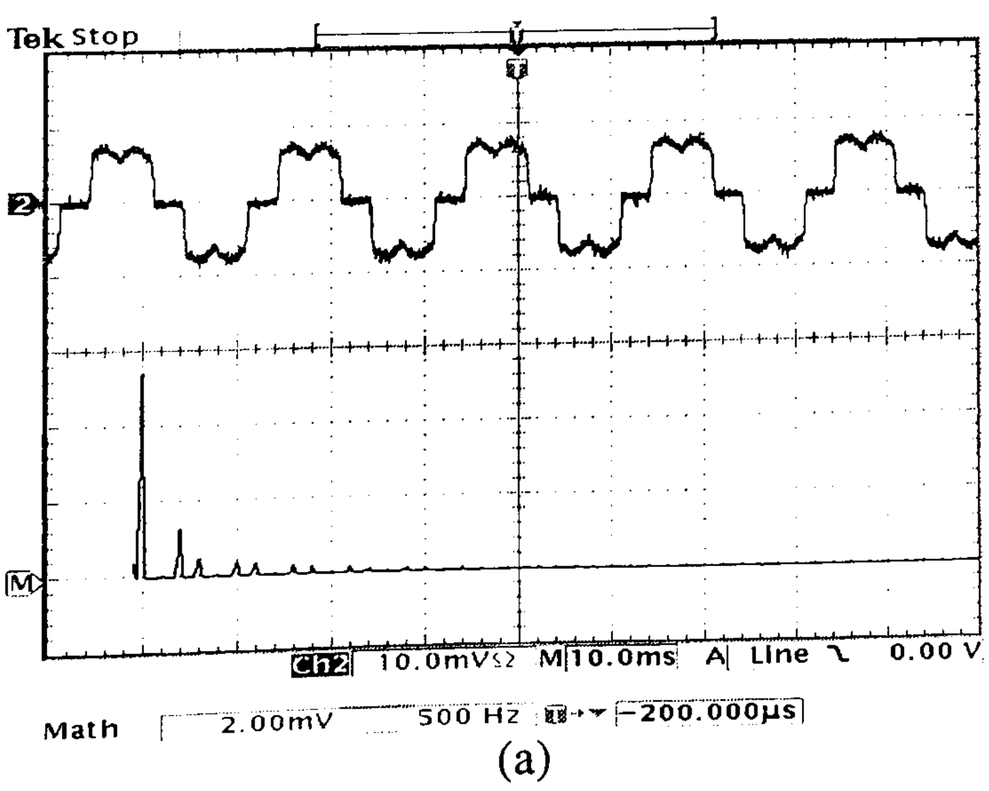
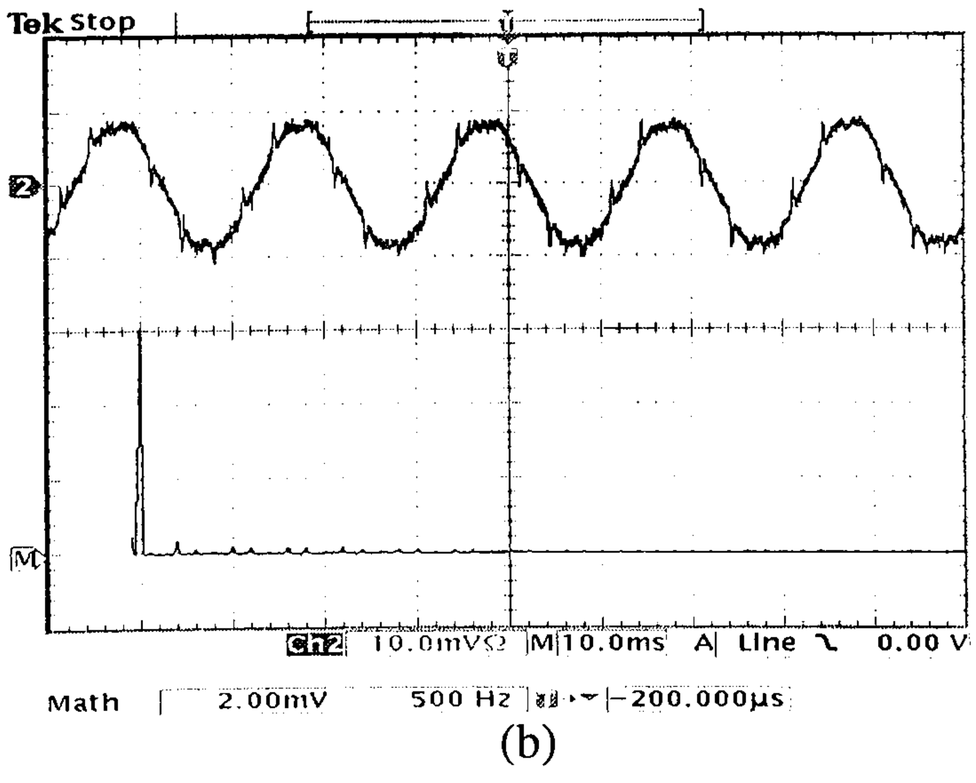


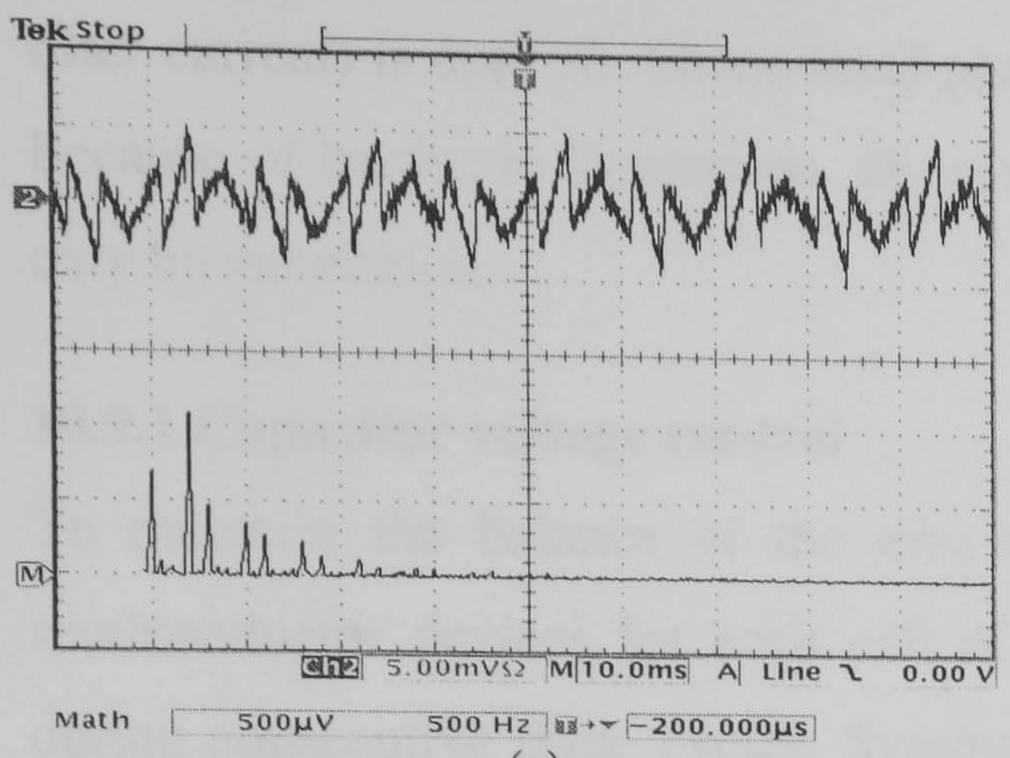
Figure 10.15. Practical system flow chart



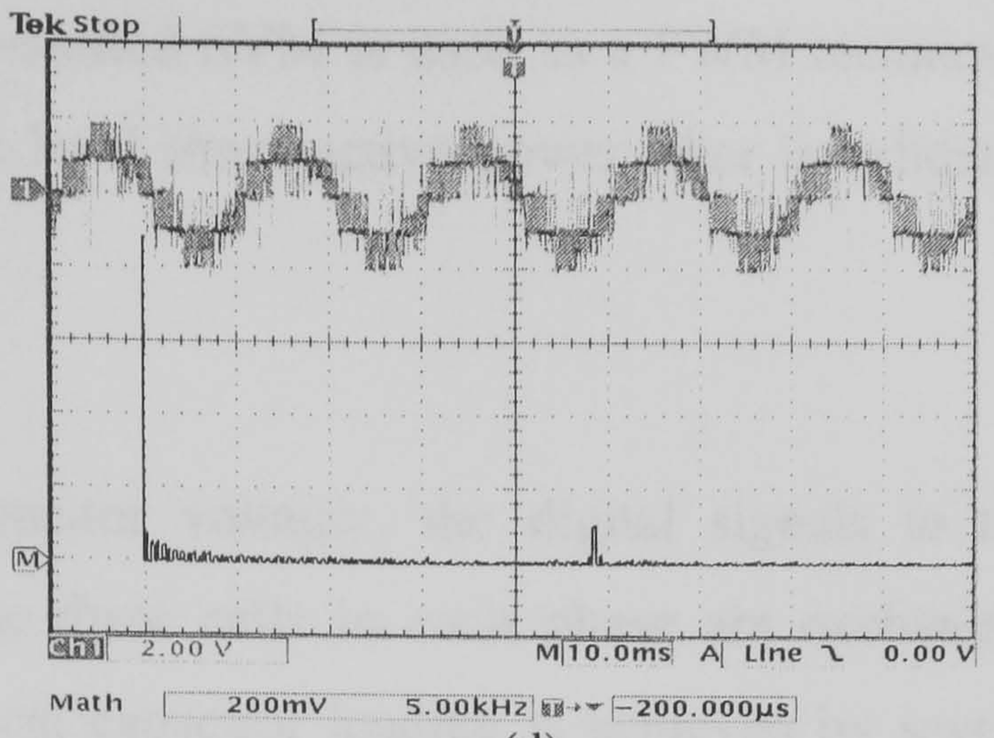
(a)



(b)

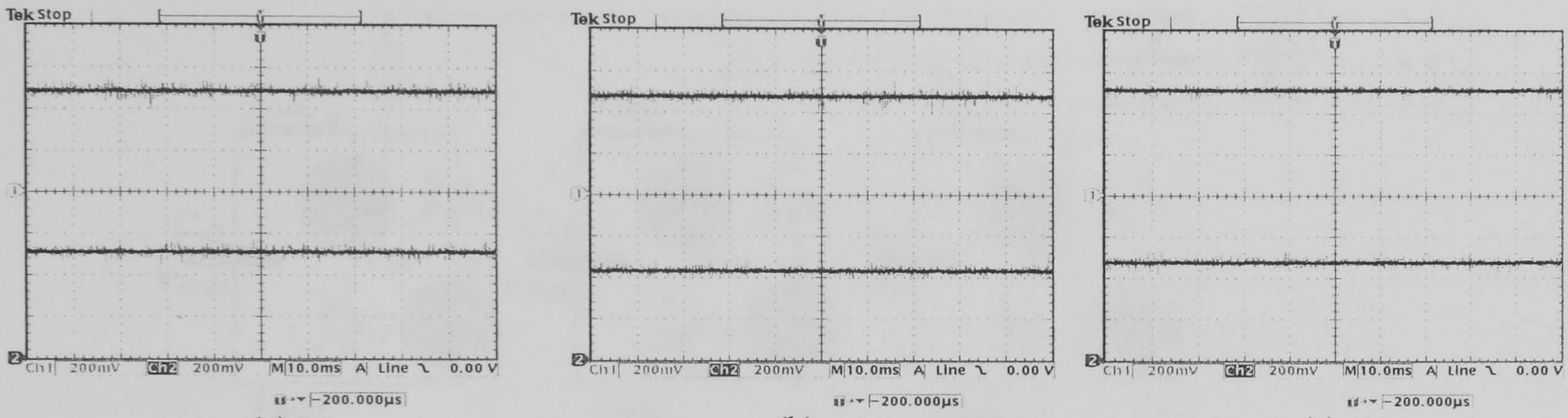


(c)



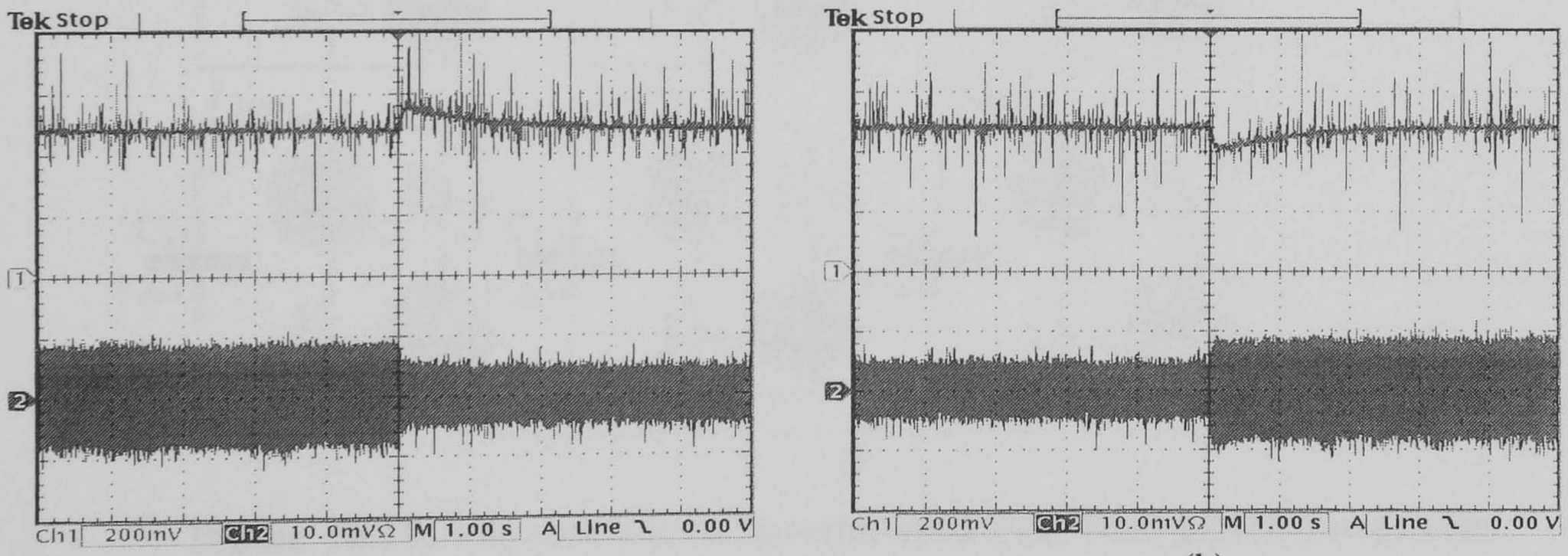
(d)

Figure 10.16. Five-level H-SVM practical results:
(a) the load current and its spectrum (5A/div), (b) the supply current and its spectrum (5A/div), (c) the active filter current and its spectrum (2.5A/div), and (d) the inverter output line voltage (400 V/div)



(a) (b) (c)

Figure 10.17. The six capacitor voltages (40 V/div):
(a) v_{dca1} and v_{dca2}, (b) v_{dcb1} and v_{dcb2}, and (c) v_{dcc1} and v_{dcc2}



(a) (b)

Figure 10.18. Phase 'a' capacitor voltage (40 V/div) and supply current (2 A/div) variation due to load resistance change (a) increased by 100% (b) decreased by 50%

10.9 Seven-level Shunt Active Power Filter

The seven-level cascaded type inverter, shown in figure (10.19) is investigated as a shunt power filter. The capacitor voltage control technique used as a harmonic current extraction method for the two-level inverter is extended to the seven-level shunt active power filter. A predictive current controller based on the supply current (not the active

filter current) is applied. Seven-level phase-shifted SVM is used as a PWM technique. Because of hardware limitations, the seven-level shunt active power filter is validated only by simulation.

10.9.1 Capacitor voltage control

To maintain the balance of the nine capacitor voltages, the digital signals to the semiconductor devices for each cell of the three cells in each phase are exchanged during consecutive three cycles. Symmetrical capacitor loading is achieved by seven-level PS-SVM which will be discussed later. Figure (10.20) shows the proposed block diagram.

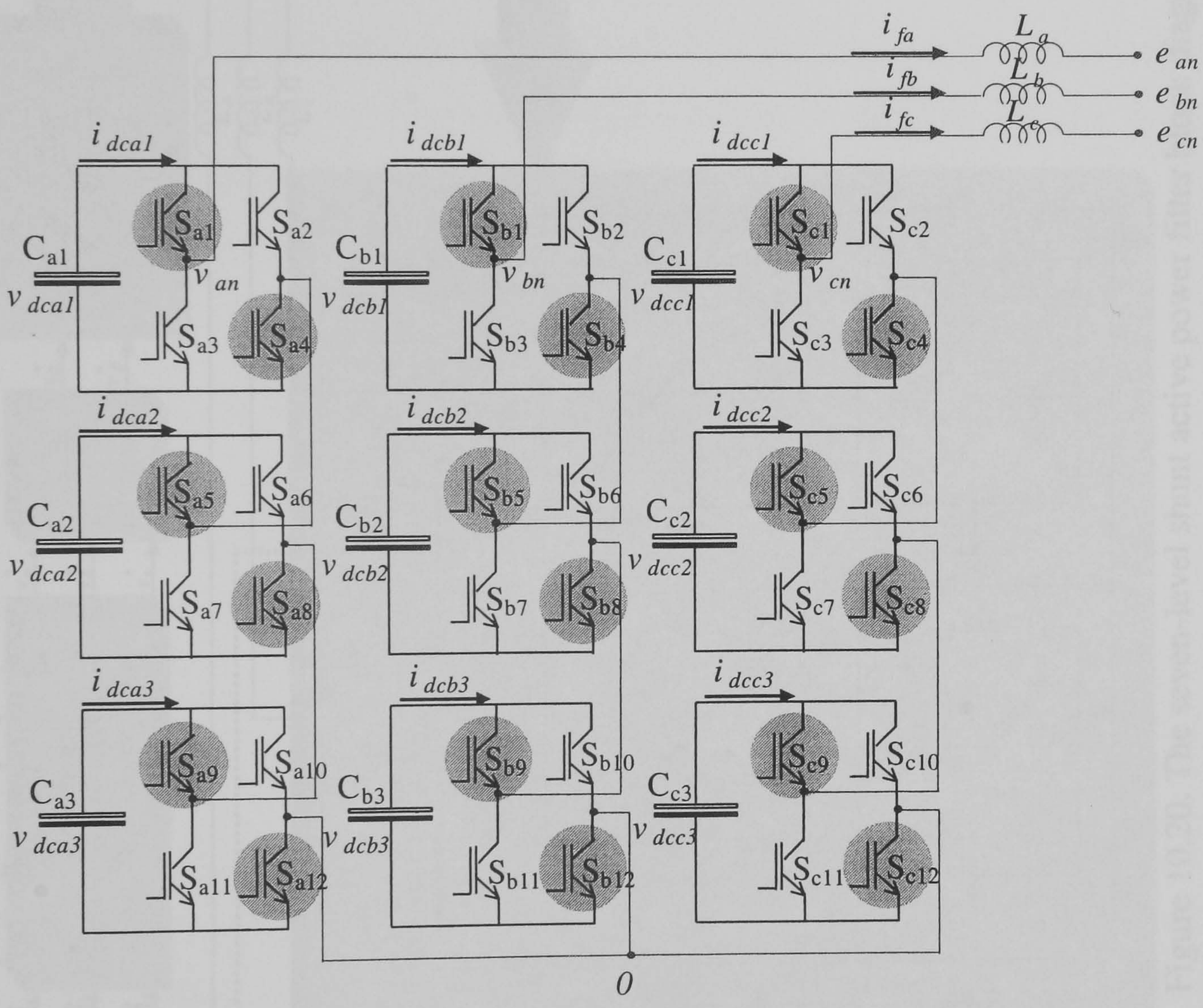


Figure 10.19. The seven-level inverter used as a shunt active power filter (freewheel diodes not shown, main switches shaded)

10.9.2 Seven-level phase-shifted SVM for multilevel inverters

For the seven-level inverter, six up-down counters are used with a phase shift of $T_{sw}/6$ between the counters as shown in figure (10.21). The main advantage of using PS-SVM in the seven-level shunt APF is that capacitor symmetrical loading can be achieved since the switches are turned on and off once each switching cycle. The penalty of using this PWM technique is that the switching loss is increased compared to conventional multilevel SVM.

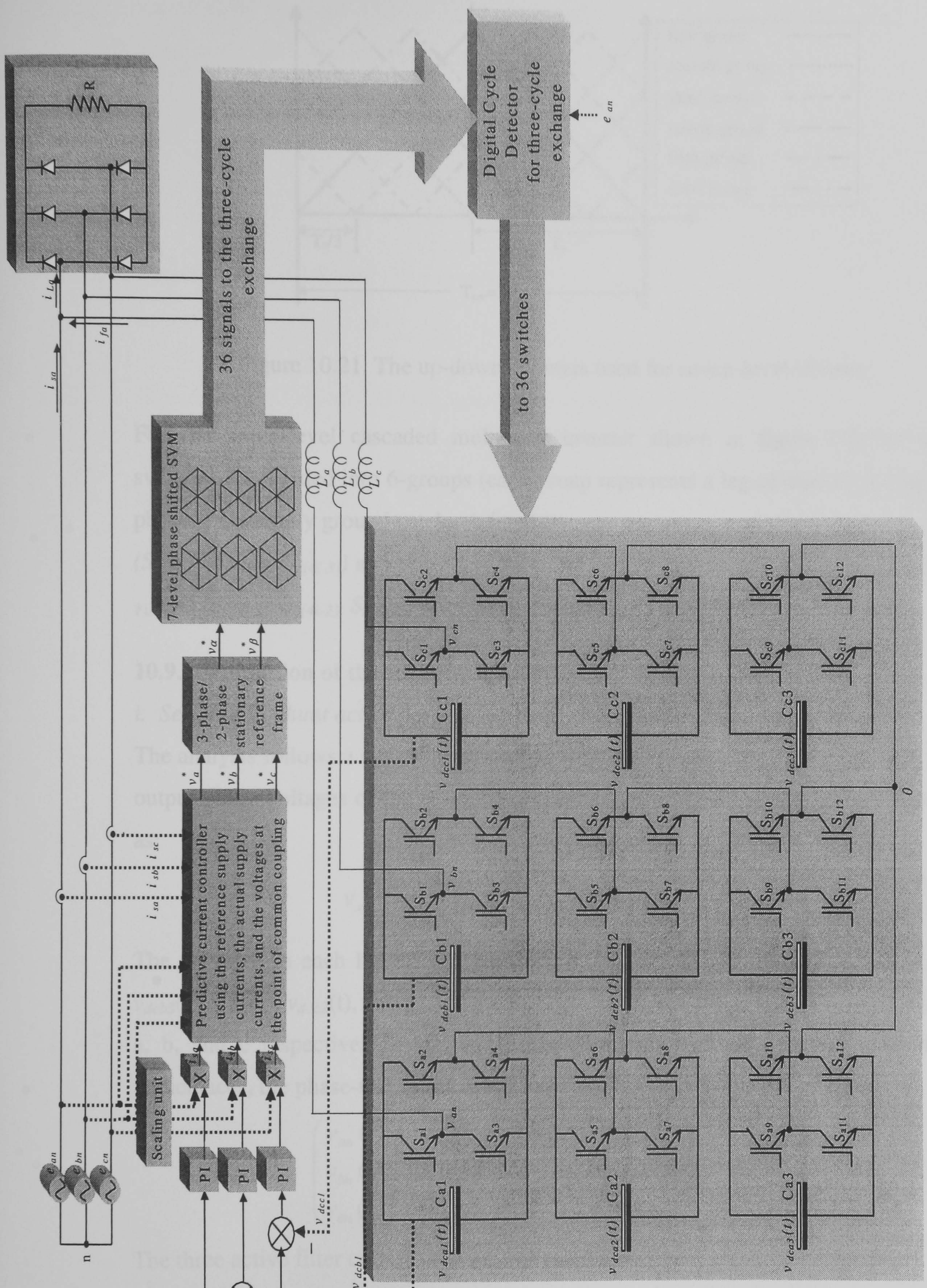


Figure 10.20. The seven-level shunt active power filter block diagram

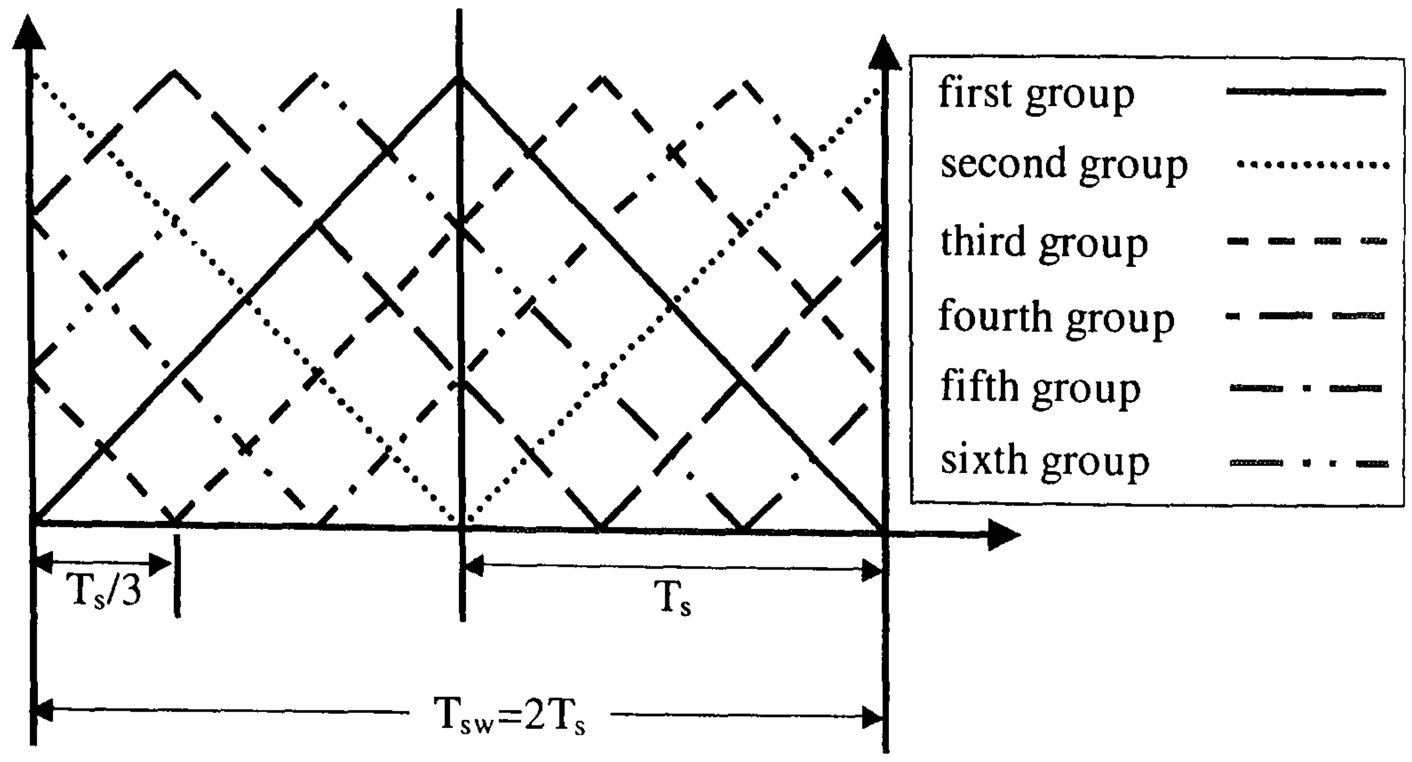


Figure 10.21. The up-down counters used for seven-level inverter

For the seven-level cascaded multilevel inverter shown in figure (10.19), the 36 switches are divided into 6-groups (each group represents a leg of one cell for the three phases). Generally group i can be defined as

$(S_{a(4i-3)}, S_{b(4i-3)}, S_{c(4i-3)})$ and $(S_{a4i}, S_{b4i}, S_{c4i})$, and their complementary $(S_{a(4i-1)}, S_{b(4i-1)}, S_{c(4i-1)})$ and $(S_{a(4i-2)}, S_{b(4i-2)}, S_{c(4i-2)})$ respectively, where $1 \le i \le 3$.

10.9.3 Simulation of the seven level inverter

i. Seven-level shunt active power filter state-space model

The analysis follows a similar procedure as for the five-level case in section 10.4.1. The output phase voltages of the seven-level inverter shown in figure (10.19) are expressed as:

$$v_{x0}(t) = \sum_{i=1}^{3} v_{dcxi}(S_{x(4i-3)} - S_{x(4i-2)}) \tag{10.13}$$

The switches in each leg are complementary. v_{dca1}(t), v_{dca2}(t), v_{dca3}(t), v_{dcb1}(t), v_{dcb2}(t), v_{dcb3}(t), v_{dcc1}(t), v_{dcc2}(t), and v_{dcc3}(t) are the instantaneous capacitor voltages of the phases a, b, and c respectively. Assuming balanced supply voltages and equal interfacing inductances, the phase-to-neutral voltage are:

$$\begin{pmatrix} v_{an}(t) \\ v_{bn}(t) \\ v_{cn}(t) \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}\begin{pmatrix} v_{a0}(t) \\ v_{b0}(t) \\ v_{c0}(t) \end{pmatrix} \tag{10.14}$$

The three active filter currents can be expressed as:

$$L\frac{di_{fx}(t)}{dt} = v_{xn}(t) - e_{xn}(t) \qquad where\ x = a, b\ or\ c \tag{10.15}$$

Equation (8.10) shows three independent currents. In simulation, the three currents must be checked to sum to zero. Equation (8.9) cannot be used for either unbalanced supply

voltages or unequal interfacing inductances. The nine capacitor currents can be expressed in terms of the filter currents i_{fa}, $i_{fb,}$ and i_{fc} as:

$$i_{dcxi}(t) = \left[s_{x(4i-3)} - s_{x(4i-2)}\right] i_{fx}(t) \qquad i = 1, 2, 3 \tag{10.16}$$

The nine capacitor voltages are

$$i_{dcxi}(t) = -C_{xi} \cdot \frac{dv_{dcxi}(t)}{dt} \tag{10.17}$$

Substituting (10.16) into (10.17) yields

$$-C_{xi} \cdot \frac{dv_{dcxi}(t)}{dt} = \left[s_{x(4i-3)} - s_{x(4i-2)}\right] i_{fx}(t) \tag{10.18}$$

Equations (10.15) and (10.18) represent the state-space model in the form

$$\dot{X} = A.X + B.U \tag{10.19}$$

where the sparse matrix A is defined as

$$A = \begin{bmatrix} 0 & A_{12} & A_{13} & A_{14} \\ A_{21} & 0 & 0 & 0 \\ A_{31} & 0 & 0 & 0 \\ A_{41} & 0 & 0 & 0 \end{bmatrix} \tag{10.20}$$

The 4-by-4 sub-matrices A_{11}, A_{12}, A_{21}, and A_{22} are defined as

$$A_{12} = \begin{bmatrix} \frac{2(s_{a1} - s_{a2})}{3L} & \frac{2(s_{a5} - s_{a6})}{3L} & \frac{2(s_{a9} - s_{a10})}{3L} \\ \frac{(s_{a2} - s_{a1})}{3L} & \frac{(s_{a6} - s_{a5})}{3L} & \frac{(s_{a10} - s_{a9})}{3L} \\ \frac{(s_{a2} - s_{a1})}{3L} & \frac{(s_{a6} - s_{a5})}{3L} & \frac{(s_{a10} - s_{a9})}{3L} \end{bmatrix},$$

$$A_{13} = \begin{bmatrix} \frac{(s_{b2} - s_{b1})}{3L} & \frac{(s_{b6} - s_{b5})}{3L} & \frac{(s_{b10} - s_{b9})}{3L} \\ \frac{2(s_{b1} - s_{b2})}{3L} & \frac{2(s_{b5} - s_{b6})}{3L} & \frac{2(s_{b9} - s_{b10})}{3L} \\ \frac{(s_{b2} - s_{b1})}{3L} & \frac{(s_{b6} - s_{b5})}{3L} & \frac{(s_{b10} - s_{b9})}{3L} \end{bmatrix}, A_{14} = \begin{bmatrix} \frac{(s_{c2} - s_{c1})}{3L} & \frac{(s_{c6} - s_{c5})}{3L} & \frac{(s_{c10} - s_{c9})}{3L} \\ \frac{(s_{c2} - s_{c1})}{3L} & \frac{(s_{c6} - s_{c5})}{3L} & \frac{(s_{c10} - s_{c9})}{3L} \\ \frac{2(s_{c1} - s_{c2})}{3L} & \frac{2(s_{c5} - s_{c6})}{3L} & \frac{2(s_{c9} - s_{c10})}{3L} \end{bmatrix}$$

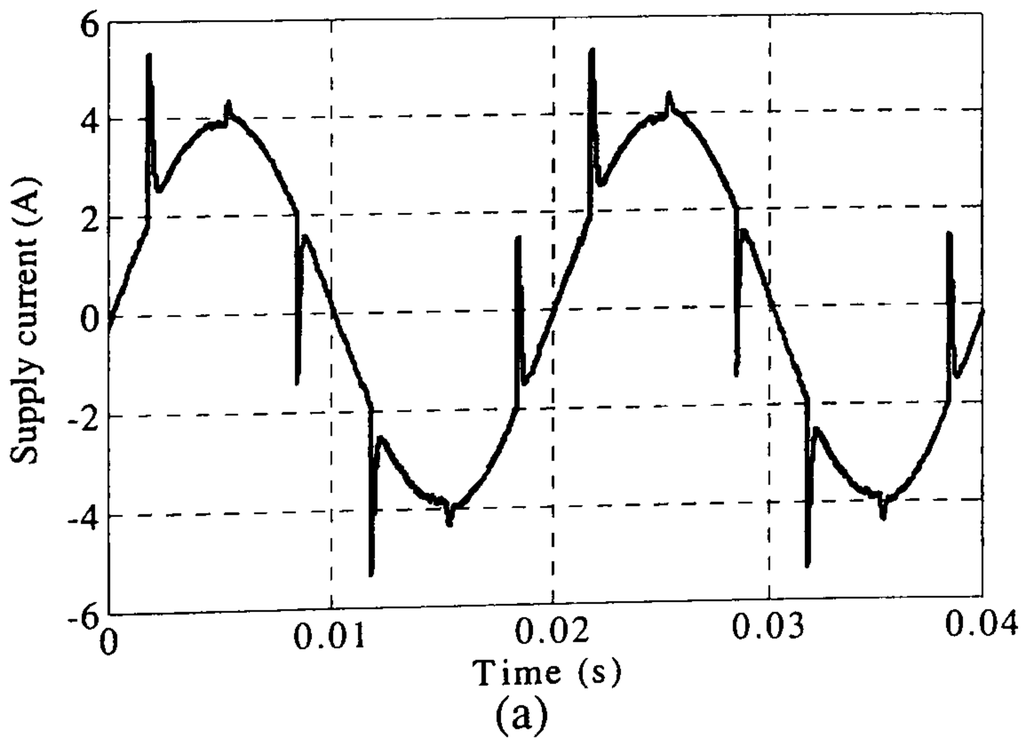
$$A_{21} = \begin{bmatrix} \frac{(s_{a2} - s_{a1})}{C_{a1}} & 0 & 0 \\ \frac{(s_{a6} - s_{a5})}{C_{a2}} & 0 & 0 \\ \frac{(s_{a10} - s_{a9})}{C_{a3}} & 0 & 0 \end{bmatrix}, A_{31} = \begin{bmatrix} 0 & \frac{(s_{b2} - s_{b1})}{C_{b1}} & 0 \\ 0 & \frac{(s_{b6} - s_{b5})}{C_{b2}} & 0 \\ 0 & \frac{(s_{b10} - s_{b9})}{C_{b3}} & 0 \end{bmatrix}, A_{41} = \begin{bmatrix} 0 & 0 & \frac{(s_{c2} - s_{c1})}{C_{c1}} \\ 0 & 0 & \frac{(s_{c6} - s_{c5})}{C_{c2}} \\ 0 & 0 & \frac{(s_{c10} - s_{c9})}{C_{c3}} \end{bmatrix} \tag{10.21}$$

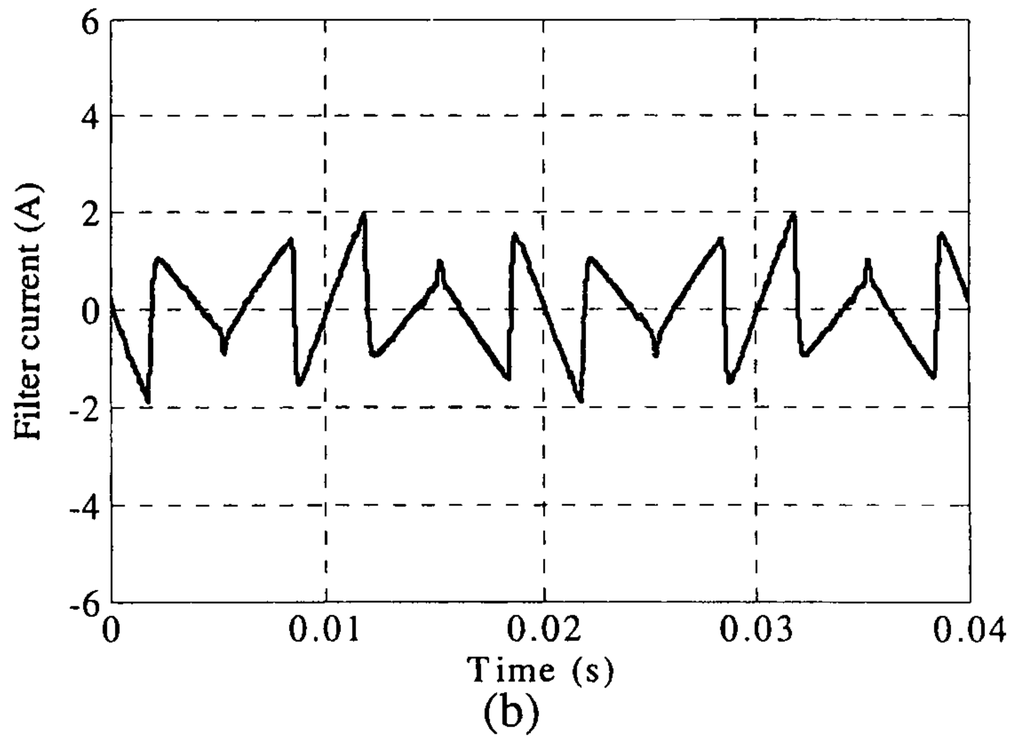
X, B, and U are defined as:

$$X = \begin{bmatrix} i_{fa}(t) \\ i_{fb}(t) \\ i_{fc}(t) \\ v_{dca1}(t) \\ v_{dca2}(t) \\ v_{dca3}(t) \\ v_{dcb1}(t) \\ v_{dcb2}(t) \\ v_{dcb3}(t) \\ v_{dcc1}(t) \\ v_{dcc2}(t) \\ v_{dcc3}(t) \end{bmatrix}, B = \begin{bmatrix} \frac{-1}{L} & 0 & 0 \\ 0 & \frac{-1}{L} & 0 \\ 0 & 0 & \frac{-1}{L} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \text{and } U = \begin{bmatrix} e_a(t) \\ e_b(t) \\ e_c(t) \end{bmatrix} \quad (10.22)$$

ii. Simulation results

The state-space model of the active filter is simulated using Matlab/Simulink. Seven-level PS-SVM is programmed using six *m*-files with *s*-function blocks in Simulink. The same system parameters are used as for the five-level case. Parts a to f of figure (10.22) show the load current, supply current, active filter current, capacitor voltages, and inverter output line voltage and its power spectrum, respectively. As can be seen in figure (10.22e), the first harmonic appears at 72 kHz, six times the switching frequency which improves the effectiveness of the interfacing inductance, enabling lower inductance.





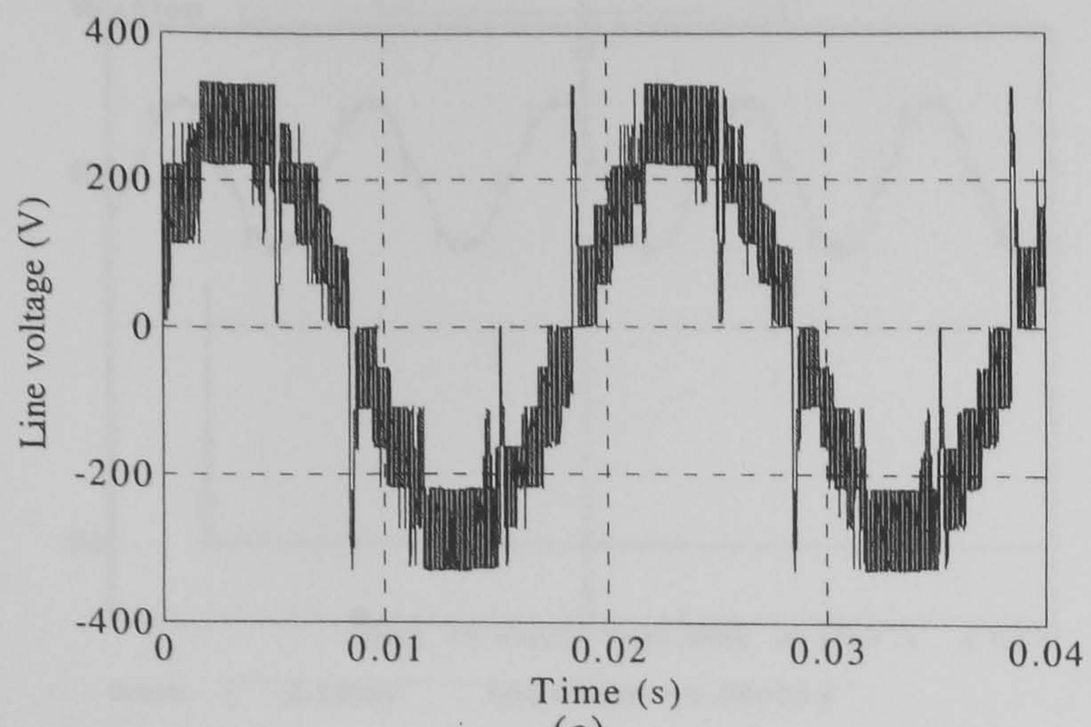
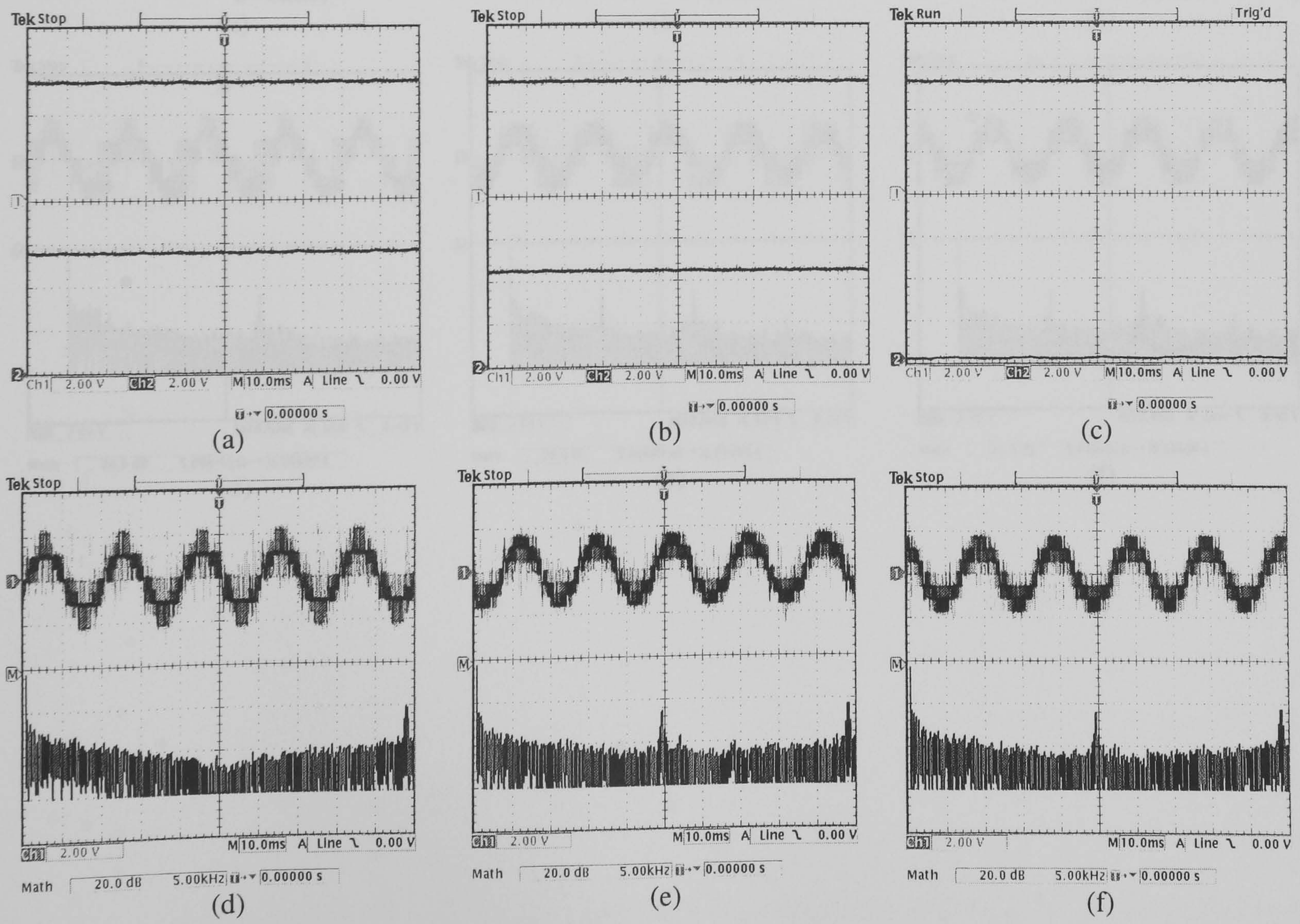
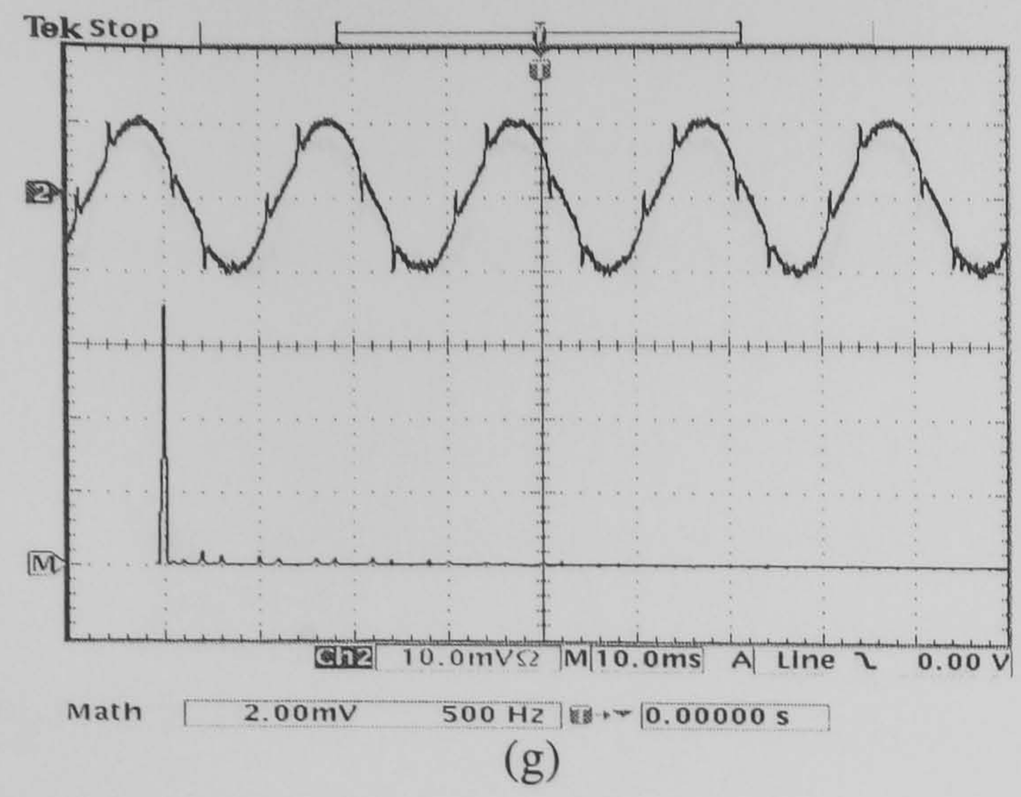


Figure 10.22. Seven-level simulation results:
(a) supply current, (b) filter current, (c) inverter output line voltage, and (d) its power spectrum

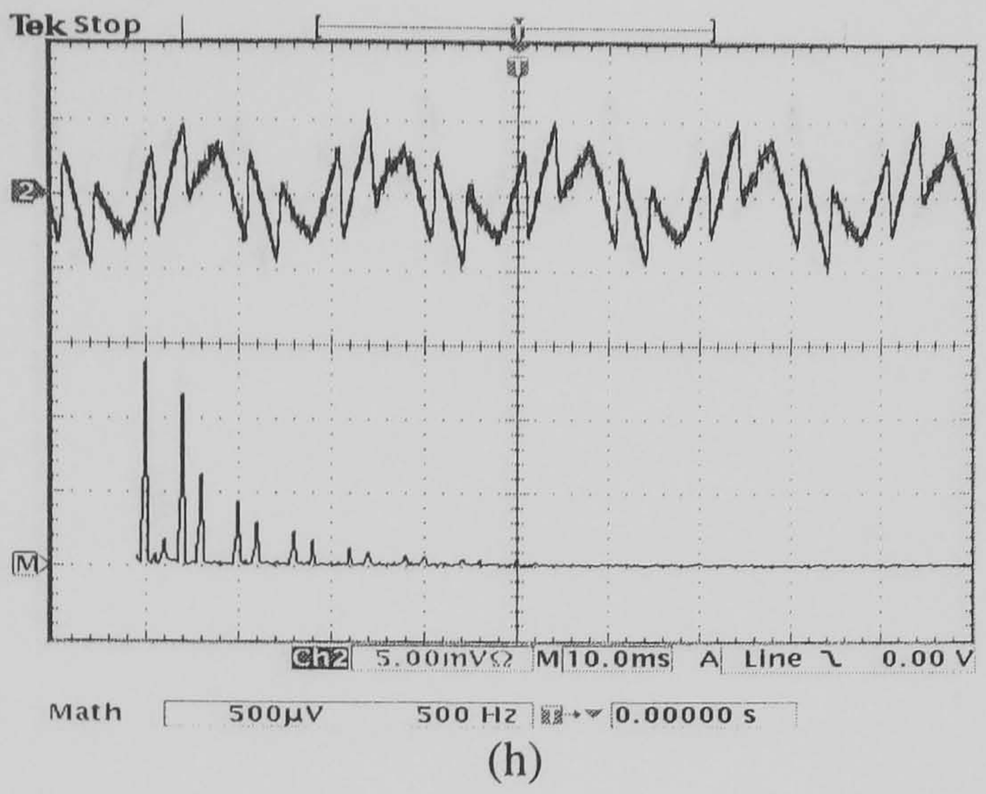
10.10 Cell failure

If an uncontrolled cell fails, the five-level APF can continue to operate provided PS-SVM is employed. Figure (10.23) shows continued operation after the uncontrolled cell of phase 'c' has failed short circuit, using PS-SVM. This feature is not applicable to conventional SVM because of the lack of redundant states. Although operation continues with H-SVM, output performance is poor because control of the complete cell is lost. Figure (10.24) shows continued operation after the uncontrolled cell of phase 'c' has failed short circuit when using H-SVM.



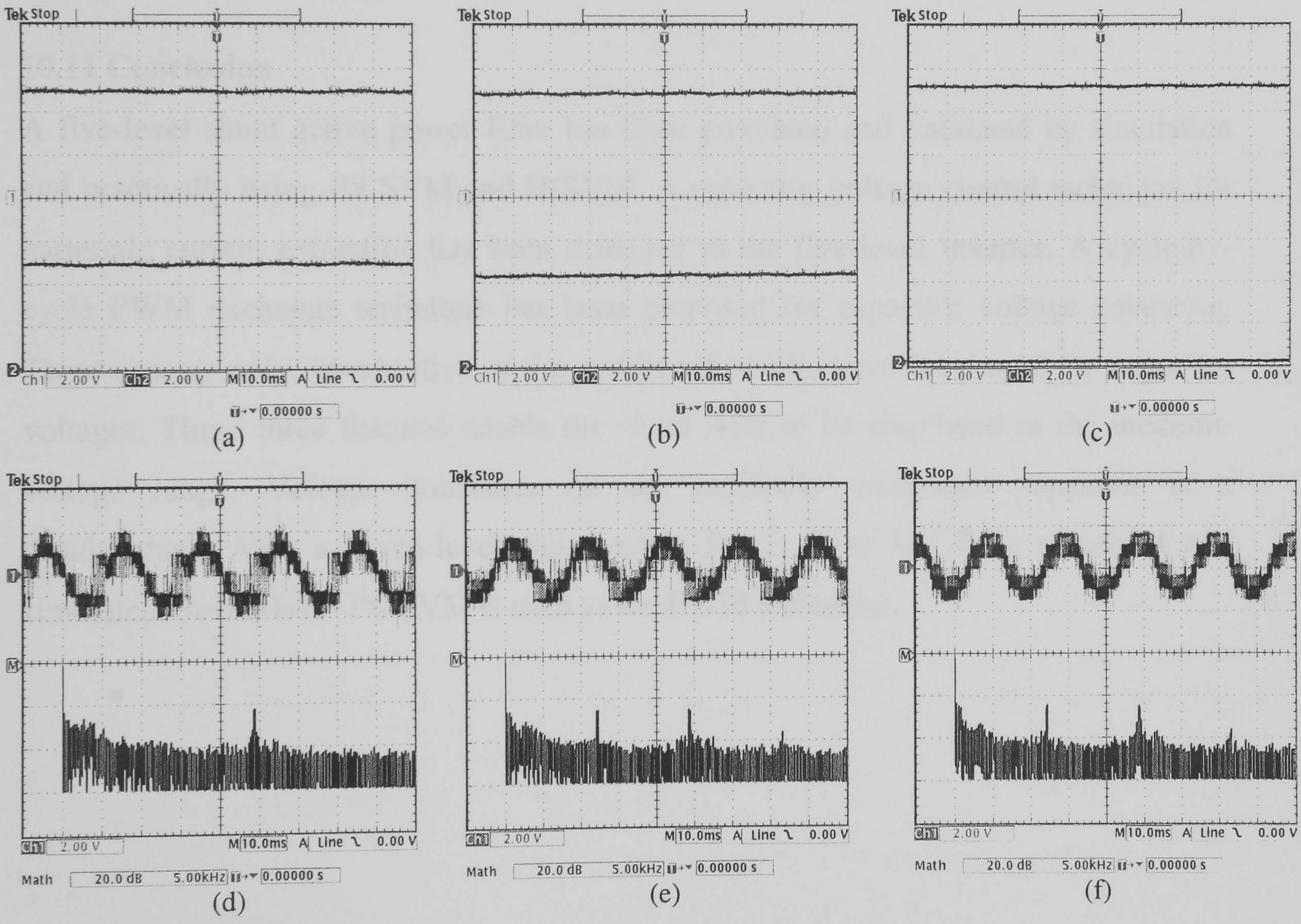


(g)



(h)

Figure 10.23. Cell failure of five-level APF using PS-SVM:
six capacitor voltages (40V/div): (a) v_{dca1} and v_{dca2}, (b) v_{dcb1} and v_{dcb2}, and (c) v_{dcc1} and v_{dcc2}
inverter line voltages (200V/div): (d)v_{ab}, (e) v_{bc}, and (f) v_{ca}
(g) supply current and its spectrum (5A/div), and (h) active filter current and its spectrum (2.5A/div).



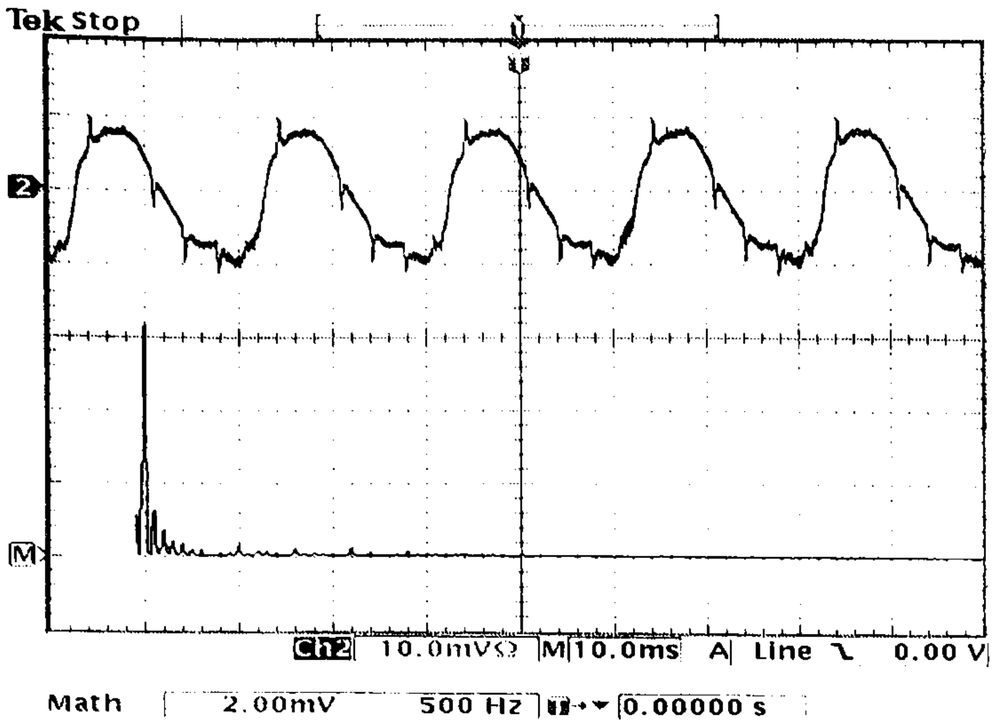


Figure 10.24. Cell failure of five-level APF using H-SVM:
six capacitor voltages (40V/div): (a) v_{dca1} and v_{dca2}, (b) v_{dcb1} and v_{dcb2}, and (c) v_{dcc1} and v_{dcc2}
inverter line voltages (200V/div): (d)v_{ab}, (e) v_{bc}, and (f) v_{ca}
(g) supply current and its spectrum (5A/div), and (h) active filter current and its spectrum (2.5A/div).

10.11 Conclusion

A five-level shunt active power filter has been presented and validated by simulation and practically using PS-SVM and H-SVM. A capacitor voltage control technique for harmonic current extraction has been extended to the five-level inverter. A cycle-by-cycle PWM exchange technique has been proposed for capacitor voltage balancing. Three sensors only, irrespective of the number of levels, have been used for capacitor voltages. These three features enable the shunt APF to be employed in the medium-voltage range. Voltage imbalance on the indirectly controlled capacitor is a disadvantage. Also a seven-level shunt active power filter has been presented and simulated. Seven-level PS-SVM is used as the PWM technique.

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Chapter 11

Conclusion

11.1 General conclusion

This thesis has addressed the use of the multilevel inverter as a shunt active power filter, in order to extend the filter rating to the medium voltage range. A general review of multilevel inverter types and their open loop modulation techniques has been presented. A comparison between inverters with series connected power semiconductor devices and the multilevel structure has been presented. A generalized approach for conduction loss calculation with carrier based pulse width modulation has been presented. A generalized and systematic approach for the generation of multilevel space vector modulation with a fast, fixed execution time has been proposed. New space vector modulation techniques for the multilevel inverter have been proposed and outlined. A predictive current control technique for the two-level shunt active power filter has been proposed and assessed. The capacitor voltage harmonic current extraction technique for the two-level active power filter has been extended to three-level and five-level active power filters using two different pulse width modulation techniques. A novel balancing technique for the five-level active power filter has been practically implemented, and an extension to the seven-level filter has been simulated.

11.2 Author's Contribution

In chapter three, a comparison between inverters with series connected power semiconductor devices and multilevel structures, as a way to extend the switch rating to medium and high-voltage applications, has been conducted. The multilevel inverter is better in terms of total harmonic distortion, distortion factor, simplicity of gate drive circuits, switching losses, and common mode voltage, than the series connection-based inverter. However both techniques have the same performance in terms of conduction loss.

Also in chapter three, a generalized approach for multilevel inverter conduction loss calculation for carrier based PWM techniques, has been presented. This approach can be used for any modulating or carrier signal, and can be used for SVM by applying it to triplen harmonic injected PWM.

In chapter five, a generalized theory for multilevel SVM has been presented. This theory is based on a systematic numerical analysis algorithm with fast, fixed DSP

execution time, independent of the number of levels. In addition, the algorithm procedures, saves the complexity faced with multilevel SVM implementation.

In chapter six, innovative SVM approaches for multilevel inverters have been proposed. Phase shifted SVM has been proposed. It has the same features as the PS-carrier based PWM. It is simple to implement but needs *(m-1)* up-down counters for an *m*-level inverter and the switching loss is *m-1* times that with conventional multilevel SVM. Hybrid SVM has been proposed and has the same features as hybrid carrier based PWM. In this technique, three-level SVM is used *(m-1)/2* times with *(m-1)/2* shifted up-down counters with an *m*-level inverter. The switching losses are *(m-1)/2* times those with conventional multilevel SVM. Mapped phase shifted SVM uses only one up counter, instead of *(m-1)* up-down counters in phase shifted SVM, by mapping the corresponding states of the shifted up-down counters to one up counter, giving the same result. Mapped hybrid SVM for the five-level inverter has been considered using one up-down counter instead of two as would be used with hybrid-SVM. The short execution time is the main feature of the new SVM algorithms.

In chapter eight, predictive current control for the two-level shunt active power filter has been investigated. The capacitor voltage control technique for harmonic current extraction is used with SVM as a PWM technique.

In chapter nine, the capacitor voltage control technique for the two-level shunt active power filter has been extended to the three-level cascaded type shunt active power filter. Two different SVM techniques have been used, phase shifted SVM and hybrid SVM. The first is easier to be implemented when using mapped phase shifted SVM. Good filtering performance is possible with the two techniques.

In chapter ten, the capacitor voltage control technique has been extended to levels higher than three with the proposed method using three capacitor voltage sensors, independent of the number of levels (cells). Two different SVM techniques have been used, viz., phase shifted SVM and hybrid SVM for the five-level shunt active power filter. The later can be replaced by the mapped hybrid SVM for ease of implementation. The simulation results for the seven-level shunt active power filter have been presented to validate the concept of capacitor voltage balance for levels higher than five.

11.3 Future research

- The application of the multilevel inverter should be assessed for replacement of the series connection method used for the high voltage DC transmission (HVDC).
- Investigation of the application of conventional SVM for capacitor voltage balancing of the diode clamping multilevel inverter for levels higher than three, using the generalised theory of multilevel SVM.
- Investigate the capacitor voltage balance in the five-level inverter, solving voltage imbalance of the lower three capacitor voltages.
- Extend the voltage rating of the practical test rig used for the five-level APF.
- Identifying a compromise between the APF bandwidth and its losses.

Appendix A

Generalized algorithm for multilevel SVM

```
% Generalized algorithm for multilevel SVM

function [sys,x0,str,ts] = new_algorithm(t,x,u,flag,mf)
mf=4*60;
switch flag,
  %%%%%%%%%%%%%%%%%%%%
  % Initialization %
  %%%%%%%%%%%%%%%%%%%%
% Initialize the states, sample times, and state ordering strings.
case 0
   [sys,x0,str,ts]=mdlInitializeSizes(mf);
case 2,
   sys=mdlUpdate(t,x,u,mf);

case 3
   sys=mdlOutputs(t,x,u,mf);

case 4,
   sys=mdlGetTimeOfNextVarHit(t,x,u,mf);

case { 1,9 }
  sys=[];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Unexpected flags (error handling)%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  % Return an error message for unhandled flag values.
  otherwise
    error(['Unhandled flag = ',num2str(flag)]);
end

function [sys,x0,str,ts] = mdlInitializeSizes(mf)
sizes = simsizes;
sizes.NumContStates  = 0;
sizes.NumDiscStates  = 16;
sizes.NumOutputs     = 3;  % dynamically sized
sizes.NumInputs      = 4;  % dynamically sized
sizes.DirFeedthrough = 1;   % has direct feedthrough
sizes.NumSampleTimes = 1;
sys = simsizes(sizes);
x0  = [0;0;0;0;0;0;0;0;0;0;0;0;0;0;-1;-1;-1];
str = [];
ts  = [-2 0];   % inherited sample time

function sys=mdlUpdate(t,x,u,mf,tss)
tss=0.02/(2*mf);
x(1)=floor(t/(2*tss));
if u(2) >=2*pi
  u(2)=u(2)-2*pi;
else
   u(2)=u(2);
end;

s=floor(u(2)/(pi/3))+1;   %theta to determine the sector
u(2)=u(2)-(s-1)*(pi/3);
```

Appendix A: Generalized algorithm for multilevel SVM

```
% check for over modulation
if u(1)>(((u(3)*(u(4)-1)*cos(pi/6))/(sin(u(2)+pi/3)))-1)
   vi=((u(3)*(u(4)-1)*cos(pi/6))/(sin(u(2)+pi/3))-1);
else
   vi=u(1);
end;

a=floor(vi*cos(u(2)+(pi/6))/(u(3)*cos(pi/6)))+1;  % to determine A
b=floor(vi*cos((pi/6)-u(2))/(u(3)*cos(pi/6)))+1;  % to determine B
h=floor(vi*sin(u(2))/(u(3)*cos(pi/6)))+1;         % to determine H

delta=u(3)^2*cos(pi/6)*(2*a-2*b+2*h-1);
a11=u(3)*cos(pi/6)*(b-h-a);
a12=0.5*u(3)*(-3*a+3*b-3*h+2);
a13=u(3)^2*cos(pi/6)*(a*h+h^2-h+b*a-b^2);

a21=u(3)*cos(pi/6);
a22=-u(3)/2;
a23=-u(3)^2*cos(pi/6)*(b-h);

a31=(a-b+h-1)*u(3)*cos(pi/6);
a32=(3*a-3*b+3*h-1)*0.5*u(3);
a33=u(3)^2*cos(pi/6)*(b^2-a*b-b+2*a-a*h+2*h-1-h^2);

x(3)=tss*(vi*cos(u(2))*a11+vi*sin(u(2))*a12+a13)/delta;
x(4)=tss*(vi*cos(u(2))*a21+vi*sin(u(2))*a22+a23)/delta;
x(5)=tss*(vi*cos(u(2))*a31+vi*sin(u(2))*a32+a33)/delta;

reg=-a+b^2-b+1+h;  % to determine the region number

if s==2 | s==4 | s==6
   are=x(4);
   x(4)=x(5);
   x(5)=are;
else
   x(4)=x(4);
   x(5)=x(5);
end;

x(3)=0.5*x(3);

if x(3)<0.0000001
   x(4)=x(4)-0.0000001+x(3);
   x(5)=x(5)-0.0000001+x(3);
   x(3)=0.0000001;
end;
if x(4)<0.0000001
   x(5)=x(5)-0.0000001+x(4);
   x(4)=0.0000001;
else if x(5)<0.0000001
      x(4)=x(4)-0.0000001+x(5);
      x(5)=0.0000001;
   end;
end;

x(7)=x(3)+2*x(1)*tss;
x(8)=x(4)+x(7);
x(9)=x(5)+x(8);
x(10)=x(3)+x(9);
x(11)=x(3)+x(10);
x(12)=x(11)+x(5);
x(13)=x(12)+x(4);
```

Appendix A: Generalized algorithm for multilevel SVM

```
for k=1:u(4)
   f(1,1,k)=(k-1)*10101;
end;
for n=1:(u(4)-1)
   for j=1:u(4)-n
      for i=1:n
         f(n+1,i,j)=10000*n+100*(i-1)+(j-1)*10101;
      end;
      for i=n+1:2*n
         f(n+1,i,j)=10000*(2*n+1-i)+100*n+(j-1)*10101;
      end;
      for i=2*n+1:3*n
         f(n+1,i,j)=100*n+(i-2*n-1)+(j-1)*10101;
      end;
      for i=3*n+1:4*n
         f(n+1,i,j)=(4*n+1-i)*100+n+(j-1)*10101;
      end;
      for i=4*n+1:5*n
         f(n+1,i,j)=10000*(i-4*n-1)+n+(j-1)*10101;
      end;
      for i=5*n+1:6*n
         f(n+1,i,j)=10000*n+(6*n+1-i)+(j-1)*10101;
      end;
   end;
end;

if b==1
   b1=1.000000000000001;
else
   b1=b;
end;
```

```
      a1=b;
      z2=floor((reg-b*(b-2))/2)+(s-1)*(b-1);
      a2=z2-6*(b-1)*floor((z2-1)/(6*(b1-1)));
      a3=1;     % it can be chosen to be between 1: m-b-1
      a4=b+1-(1-rem(b,2))*rem((s*reg),2)-(1-rem(reg,2))*rem((s*b),2);
      z5=floor((reg+1-b*(b-2))/2)+b*(s-1)+(1-rem(s,2))*[(1-rem(reg,2))*(1-
rem(b,2))+rem(reg,2)*rem(b,2)]-(s-1)*(rem(s*b,2)*(1-rem(reg,2))+rem(s*reg,2)*(1-rem(b,2)));
      a5=z5-6*b*floor((z5-1)/(6*b));
      a6=a3; % it can be chosen to be between 1: m-b-1
      a7=b+1-(1-rem(b,2))*(1-rem(s,2))*rem(reg,2)-(1-rem(reg,2))*(1-rem(s,2))*rem(b,2);
      a8=1+floor((reg-b*(b-2))/2)+(b-1)*(s-1)+(s-1)*rem(s,2)+((1-rem(b,2))*(1-
rem(reg,2))+rem(b,2)*rem(reg,2))*(s-2)*(1-rem(s,2))-6*(b-1)*floor(reg/(b1^2-
1))*floor(s/6)*[rem(reg,2)*(1-rem(b,2))+rem(b,2)*(1-rem(reg,2))];
      a9=a3+(1-rem(b,2))*(1-rem(s,2))*rem(reg,2)+(1-rem(reg,2))*(1-rem(s,2))*rem(b,2);  % it can be
chosen to be between 1: m-b-1
      a10=a1;
      a11=a2;
      a12=a3+1;    % it can be chosen to be between 1: m-b-1

r1=floor(f(a1,a2,a3)/10000);
r2=floor((f(a1,a2,a3)-10000*r1)/100);
r3=f(a1,a2,a3)-10000*r1-100*r2;
r4=floor(f(a4,a5,a6)/10000);
r5=floor((f(a4,a5,a6)-10000*r4)/100);
r6=f(a4,a5,a6)-10000*r4-100*r5;
r7=floor(f(a7,a8,a9)/10000);
r8=floor((f(a7,a8,a9)-10000*r7)/100);
r9=f(a7,a8,a9)-10000*r7-100*r8;

r10=floor(f(a10,a11,a12)/10000);
```

```
r11=floor((f(a10,a11,a12)-10000*r10)/100);
r12=f(a10,a11,a12)-10000*r10-100*r11;

s0=[r1 r2 r3];
s1=[r4 r5 r6];
s2=[r7 r8 r9];
s7=[r10 r11 r12];

if t>=x(7) & t< x(8)
   sout=s1;
else if t>=x(8) & t< x(9)
       sout=s2;
   else if t>=x(9) & t< x(10)
          sout=s7;
       else if t>= x(10) & t< x(11)
              sout=s7;
          else if t>= x(11) & t< x(12)
                 sout=s2;
              else if t>=x(12)&t<x(13)
                     sout=s1;
                  else
                     sout=s0;
                  end;
              end;
          end;
       end;
   end;
end;

%e1(i)=(1/3)*[2*s(i,1)-s(i,2)-s(i,3)];
%  e2(i)=(1/3)*[2*s(i,2)-s(i,1)-s(i,3)];
x(14) = sout(1);
x(15) =sout(2);
x(16) =sout(3);
%e12=e11-e22;
%e55=e11-0.5*e22(i)-0.5*e33(i);
%e66=0.5*(3^0.5)*[e22(i)-e33(i)];
sys=x;

function sys = mdlOutputs(t,x,u,mf)
tss=0.02/(2*mf);
x(1)=floor(t/(2*tss));
if u(2) >=2*pi
  u(2)=u(2)-2*pi;
else
   u(2)=u(2);
end;

s=floor(u(2)/(pi/3))+1;   %theta to determine the sector
u(2)=u(2)-(s-1)*(pi/3);

% check for over modulation
if u(1)>(((u(3)*(u(4)-1)*cos(pi/6))/(sin(u(2)+pi/3)))-1)
   vi=((u(3)*(u(4)-1)*cos(pi/6))/(sin(u(2)+pi/3))-1);
else
   vi=u(1);
end;

a=floor(vi*cos(u(2)+(pi/6))/(u(3)*cos(pi/6)))+1;  % to determine A
b=floor(vi*cos((pi/6)-u(2))/(u(3)*cos(pi/6)))+1;  % to determine B
h=floor(vi*sin(u(2))/(u(3)*cos(pi/6)))+1;         % to determine H
delta=u(3)^2*cos(pi/6)*(2*a-2*b+2*h-1);
```

Appendix A: Generalized algorithm for multilevel SVM

```
a11=u(3)*cos(pi/6)*(b-h-a);
a12=0.5*u(3)*(-3*a+3*b-3*h+2);
a13=u(3)^2*cos(pi/6)*(a*h+h^2-h+b*a-b^2);

a21=u(3)*cos(pi/6);
a22=-u(3)/2;
a23=-u(3)^2*cos(pi/6)*(b-h);

a31=(a-b+h-1)*u(3)*cos(pi/6);
a32=(3*a-3*b+3*h-1)*0.5*u(3);
a33=u(3)^2*cos(pi/6)*(b^2-a*b-b+2*a-a*h+2*h-1-h^2);

x(3)=tss*(vi*cos(u(2))*a11+vi*sin(u(2))*a12+a13)/delta;
x(4)=tss*(vi*cos(u(2))*a21+vi*sin(u(2))*a22+a23)/delta;
x(5)=tss*(vi*cos(u(2))*a31+vi*sin(u(2))*a32+a33)/delta;

reg=-a+b^2-b+1+h;  % to determine the region number

if s==2 | s==4 | s==6
   are=x(4);
   x(4)=x(5);
   x(5)=are;
else
   x(4)=x(4);
   x(5)=x(5);
end;
x(3)=0.5*x(3);

if x(3)<0.0000001
   x(4)=x(4)-0.0000001+x(3);
   x(5)=x(5)-0.0000001+x(3);
   x(3)=0.0000001;
end;
if x(4)<0.0000001
   x(5)=x(5)-0.0000001+x(4);
   x(4)=0.0000001;
else if x(5)<0.0000001
       x(4)=x(4)-0.0000001+x(5);
       x(5)=0.0000001;
   end;
end;

x(7)=x(3)+2*x(1)*tss;
x(8)=x(4)+x(7);
x(9)=x(5)+x(8);
x(10)=x(3)+x(9);
x(11)=x(3)+x(10);
x(12)=x(11)+x(5);
x(13)=x(12)+x(4);

for k=1:u(4)
   f(1,1,k)=(k-1)*10101;
end;
for n=1:(u(4)-1)
   for j=1:u(4)-n
      for i=1:n
         f(n+1,i,j)=10000*n+100*(i-1)+(j-1)*10101;
      end;
      for i=n+1:2*n
         f(n+1,i,j)=10000*(2*n+1-i)+100*n+(j-1)*10101;
      end;
      for i=2*n+1:3*n
```

```
        f(n+1,i,j)=100*n+(i-2*n-1)+(j-1)*10101;
      end;
      for i=3*n+1:4*n
        f(n+1,i,j)=(4*n+1-i)*100+n+(j-1)*10101;
      end;
      for i=4*n+1:5*n
        f(n+1,i,j)=10000*(i-4*n-1)+n+(j-1)*10101;
      end;
      for i=5*n+1:6*n
        f(n+1,i,j)=10000*n+(6*n+1-i)+(j-1)*10101;
      end;
   end;
end;

if b==1
   b1=1.000000000000001;
else
   b1=b;
end;
        a1=b;
        z2=floor((reg-b*(b-2))/2)+(s-1)*(b-1);
        a2=z2-6*(b-1)*floor((z2-1)/(6*(b1-1)));
        a3=1;     % it can be chosen to be between 1: m-b-1
        a4=b+1-(1-rem(b,2))*rem((s*reg),2)-(1-rem(reg,2))*rem((s*b),2);
        z5=floor((reg+1-b*(b-2))/2)+b*(s-1)+(1-rem(s,2))*[(1-rem(reg,2))*(1-
rem(b,2))+rem(reg,2)*rem(b,2)]-(s-1)*(rem(s*b,2)*(1-rem(reg,2))+rem(s*reg,2)*(1-rem(b,2)));
        a5=z5-6*b*floor((z5-1)/(6*b));

        a6=a3; % it can be chosen to be between 1: m-b-1
        a7=b+1-(1-rem(b,2))*(1-rem(s,2))*rem(reg,2)-(1-rem(reg,2))*(1-rem(s,2))*rem(b,2);
        a8=1+floor((reg-b*(b-2))/2)+(b-1)*(s-1)+(s-1)*rem(s,2)+((1-rem(b,2))*(1-
rem(reg,2))+rem(b,2)*rem(reg,2))*(s-2)*(1-rem(s,2))-6*(b-1)*floor(reg/(b1^2-
1))*floor(s/6)*[rem(reg,2)*(1-rem(b,2))+rem(b,2)*(1-rem(reg,2))];
        a9=a3+(1-rem(b,2))*(1-rem(s,2))*rem(reg,2)+(1-rem(reg,2))*(1-rem(s,2))*rem(b,2);  % it can be
chosen to be between 1: m-b-1
        a10=a1;
        a11=a2;
        a12=a3+1;    % it can be chosen to be between 1: m-b-1

r1=floor(f(a1,a2,a3)/10000);
r2=floor((f(a1,a2,a3)-10000*r1)/100);
r3=f(a1,a2,a3)-10000*r1-100*r2;
r4=floor(f(a4,a5,a6)/10000);
r5=floor((f(a4,a5,a6)-10000*r4)/100);
r6=f(a4,a5,a6)-10000*r4-100*r5;
r7=floor(f(a7,a8,a9)/10000);
r8=floor((f(a7,a8,a9)-10000*r7)/100);
r9=f(a7,a8,a9)-10000*r7-100*r8;
r10=floor(f(a10,a11,a12)/10000);
r11=floor((f(a10,a11,a12)-10000*r10)/100);
r12=f(a10,a11,a12)-10000*r10-100*r11;

s0=[r1 r2 r3];
s1=[r4 r5 r6];
s2=[r7 r8 r9];
s7=[r10 r11 r12];

if t>=x(7) & t< x(8)
   sout=s1;
else if t>=x(8) & t< x(9)
      sout=s2;
   else if t>=x(9) & t< x(10)
```

```
    sout=s7;
elseif t>= x(10) & t< x(11)
      sout=s7;
   elseif t>= x(11) & t< x(12)
         sout=s2;
      elseif t>=x(12)&t<x(13)
            sout=s1;
         else
            sout=s0;
         end;
      end;
   end;
end;
   end;
end;

%e1(i)=(1/3)*[2*s(i,1)-s(i,2)-s(i,3)];
%  e2(i)=(1/3)*[2*s(i,2)-s(i,1)-s(i,3)];
x(14) = sout(1);
x(15) =sout(2);
x(16) =sout(3);
%e12=e11-e22;
%e55=e11-0.5*e22(i)-0.5*e33(i);
%e66=0.5*(3^0.5)*[e22(i)-e33(i)];
sys=x;
sys= [x(14) x(15) x(16)];
%sys= [(1/3)*(2*x(14)-x(15)-x(16)) (1/3)*(2*x(15)-x(14)-x(16)) (1/3)*(2*x(16)-x(14)-x(15))];

function sys=mdlGetTimeOfNextVarHit(t,x,u,mf,tss)

tss=0.02/(2*mf);
x(1)=floor(t/(2*tss));
if u(2) >=2*pi
  u(2)=u(2)-2*pi;
else
   u(2)=u(2);
end;
s=floor(u(2)/(pi/3))+1;   %theta to determine the sector
u(2)=u(2)-(s-1)*(pi/3);

% check for over modulation
if u(1)>(((u(3)*(u(4)-1)*cos(pi/6))/(sin(u(2)+pi/3)))-1)
    vi=((u(3)*(u(4)-1)*cos(pi/6))/(sin(u(2)+pi/3))-1);
else
    vi=u(1);
end;

a=floor(vi*cos(u(2)+(pi/6))/(u(3)*cos(pi/6)))+1;  % to determine A
b=floor(vi*cos((pi/6)-u(2))/(u(3)*cos(pi/6)))+1;  % to determine B
h=floor(vi*sin(u(2))/(u(3)*cos(pi/6)))+1;         % to determine H

delta=u(3)^2*cos(pi/6)*(2*a-2*b+2*h-1);
a11=u(3)*cos(pi/6)*(b-h-a);
a12=0.5*u(3)*(-3*a+3*b-3*h+2);
a13=u(3)^2*cos(pi/6)*(a*h+h^2-h+b*a-b^2);
a21=u(3)*cos(pi/6);
a22=-u(3)/2;
a23=-u(3)^2*cos(pi/6)*(b-h);
a31=(a-b+h-1)*u(3)*cos(pi/6);
a32=(3*a-3*b+3*h-1)*0.5*u(3);
a33=u(3)^2*cos(pi/6)*(b^2-a*b-b+2*a-a*h+2*h-1-h^2);
```

```
x(3)=tss*(vi*cos(u(2))*a11+vi*sin(u(2))*a12+a13)/delta;
x(4)=tss*(vi*cos(u(2))*a21+vi*sin(u(2))*a22+a23)/delta;
x(5)=tss*(vi*cos(u(2))*a31+vi*sin(u(2))*a32+a33)/delta;

reg=-a+b^2-b+1+h;  % to determine the region number

if s==2 | s==4 | s==6
   are=x(4);
   x(4)=x(5);
   x(5)=are;
else
   x(4)=x(4);
   x(5)=x(5);
end;

x(3)=0.5*x(3);
if x(3)<0.0000001
   x(4)=x(4)-0.0000001+x(3);
   x(5)=x(5)-0.0000001+x(3);
   x(3)=0.0000001;
end;
if x(4)<0.0000001
   x(5)=x(5)-0.0000001+x(4);
   x(4)=0.0000001;
else if x(5)<0.0000001
       x(4)=x(4)-0.0000001+x(5);
       x(5)=0.0000001;
   end;
end;

x(7)=x(3)+2*x(1)*tss;
x(8)=x(4)+x(7);
x(9)=x(5)+x(8);
x(10)=x(3)+x(9);
x(11)=x(3)+x(10);
x(12)=x(11)+x(5);
x(13)=x(12)+x(4);

if t>=x(7) & t< x(8)
   nextt=t+x(4);
else if t>=x(8)& t<x(9)
       nextt=t+x(5);
   else if t>=x(9)& t<x(10)
          nextt=t+x(3);
       else if t>=x(10) & t< x(11)
              nextt=t+x(3);
          else if t>=x(11) & t<x(12)
                 nextt=t+x(5);
              else if t>=x(12) & t<x(13)
                     nextt=t+x(4);
                 else
                     nextt=t+x(3);
                 end;
              end;
          end;
       end;
   end;
end;

sys=nextt;
```

Appendix B

C code for the generalized algorithm of SVM

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "math.h"
#include "mathf.h"
#include "intr.h"
#include "FPGA_CONTROL_5level.h"
#include "AED_new.h"

unsigned short int state[6][25][6],state0,state1,state2,state7;
unsigned short int y,s,ss00,time0,time1,time2,time00,time11,time22;
unsigned int total_1,total_2,total_3;
unsigned short int sa_0,sb_0,sc_0,s0,sa_1,sb_1,sc_1,s1,sa_2,sb_2,sc_2,s2,sa_7,sb_7,sc_7,s7;
unsigned int x,reg,a,b,h,total,a0,a1,a2,a3,a4,a5,a6,a7,a8,a9,a10,a11,a12;
unsigned int even_b,odd_b,even_reg,odd_reg,odd_s_reg,odd_s_b,odd_s,even_s;
unsigned int w00,w0,w1,w2,w3,w4,w5,w6,w7,w8,w9,w10,w11,choose_redundant=1,k,j,n,i;
float ma,m,t1,t2,t0,theta=0,theta1,samp=0.00016384;
float E=100,input_voltage,v_input_new,ma_3level,xx,max_input_voltage;
float rrr1,rrr2,rrr3,rrr4,rrr6,rrr7,rrr8;
int rr1,rr2,rr3,rr4,rr6,rr7,rr8,count_loop=0,count_intr=0;

interrupt void ahmed();

void main()
{
/*************************************************************************/
/* Initialize                                                            */
/*************************************************************************/
 board_init();

                emif_init(0x00003078,
                          0x00000040,
                          0x40FD0220,
                          0x00000030,
                          0x00000030,
                          0x07229000,
                          0x00000619);

          SET_BIT(0X01780000,5);
          delay_msec(1);
          RESET_BIT(0X01780000,5);
          printf("enter the ref voltage\n\n");
          scanf("%f",&input_voltage);

          m=5;

          /*generation of the states*/
          for(k=1;k<=m;++k)
          { state[1][1][k]=(k-1)*111;}

          for(n=1;n<=(m-1);++n)      /* hexagon number*/
          {
                for(j=1;j<=(m-n);++j)       /* order of redundant state*/
                {
```

```
                for(i=1;i<=n;++i)
                {state[n+1][i][j]=100*n+10*(i-1)+(j-1)*111;}
                for(i=n+1;i<=2*n;++i)
                {state[n+1][i][j]=100*(2*n+1-i)+10*n+(j-1)*111;}
                for(i=2*n+1;i<=3*n;++i)
                {state[n+1][i][j]=10*n+(i-2*n-1)+(j-1)*111;}
                for(i=3*n+1;i<=4*n;++i)
                {state[n+1][i][j]=10*(4*n+1-i)+n+(j-1)*111;}
                for(i=4*n+1;i<=5*n;++i)
                {state[n+1][i][j]=100*(i-4*n-1)+n+(j-1)*111;}
                for(i=5*n+1;i<=6*n;++i)
                {state[n+1][i][j]=100*n+(6*n+1-i)+(j-1)*111;}
        }

        }

        WRITE1_DAUGHTER=0X01C29030;
        WRITE2_DAUGHTER=0X00000000;
        WRITE3_DAUGHTER=0X00000000;/* 1C29030;*/

       intr_map(CPU_INT7,ISN_EXT_INT7);
       INTR_ENABLE(CPU_INT_NMI);
       INTR_ENABLE(CPU_INT7);

       SET_BIT(0X01780000,6);
       intr_hook(ahmed,CPU_INT7);
/*=============================================================================*/
/*=============================================================================*/
       while (1)
       {
                /* chech if the angle > 2*pi to reduce it by an offest of 2*pi */
                    if (theta>6.28318)
                    {theta-=6.28318;}

                    /* check in wchich sector lies the vector */
                    ss00=(int)(0.955*theta);
                    s=ss00+1;

                    /* scale theta according to the scetor where the vector lies*/
                    theta1=theta-(1.0472)*ss00;

/*=============================================================================*/

                /* check over modulation*/
                    max_input_voltage=(346.4/sinf(theta1+1.0472))-1;
                    if (input_voltage>max_input_voltage)
                    {v_input_new=max_input_voltage;}
                    else
                    {v_input_new=input_voltage;}

/* modulation index*/
/*ma=vm/(E*(m-1)*0.866);*/
                ma=v_input_new/(346.4);
                 ma_3level=4*ma;

                 a=(int)(ma_3level*cosf(theta1+0.5236))+1;
                 b=(int)(ma_3level*cosf(0.5236-theta1))+1;
                 h=(int)(ma_3level*sinf(theta1))+1;
                 x=a-b+h;

                xx=(97656.25*x-48828.125)/4;
                rr1=2*(x-a);
                rrr1=rr1;
```

```
   rr2=2*(-x*(h+b-2)+b-1);
rrr2=rr2;
t1=(6.928*ma*cosf(theta1)-4*ma*sinf(theta1)+rrr1)/(xx);

rr3=x-1;
rrr3=rr3;
rr4=3*x-1;
rrr4=rr4;
t2=(6.928*ma*rrr3*cosf(theta1)+4*ma*rrr4*sinf(theta1)+rrr2)/(xx);

  t0=0.5*(samp-t1-t2);

time0=(int)(1562500*t0);          /*(int)(256*t0/samp);*/
time1=(int)(1562500*t1);          /*(int)(256*t1/samp);*/
time2=(int)(1562500*t2);          /*(int)(256*t2/samp);*/

if (s==2||s==4||s==6)
{
y=time1;
time1=time2;
time2=y;
}

if (time0<5)
{time1=time1-5+time0;
time2=time2-5+time0;
time0=5;
}
if (time1<5)
{time2=time2-5+time1;
time1=5;
}
if (time2<5)
{time1=time1-5+time2;
time2=5;
}

time00=time0;
time11=time0+time1;
time22=time0+time1+time2;

reg=-a+b*b-b+1+h;

/*==========================================================*/
/* the sequence of the states*/
/*__________________________________________________________*/
 a1=b;
/*__________________________________________________________*/
 w0=(reg-b*(b-2));
 w00=(s-1)*(b-1);
 w1=(int)(w0/2)+w00;
 if (b!=1)
 {a2=w1-6*(b-1)*(int)((w1-1)/(6*(b-1)));}
 else
 {a2=w1;}
/*__________________________________________________________*/
 odd_b=b%2;
 even_b=1-odd_b;
 odd_reg=reg%2;
 even_reg=1-odd_reg;
 odd_s=s%2;
 even_s=1-odd_s;
```

```
odd_s_reg=(s*reg)%2;
odd_s_b=(s*b)%2;
a3=choose_redundant;
/*_____________________________________________________*/
w2=even_b*odd_s_reg;
w3=even_reg*odd_s_b;
a4=b+1-w2-w3;
/*_____________________________________________________*/
w4=odd_reg*odd_b;
w5=even_reg*even_b;
w6=(int)((1+w0)/2);
w7=w6+b*(s-1)+even_s*(w4+w5)-(s-1)*(w2+w3);
a5=w7-6*b*(int)((w7-1)/(6*b));
/*_____________________________________________________*/
a6=a3;
/*_____________________________________________________*/
w8=even_b*odd_reg;
w9=even_reg*odd_b;
a7=b+1-even_s*(w8+w9);
/*_____________________________________________________*/
w10=(s-2)*even_s*(w4+w5);
if (b==1)
{w11=0;}
else
{w11=6*(b-1)*(int)(reg/(b*b-1))*(int)(s/6)*(w8+w9);}
a8=1+(int)(w0/2)+w00+(s-1)*odd_s+w10-w11;
/*_____________________________________________________*/
a9=choose_redundant+even_s*(w8+w9);
/*_____________________________________________________*/
a10=b;
/*_____________________________________________________*/
a11=a2;
/*_____________________________________________________*/
a12=choose_redundant+1;
/*_____________________________________________________*/

state0=state[a1][a2][a3];
state1=state[a4][a5][a6];
state2=state[a7][a8][a9];
state7=state[a10][a11][a12];

sa_0=state0/100;
s0=state0%100;
sb_0=s0/10;
sc_0=s0%10;

sa_1=state1/100;
s1=state1%100;
sb_1=s1/10;
sc_1=s1%10;

sa_2=state2/100;
s2=state2%100;
sb_2=s2/10;
sc_2=s2%10;

sa_7=state7/100;
s7=state7%100;
sb_7=s7/10;
sc_7=s7%10;

        LOAD_FIELD(&total_1,time00,0,8);
```

```
                LOAD_FIELD(&total_1,time11,8,8);
                LOAD_FIELD(&total_1,time22,16,8);
                LOAD_FIELD(&total_2,sc_0/*phase_c_t0*/,0,3);
                LOAD_FIELD(&total_2,sb_0/*phase_b_t0*/,3,3);
                LOAD_FIELD(&total_2,sa_0/*phase_a_t0*/,6,3);

                LOAD_FIELD(&total_2,sc_1/*phase_c_t0*/,9,3);
                LOAD_FIELD(&total_2,sb_1/*phase_b_t0*/,12,3);
                LOAD_FIELD(&total_2,sa_1/*phase_a_t0*/,15,3);

                LOAD_FIELD(&total_3,sc_2/*phase_c_t0*/,0,3);
                LOAD_FIELD(&total_3,sb_2/*phase_b_t0*/,3,3);
                LOAD_FIELD(&total_3,sa_2/*phase_a_t0*/,6,3);
                                LOAD_FIELD(&total_3,sc_7/*phase_c_t0*/,9,3);
                                LOAD_FIELD(&total_3,sb_7/*phase_b_t0*/,12,3);
                                LOAD_FIELD(&total_3,sa_7/*phase_a_t0*/,15,3);
                                while (count_intr!=count_loop)
                                { }
                                ++count_loop;
        }

}

        interrupt void ahmed(void)
                {
                        WRITE1_DAUGHTER=total_1;
                        WRITE2_DAUGHTER=total_2;
                        WRITE3_DAUGHTER=total_3;
                        theta+=0.102943708086272;/*2*pi*samp*50;        */
                        ++count_intr;
                }
```

Appendix C

C code for the new SVM techniques

C.1 PS-SVM

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "emif.h"
#include "AED_new.h"
#include "dma.h"
#include "math.h"
#include "intr.h"
#include "FPGA_CONTROL.h"

unsigned short int y,s,ss00,time0,time1,time2,time00,time11,time22;
float m,t1,t2,t0,theta=0,theta1,samp=0.00016384/*samp=0.00004096*/;
float t00,t11,t22;
unsigned int total;
int count_intr=0,count_loop=0;

interrupt void ahmed();

void main()
{
/*************************************************************/
/* Initialize                                                */
/*************************************************************/
        board_init();
        emif_init(0x00003078,
                  0x00000040,
                  0x40FD0220,
                  0x00000030,
                  0x00000030,
                  0x07229000,
                  0x00000619);

SET_BIT(0X01780000,5);
delay_msec(1);
RESET_BIT(0X01780000,5);

printf("enter the modulation index please\n\n");
scanf("%f",&m);

WRITE1_DAUGHTER=0X01C29030;
 SET_BIT(0X01780000,6);
 intr_map(CPU_INT7,ISN_EXT_INT7);
 INTR_ENABLE(CPU_INT_NMI);
 INTR_ENABLE(CPU_INT7);
 intr_hook(ahmed,CPU_INT7);

while(1)
{
                if (theta>6.28318)
                {theta-=6.28318;}

                /* check in wchich sector lies the vector */
                 ss00=(int)(0.955*theta);
```

```
s=ss00+1;

/* scale theta according to the scetor where the vector lies*/
theta1=theta-(1.0472)*ss00;

/*calculation of the time distribution between the states*/
t1=m*samp*sinf(1.0472-theta1);
t2=m*samp*sinf(theta1);
t0=0.5*(samp-t1-t2);

/* check over modulation */
if (t0<0)
{
        t00=0;
        t11=samp*t1/(t1+t2);
        t22=samp*t2/(t1+t2);
}
else
{
        t00=t0;
        t11=t1;
        t22=t2;
}

/* convert t00,t11,t22 to the number of counts required in fpga*/

time0=(int)(1562500*t00);
time1=(int)(1562500*t11);
time2=(int)(1562500*t22);

if (s==2||s==4||s==6)
{
y=time1;
time1=time2;
time2=y;
}

if (time0<4)
{time0=4;
time1=time1-4;
time2=time2-4;
}
if (time1<4)
{time1=4;
time2=time2-4;
time0=time0;
}
if (time2<4)
{
time2=4;
time1=time1-4;
time0=time0;
}

time00=time0;
time11=time0+time1;
time22=time0+time1+time2;

LOAD_FIELD(&total,time00,0,8);
LOAD_FIELD(&total,time11,8,8);
LOAD_FIELD(&total,time22,16,8);
LOAD_FIELD(&total,s,24,3);
```

```
                        ++count_loop;
                        }
}

        interrupt void ahmed(void)
                {
                        WRITE1_DAUGHTER=total;
                        theta+=0.102943708086272;/*2*pi*samp*50;        */
                  ++count_intr;
                }
```

C.2 MPS-SVM

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "math.h"
#include "intr.h"
#include "FPGA_CONTROL.h"

unsigned short int difference,s,ss00,time0_a,time1_a,time2_a,time00_a,time11_a,time22_a;
unsigned short int time00_aa,time11_aa,time22_aa,time00_aaa,time11_aaa,time22_aaa;
unsigned short int time00_aaaa,time11_aaaa,time22_aaaa,time0_3rd,time0_4th;
unsigned short int time22_a,time33_a,time44_a,time55_a;
unsigned short int time22_aa,time33_aa,time44_aa,time55_aa;
unsigned short int time22_aaa,time33_aaa,time44_aaa,time55_aaa;
unsigned short int time22_aaaa,time33_aaaa,time44_aaaa,time55_aaaa;
unsigned short int a0=0,a1=1,a2=2,a3=3;
unsigned short int b0,b1,b2,b3,b4,b5,b6;
unsigned short int c0,c1,c2,c3,c4,c5,c6;
float y,ma,t1,t2,t0,theta=0,theta1,samp=0.00016384/*samp=0.00004096*/;
float input_voltage,max_input_voltage,v_input_new,t_start_3rd,t_start_4th;
unsigned int total_1,total_2,total_3,total_4;
unsigned int total_5,total_6,total_7,total_8;
int count_intr=0,count_loop=0;

interrupt void ahmed();

void main()
{
/*****************************************************************/
/* Initialize                                                    */
/*****************************************************************/
 board_init();
                emif_init(0x00003078,
                0x00000040,
                0x40FD0220,
                0x00000030,
                0x00000030,
                0x07229000,
                0x00000619);

 SET_BIT(0X01780000,5);
 delay_msec(1);
 RESET_BIT(0X01780000,5);

 printf("enter the voltage  the cell voltage is 100 V \n\n");
scanf("%f",&input_voltage);
```

```
WRITE1_DAUGHTER=0X01C29030;
WRITE2_DAUGHTER=0X01C29030;
WRITE3_DAUGHTER=0X01C29030;
WRITE4_DAUGHTER=0X01C29030;
WRITE5_DAUGHTER=0X01C29030;
WRITE6_DAUGHTER=0X01C29030;
WRITE7_DAUGHTER=0X01C29030;
WRITE8_DAUGHTER=0X01C29030;

SET_BIT(0X01780000,6);
intr_map(CPU_INT7,ISN_EXT_INT7);
INTR_ENABLE(CPU_INT_NMI);
INTR_ENABLE(CPU_INT7);

intr_hook(ahmed,CPU_INT7);

while(1)
{
                if (theta>6.28318)
                {
                        theta-=6.28318;
                }
                ss00=(int)(0.955*theta);
                s=ss00+1;
                theta1=theta-(1.0472)*ss00;

                max_input_voltage=(346.4/sinf(theta1+1.0472))-1;
                if (input_voltage>max_input_voltage)
                {v_input_new=max_input_voltage;}
                else
                {v_input_new=input_voltage;}

                /* modulation index*/
                /*ma=vm/(E*(m-1)*0.866);*/
                 ma=v_input_new/(346.4);

                /*calculation of the time distribution between the states*/
                t1=ma*samp*sinf(1.0472-theta1);
                t2=ma*samp*sinf(theta1);
                t0=0.5*(samp-t1-t2);

                if (s==2||s==4||s==6)
                {
                y=t1;
                t1=t2;
                t2=y;
                }
                /* convert t00,t11,t22 to the number of counts required in fpga*/
                 time1_a=(int)(781250*t1);  /* time1=(int)(128*t11/samp);*/
                time2_a=(int)(781250*t2);  /* time2=(int)(128*t22/samp);*/
                difference=128-time1_a-time2_a;
                time0_a=(int)(difference/2);

/*=============================================================*/
/*                          third group                        */
/*=============================================================*/
if (t0+t2<0.5*samp)
                {
                t_start_3rd=0.5*samp-t0;
                time0_3rd=(int)(781250*t_start_3rd);  /* time2=(int)(128*t22/samp);*/
```

```
time00_aaa=time0_3rd;
time11_aaa=time0_3rd+2*time0_a;
time22_aaa=time11_aaa+time1_a;
time33_aaa=time22_aaa+time2_a;
time44_aaa=time33_aaa+2*time0_a;
time55_aaa=time44_aaa+time2_a;

b0=1;
b1=0;
b2=1;
b3=2;
b4=3;
b5=2;
b6=1;
}
else
{
t_start_3rd=0.5*samp-t0-t1;
time0_3rd=(int)(781250*t_start_3rd);  /* time2=(int)(128*t22/samp);*/

time00_aaa=time0_3rd;
time11_aaa=time0_3rd+time1_a;
time22_aaa=time11_aaa+2*time0_a;
time33_aaa=time22_aaa+time1_a;
time44_aaa=time33_aaa+time2_a;
time55_aaa=time44_aaa+2*time0_a;

b0=2;
b1=1;
b2=0;
b3=1;
b4=2;
b5=3;
b6=2;
}


 /*=========================================================*/
 /*                      fourth group                       */
/*=========================================================*/
if (t0+t2<0.5*samp)
                {
                t_start_4th=0.5*samp-t0-t2;
                time0_4th=(int)(781250*t_start_4th);  /* time2=(int)(128*t22/samp);*/

                time00_aaaa=time0_4th;
                time11_aaaa=time0_4th+time2_a;
                time22_aaaa=time11_aaaa+2*time0_a;
                time33_aaaa=time22_aaaa+time2_a;
                time44_aaaa=time33_aaaa+time1_a;
                time55_aaaa=time44_aaaa+2*time0_a;

                c0=1;
                c1=2;
                c2=3;
                c3=2;
                c4=1;
                c5=0;
                c6=1;
                }
else
```

```
{
t_start_4th=0.5*samp-t0;
time0_4th=(int)(781250*t_start_4th);  /* time2=(int)(128*t22/samp);*/

time00_aaaa=time0_4th;
time11_aaaa=time0_4th+2*time0_a;
time22_aaaa=time11_aaaa+time2_a;
time33_aaaa=time22_aaaa+time1_a;
time44_aaaa=time33_aaaa+time0_a;
time55_aaaa=time44_aaaa+time1_a;

c0=2;
c1=3;
c2=2;
c3=1;
c4=0;
c5=1;
c6=2;
}

 /*=================================================*/
 /*                  first group                    */
/*=================================================*/
time00_a=time0_a;
                time11_a=time0_a+time1_a;
                time22_a=time11_a+time2_a;
                time33_a=time22_a+2*time0_a;
                time44_a=time33_a+time2_a;
                time55_a=time44_a+time1_a;

 /*=================================================*/
 /*                  second group                   */
/*=================================================*/
time00_aa=time0_a;
                time11_aa=time0_a+time2_a;
                time22_aa=time11_aa+time1_a;
                time33_aa=time22_aa+2*time0_a;
                time44_aa=time33_aa+time1_a;
                time55_aa=time44_aa+time2_a;

                LOAD_FIELD(&total_1,time00_a,0,8);
                LOAD_FIELD(&total_1,time11_a,8,8);
                LOAD_FIELD(&total_1,time22_a,16,8);
                LOAD_FIELD(&total_1,time33_a,24,8);
                LOAD_FIELD(&total_2,time44_a,0,8);
                LOAD_FIELD(&total_2,time55_a,8,8);
                LOAD_FIELD(&total_2,s,16,3);
                LOAD_FIELD(&total_2,a0,19,2);
                LOAD_FIELD(&total_2,a1,21,2);
                LOAD_FIELD(&total_2,a2,23,2);
                LOAD_FIELD(&total_2,a3,25,2);
                LOAD_FIELD(&total_2,a2,27,2);
                LOAD_FIELD(&total_2,a1,29,2);
                LOAD_FIELD(&total_4,a0,30,2);
                LOAD_FIELD(&total_3,time00_aa,0,8);
                LOAD_FIELD(&total_3,time11_aa,8,8);
                LOAD_FIELD(&total_3,time22_aa,16,8);
                LOAD_FIELD(&total_3,time33_aa,24,8);
                LOAD_FIELD(&total_4,time44_aa,0,8);
                LOAD_FIELD(&total_4,time55_aa,8,8);
                LOAD_FIELD(&total_4,a3,16,2);
                LOAD_FIELD(&total_4,a2,18,2);
```

```
LOAD_FIELD(&total_4,a1,20,2);
LOAD_FIELD(&total_4,a0,22,2);
LOAD_FIELD(&total_4,a1,24,2);
LOAD_FIELD(&total_4,a2,26,2);
LOAD_FIELD(&total_4,a3,28,2);
LOAD_FIELD(&total_5,time00_aaa,0,8);
LOAD_FIELD(&total_5,time11_aaa,8,8);
LOAD_FIELD(&total_5,time22_aaa,16,8);
LOAD_FIELD(&total_5,time33_aaa,24,8);
LOAD_FIELD(&total_6,time44_aaa,0,8);
LOAD_FIELD(&total_6,time55_aaa,8,8);
LOAD_FIELD(&total_6,b0,16,2);
LOAD_FIELD(&total_6,b1,18,2);
LOAD_FIELD(&total_6,b2,20,2);
LOAD_FIELD(&total_6,b3,22,2);
LOAD_FIELD(&total_6,b4,24,2);
LOAD_FIELD(&total_6,b5,26,2);
LOAD_FIELD(&total_6,b6,28,2);
LOAD_FIELD(&total_7,time00_aaaa,0,8);
LOAD_FIELD(&total_7,time11_aaaa,8,8);
LOAD_FIELD(&total_7,time22_aaaa,16,8);
LOAD_FIELD(&total_7,time33_aaaa,24,8);
LOAD_FIELD(&total_8,time44_aaaa,0,8);
LOAD_FIELD(&total_8,time55_aaaa,8,8);
LOAD_FIELD(&total_8,c0,16,2);
LOAD_FIELD(&total_8,c1,18,2);
LOAD_FIELD(&total_8,c2,20,2);
LOAD_FIELD(&total_8,c3,22,2);
LOAD_FIELD(&total_8,c4,24,2);
LOAD_FIELD(&total_8,c5,26,2);
LOAD_FIELD(&total_8,c6,28,2);
                ++count_loop;
                while (count_intr<count_loop)
                { }
                }
        }

interrupt void ahmed(void)
        {
                WRITE1_DAUGHTER=total_1;
                WRITE2_DAUGHTER=total_2;
                WRITE3_DAUGHTER=total_3;
                WRITE4_DAUGHTER=total_4;
                WRITE5_DAUGHTER=total_5;
                WRITE6_DAUGHTER=total_6;
                WRITE7_DAUGHTER=total_7;
                WRITE8_DAUGHTER=total_8;
                theta+=0.102943708086272;/*2*pi*samp*50;        */
          ++count_intr;
}
```

C.3 H-SVM

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "math.h"
#include "intr.h"
#include "FPGA_3level.h"
#include "mathf.h"

unsigned short int y,s,ss00,time00,time11,time22,time0,time1,time2;
unsigned int sa_0,total_1,total_2,ADC[8];
int trial,count_loop=0,count_intr=0;
float ma,t1,t2,t0,theta=0,theta1,samp=0.00016384;
float ma_3level,max_input_voltage;
float input_voltage,v_input_new;
float ma_samp;
unsigned int reg,a,b,h;

interrupt void ahmed();

void main()

{
/*************************************************************************/
/* Initialize                                                            */
/*************************************************************************/
        board_init();
            emif_init(0x00003078,
                      0x00000040,
                      0x40FD0220,
                      0x00000030,
                      0x00000030,
                      0x07229000,
                      0x00000619);

              SET_BIT(0X01780000,5);
              delay_msec(1);
              RESET_BIT(0X01780000,5);

printf("enter voltage reference value \n\n");
scanf("%f",&input_voltage);

WRITE1_DAUGHTER=0X01C29030;
WRITE2_DAUGHTER=0X00000000;/* 1C29030;*/
intr_map(CPU_INT7,ISN_EXT_INT7);
INTR_ENABLE(CPU_INT_NMI);
INTR_ENABLE(CPU_INT7);
SET_BIT(0X01780000,6);
                intr_hook(ahmed,CPU_INT7);

/*=======================================================================*/
/*=======================================================================*/
        while (1)
        {
                if (theta>6.28318)
                  {theta-=6.28318;}
        /*=======================================================*/
                        ss00=(int)(0.955*theta);
                        s=ss00+1;
                        theta1=theta-(1.0472)*ss00;
          /*=============================================*/
```

```
/* check over modulation*/
        max_input_voltage=(173.2/sinf(theta1+1.0472))-1;
        if (input_voltage>max_input_voltage)
        {v_input_new=max_input_voltage;}
        else
        {v_input_new=input_voltage;}

/* modulation index*/
/*ma=vm/(E*(m-1)*0.866);*/
   ma=v_input_new/(173.2);
   ma_3level=2*ma;
   a=(int)(ma_3level*cosf(theta1+0.5236))+1;
   b=(int)(ma_3level*cosf(0.5236-theta1))+1;
   h=(int)(ma_3level*sinf(theta1))+1;
   reg=-a+b*b-b+1+h;

        ma_samp=ma_3level*samp;
        if (reg==1)
        {t1=ma_samp*sinf(1.0472-theta1);
         t2=ma_samp*sinf(theta1);}
         else if (reg==2)
         {t1=ma_samp*sinf(1.0472-theta1)-samp;
         t2=ma_samp*sinf(theta1);}
         else if (reg==3)
         {t1=samp-ma_samp*sinf(1.0472-theta1);
         t2=ma_samp*sinf(theta1+1.0472)-samp;}
         else
         {t1=ma_samp*sinf(1.0472-theta1);
         t2=ma_samp*sinf(theta1)-samp;}

         t0=0.5*(samp-t1-t2);
                time0=(int)(1562500*t0);        /*(int)(256*t0/samp);*/
                time1=(int)(1562500*t1);        /*(int)(256*t1/samp);*/
                time2=(int)(1562500*t2);        /*(int)(256*t2/samp);*/

                if (s==2||s==4||s==6)
                {
                y=time1;
                time1=time2;
                time2=y;
                }

                time00=time0;
                time11=time0+time1;
                time22=time0+time1+time2;

if (s==1)
{
        if (reg==1)
        {sa_0=5587968;}
        else if (reg==2)
        {sa_0=9848848;}
        else if (reg==3)
        {sa_0=9848080;}
        else
        {sa_0=10914068;}
}
/*=====================================*/
else if (s==2)
{
        if (reg==1)
```

```
                {sa_0=5587200;}
                else if (reg==2)
                {sa_0=10913300;}
                else if (reg==3)
                {sa_0=10851860;}
                else
                {sa_0=6652420;}
}

/*==================================*/
else if (s==3)
{
                if (reg==1)
                {sa_0=5525760;}
                else if (reg==2)
                {sa_0=6590980;}
                else if (reg==3)
                {sa_0=6590788;}
                else
                {sa_0=6857285;}
}

/*==================================*/

else if (s==4)
{
                if (reg==1)
                {sa_0=5525568;}
                else if (reg==2)
                {sa_0=6857093;}
                else if (reg==3)
                {sa_0=6906245;}
                else
                {sa_0=5841025;}
}

/*==================================*/

else if (s==5)
{
                if (reg==1)
                {sa_0=5574720;}
                else if (reg==2)
                {sa_0=5841025;}
                else if (reg==3)
                {sa_0=5841985;}
                else
                {sa_0=10101905;}
}

/*==================================*/
else
{
                if (reg==1)
                {sa_0=5575680;}
                else if (reg==2)
                {sa_0=10102865;}
                else if (reg==3)
                {sa_0=10115153;}
                else
                {sa_0=9836560;}
}
```

```
                        LOAD_FIELD(&total_1,time00,0,8);
                        LOAD_FIELD(&total_1,time11,8,8);
                        LOAD_FIELD(&total_1,time22,16,8);
                        LOAD_FIELD(&total_2,sa_0,0,24);
                        ++count_loop;
                        }
}

interrupt void ahmed(void)
        {
                        WRITE1_DAUGHTER=total_1;
                        WRITE2_DAUGHTER=total_2;
                        theta+=0.10294362112;/*2*pi*samp*50;     */
                        ++count_intr;
        }
```

C.4 MH-SVM

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "math.h"
#include "intr.h"
#include "FPGA_3level.h"
#include "mathf.h"

unsigned short int y,s,ss00,time00,time11,time22,time000,time111,time222,time0,time1,time2;
unsigned int sa_0,total_1,total_2,total_3,ADC[8];
int trial,count_loop=0,count_intr=0;
float ma,t1,t2,t0,theta=0,theta1,samp=0.00016384;
float ma_3level,max_input_voltage;
float input_voltage,v_input_new;
float ma_samp;
unsigned int reg,a,b,h;

interrupt void ahmed();

void main()
{
/*****************************************************************************/
/* Initialize                                                                */
/*****************************************************************************/
        board_init();
            emif_init(0x00003078,
                                                0x00000040,
                                                0x40FD0220,
                                                0x00000030,
                                                0x00000030,
                                                0x07229000,
                                                0x00000619);

                SET_BIT(0X01780000,5);
                delay_msec(1);
                RESET_BIT(0X01780000,5);

        printf("enter voltage reference value \n\n");
scanf("%f",&input_voltage);

        WRITE1_DAUGHTER=0X01C29030;
            WRITE2_DAUGHTER=0X00000000;/* 1C29030;*/
        intr_map(CPU_INT7,ISN_EXT_INT7);
```

```
                        INTR_ENABLE(CPU_INT_NMI);
                        INTR_ENABLE(CPU_INT7);
                        SET_BIT(0X01780000,6);
                                intr_hook(ahmed,CPU_INT7);
/*==========================================================================
====*/
/*==========================================================================
====*/
        while (1)
        {
                        if (theta>6.28318)
                                {theta-=6.28318;}

        /*=============================================================*/
                                ss00=(int)(0.955*theta);
                                s=ss00+1;
                                theta1=theta-(1.0472)*ss00;


/*=================================================================*/
                        /* check over modulation*/
                                max_input_voltage=(173.2/sinf(theta1+1.0472))-1;
                                if (input_voltage>max_input_voltage)
                                {v_input_new=max_input_voltage;}
                                else
                                {v_input_new=input_voltage;}

        /* modulation index*/
        /*ma=vm/(E*(m-1)*0.866);*/
        ma=v_input_new/(173.2);
                ma_3level=2*ma;

a=(int)(ma_3level*cosf(theta1+0.5236))+1;
                b=(int)(ma_3level*cosf(0.5236-theta1))+1;
                h=(int)(ma_3level*sinf(theta1))+1;

                reg=-a+b*b-b+1+h;
                        ma_samp=ma_3level*samp;

                        if (reg==1)
                        {t1=ma_samp*sinf(1.0472-theta1);
                         t2=ma_samp*sinf(theta1);}
                         else if (reg==2)
                         {t1=ma_samp*sinf(1.0472-theta1)-samp;
                         t2=ma_samp*sinf(theta1);}
                         else if (reg==3)
                         {t1=samp-ma_samp*sinf(1.0472-theta1);
                         t2=ma_samp*sinf(theta1+1.0472)-samp;}
                         else
                         {t1=ma_samp*sinf(1.0472-theta1);
                         t2=ma_samp*sinf(theta1)-samp;}

                         t0=0.5*(samp-t1-t2);

                        time0=(int)(1562500*t0);        /*(int)(256*t0/samp);*/
                        time1=(int)(1562500*t1);        /*(int)(256*t1/samp);*/
                        time2=(int)(1562500*t2);        /*(int)(256*t2/samp);*/

                        if (s==2||s==4||s==6)
                        {
                        y=time1;
```

```
                                time1=time2;
                                time2=y;
                                }

                                time00=time0;
                                time11=time0+time1;
                                time22=time0+time1+time2;
                                time000=time0;
                                time111=time0+time2;
                                time222=time0+time1+time2;
if (s==1)
{
        if (reg==1)
        {sa_0=5587968;}
        else if (reg==2)
        {sa_0=9848848;}
        else if (reg==3)
        {sa_0=9848080;}
        else
        {sa_0=10914068;}
}
/*=====================================*/
else if (s==2)
{
        if (reg==1)
        {sa_0=5587200;}
        else if (reg==2)
        {sa_0=10913300;}
        else if (reg==3)
        {sa_0=10851860;}
        else
        {sa_0=6652420;}
}
/*=====================================*/
else if (s==3)
{
        if (reg==1)
        {sa_0=5525760;}
        else if (reg==2)
        {sa_0=6590980;}
        else if (reg==3)
        {sa_0=6590788;}
        else
        {sa_0=6857285;}
}
/*=====================================*/
else if (s==4)
{
        if (reg==1)
        {sa_0=5525568;}
        else if (reg==2)
        {sa_0=6857093;}
        else if (reg==3)
        {sa_0=6906245;}
        else
        {sa_0=5841025;}
}
/*=====================================*/
else if (s==5)
{
        if (reg==1)
        {sa_0=5574720;}
```

```
            else if (reg==2)
            {sa_0=5841025;}
            else if (reg==3)
            {sa_0=5841985;}
            else
            {sa_0=10101905;}
}
/*==================================*/
else
{
            if (reg==1)
            {sa_0=5575680;}
            else if (reg==2)
            {sa_0=10102865;}
            else if (reg==3)
            {sa_0=10115153;}
            else
            {sa_0=9836560;}
}
                        LOAD_FIELD(&total_1,time00,0,8);
                        LOAD_FIELD(&total_1,time11,8,8);
                        LOAD_FIELD(&total_1,time22,16,8);
                  LOAD_FIELD(&total_2,sa_0,0,24);
                        LOAD_FIELD(&total_3,time000,0,8);
                        LOAD_FIELD(&total_3,time111,8,8);
                        LOAD_FIELD(&total_3,time222,16,8);

                        ++count_loop;
                        }

            }
interrupt void ahmed(void)
            {
                        WRITE1_DAUGHTER=total_1;
                        WRITE2_DAUGHTER=total_2;
                        WRITE3_DAUGHTER=total_3;
                        theta+=0.10294362112;/*2*pi*samp*50;      */
++count_intr;
            }
```

Appendix D

C code for the two-level APF

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "emif.h"
#include "AED_new.h"
#include "dma.h"
#include "math.h"
#include "intr.h"
#include "FPGA_CONTROL.h"

unsigned short int y,s,ss00,time0,time1,time2,time00,time11,time22;
unsigned short int offset_ica,offset_icb,offset_iLa,offset_iLb;
unsigned short int check_bit,offset_vc,offset_vsa,offset_vsb;
unsigned int count_loop=0,count_intr=0;
unsigned int ica_offset,icb_offset;
unsigned int vc_offset,vsa_offset,vsb_offset,jj,total,ADC[8];
unsigned int read_vc_1,read_vsa_1,read_vsb_1,read_vsc_1;
unsigned int read_ica_1,read_icb_1;
unsigned short int read_vc,read_vsa,read_vsb;
unsigned short int read_ica,read_icb;
float kp=0.1,ki_samp=0.000004096,ma,t1,t2,t0,theta,theta1;
float ica,icb,icc,vsa,vsb,vsc;
float vd,vq,vab,vbc,vca,max_input_voltage;
float p_cap=0,samp=0.00004096,value,cap_volt;
float ica_ref,icb_ref,icc_ref;
float va_ref,vb_ref,vc_ref,sum_1,delta_vcap;
int one;

interrupt void ahmed();

void main()

{
        board_init();

            RESET_BIT(DSP_CNTL_ADDR,XCNTL0);
             SET_BIT(DSP_CNTL_ADDR,XCNTL0);
             emif_init(0x00003078,
                       0x00000040,
                       0x40FD0220,
                       0x00000030,
                       0x00000030,
        0x07229000,
        0x00000619);

total=0X01C29030;

ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/
```

```
RESET_BIT(DSP_CNTL_ADDR,XCNTL0);
vc_offset=ADC[1]&0x0000ffff;
ica_offset=ADC[0]&0x0000ffff;
icb_offset=ADC[0]&0xffff0000;
icb_offset=icb_offset>>16;

vsa_offset=ADC[4]&0x0000ffff;
vsb_offset=ADC[4]&0xffff0000;
vsb_offset=vsb_offset>>16;

offset_vc=vc_offset;
offset_ica=ica_offset;
offset_icb=icb_offset;
offset_vsa=vsa_offset;
offset_vsb=vsb_offset;

SET_BIT(DSP_CNTL_ADDR,XCNTL0);

printf("enter 1\n\n");
scanf("%d",&one);

intr_map(CPU_INT7,ISN_EXT_INT7);
INTR_ENABLE(CPU_INT_NMI);
INTR_ENABLE(CPU_INT7);
SET_BIT(DSP_CNTL_ADDR,XCNTL1);

        intr_hook(ahmed,CPU_INT7);

while(1)
{
        while(GET_BIT(DSP_STAT_ADDR,XSTAT0)==0)
{ ;}
        ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
        ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
        ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
        ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
        ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
        ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
        ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
        ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/

        read_vc_1=ADC[1]&0x0000ffff;
        read_ica_1=ADC[0]&0x0000ffff;
        read_icb_1=ADC[0]&0xffff0000;
        read_icb_1=read_icb_1>>16;

        read_vsa_1=ADC[4]&0x0000ffff;
        read_vsb_1=ADC[4]&0xffff0000;
        read_vsb_1=read_vsb_1>>16;

        read_vc=read_vc_1;
        read_ica=read_ica_1;
        read_icb=read_icb_1;
        read_vsa=read_vsa_1;
        read_vsb=read_vsb_1;

        RESET_BIT(DSP_CNTL_ADDR,XCNTL0);

            cap_volt=0.293*(float)(read_vc-offset_vc);
            ica=0.002441*(float)(read_ica-offset_ica);
            icb=0.002441*(float)(read_icb-offset_icb);
```

```
                    icc=-ica-icb;

vab=0.0006278*(float)(read_vsa-offset_vsa);
vbc=0.0006278*(float)(read_vsb-offset_vsb);
                    vca=-vbc-vab;
                    vsa=vab-vca;
                    vsb=vbc-vab;
                    vsc=vca-vbc;

                    if (cap_volt>550)
                    {check_bit=1;}
                    else
                    {check_bit=0;}
                    delta_vcap=300-cap_volt;
                    sum_1=sum_1+ki_samp*delta_vcap;
                    p_cap=kp*delta_vcap+sum_1;

                    if (p_cap>2000)
                    {p_cap=2000;}
                    else if (p_cap<-2000)
                    {p_cap=-2000;}

                    ica_ref=vsa*p_cap;
                    icb_ref=vsb*p_cap;
                    icc_ref=vsc*p_cap;

                    va_ref=61*(ica-ica_ref)+155.56*vsa;
                    vb_ref=61*(icb-icb_ref)+155.56*vsb;
                    vc_ref=61*(icc-icc_ref)+155.56*vsc;

                    vd=0.5*(2*va_ref-vb_ref-vc_ref);
                    vq=0.866*(vb_ref-vc_ref);

                    value=sqrt(vd*vd+vq*vq);
                    theta=asin(vq/value);
                    if (vd<0&vq<0)
                    {theta=3.14159-theta;}
                    if (vd<0&vq>0)
                    {theta=3.14159-theta;}
                    if (vd>0&vq<0)
                    {theta=theta+2*3.14159;}

SET_BIT(DSP_CNTL_ADDR,XCNTL0);
if (theta>6.28318/*2*pi*/)
                    {theta-=6.28318;}

                    ss00=(int)(0.955*theta);
                    s=ss00+1;

                    theta1=theta-(1.0472)*ss00;

/* check over modulation*/
                    max_input_voltage=(259.8/sinf(theta1+1.0472))-1;
                    if (value>max_input_voltage)
                    {value=max_input_voltage;}

                    ma=0.0038491*value;

                    t1=ma*samp*sin(1.0472-theta1);
                    t2=ma*samp*sin(theta1);
                    t0=0.5*(samp-t1-t2);
```

```
time0=(int)(6250000*t0);
time1=(int)(6250000*t1);
time2=(int)(6250000*t2);

if (s==2||s==4||s==6)
{
y=time1;
time1=time2;
time2=y;
}
else
{
time1=time1;
time2=time2;
}

if (time0<4)
{time0=4;
time1=time1-4;
time2=time2-4;
}
if (time1<4)
{time1=4;
time2=time2-4;
time0=time0;
}
if (time2<4)
{
time2=4;
time1=time1-4;
                time0=time0;
                }

                time00=time0;
                time11=time0+time1;
                time22=time0+time1+time2;

          LOAD_FIELD(&total,time00,0,8);
                LOAD_FIELD(&total,time11,8,8);
                LOAD_FIELD(&total,time22,16,8);
                LOAD_FIELD(&total,s,24,3);
                LOAD_FIELD(&total,check_bit,27,1);
          ++count_loop;
        }
}

        interrupt void ahmed(void)
                {
    WRITE1_DAUGHTER=total;
    ++count_intr;
}
```

Appendix E

C code for the three-level APF

E.1 Using nromal SVM

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "math.h"
#include "intr.h"
#include "FPGA_3level.h"
#include "mathf.h"

unsigned short int offset_ica,offset_icb,read_ica,read_icb;
unsigned short int offset_vsab,offset_vsbc,read_vsab,read_vsbc;
unsigned short int offset_vcapa,offset_vcapb,offset_vcapc,read_vcapa,read_vcapb,read_vcapc;
unsigned short int y,s,ss00,time00,time11,time22,time0,time1,time2;
unsigned short int check_bit=1;
unsigned int sa_0,total_1,total_2,ADC[8];
unsigned int read_ica_1,read_icb_1,ica_offset,icb_offset;
unsigned int read_vsab_1,read_vsbc_1,vsab_offset,vsbc_offset;
unsigned int read_vcapa_1,read_vcapb_1,read_vcapc_1,vcapa_offset,vcapb_offset,vcapc_offset;
int trial,count_loop=0,count_intr=0;
float ma,t1,t2,t0,theta=0,theta1,samp=0.00004096;
float ma_3level,max_input_voltage;
float vd,vq,va_ref,vb_ref,vc_ref,value;
float ica,icb,icc,ica_ref,icb_ref,icc_ref;
float vsab,vsbc,vsca,vcapa,vcapb,vcapc,ida,idb,idc;
float delta_vcapa,delta_vcapb,delta_vcapc,sine_1,sine_2,sine_3,sine_4,sine_5;
float sum_a=0,sum_b=0,sum_c=0,kp=0.08,ki=8/*0.1*/,ki_samp=0.00032768/*0.000004096*/;
float va,vb,vc,ma_samp,cosec,bb;
unsigned int reg,a,b,h;
float ah[1000],ah1[1000],ah2[1000],ah3[1000],ah4[1000],ah5[1000],ah6[1000];
unsigned int init=0;

interrupt void ahmed();

void main()
{
/*************************************************************/
/* Initialize                                                */
/*************************************************************/
        board_init();
                RESET_BIT(0x1780000,XCNTL0);
        SET_BIT(0x1780000,XCNTL0);
emif_init(0x00003078,
                0x00000040,
                0x40FD0220,
                0x00000030,
                0x00000030,
                0x07229000,
                0x00000619);
    WRITE1_DAUGHTER=0X01C29030;
    WRITE2_DAUGHTER=0X00000000;

      ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
      ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
```

```
ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/

RESET_BIT(0x1780000,XCNTL0);

ica_offset=ADC[0]&0x0000ffff;
icb_offset=ADC[0]&0xffff0000;
icb_offset=icb_offset>>16;
offset_ica=ica_offset;
offset_icb=icb_offset;

vsab_offset=ADC[1]&0x0000ffff;
vsbc_offset=ADC[1]&0xffff0000;
vsbc_offset=vsbc_offset>>16;
offset_vsab=vsab_offset;
offset_vsbc=vsbc_offset;

vcapa_offset=ADC[2]&0x0000ffff;
vcapb_offset=ADC[2]&0xffff0000;
vcapb_offset=vcapb_offset>>16;
vcapc_offset=ADC[3]&0xffff0000;
vcapc_offset=vcapc_offset>>16;
offset_vcapa=vcapa_offset;
offset_vcapb=vcapb_offset;
offset_vcapc=vcapc_offset;

printf("enter the trial\n\n");
scanf("%d",&trial);

SET_BIT(0x1780000,XCNTL0);
intr_map(CPU_INT7,ISN_EXT_INT7);
INTR_ENABLE(CPU_INT_NMI);
INTR_ENABLE(CPU_INT7);
SET_BIT(0x1780000,XCNTL1);
intr_hook(ahmed,CPU_INT7);
/*=============================================================================*/
/*=============================================================================*/
        while (1)
        {
                while(GET_BIT(DSP_STAT_ADDR,XSTAT0)==0)
            { ;}

                ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
                ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
                ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
                ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
                ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
                ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
                ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
                ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/

                read_ica_1=ADC[0]&0x0000ffff;
                read_icb_1=ADC[0]&0xffff0000;
                read_icb_1=read_icb_1>>16;
                read_ica=read_ica_1;
                read_icb=read_icb_1;

                read_vsab_1=ADC[1]&0x0000ffff;
```

```
read_vsbc_1=ADC[1]&0xffff0000;
read_vsbc_1=read_vsbc_1>>16;
read_vsab=read_vsab_1;
read_vsbc=read_vsbc_1;

read_vcapa_1=ADC[2]&0x0000ffff;
read_vcapb_1=ADC[2]&0xffff0000;
read_vcapb_1=read_vcapb_1>>16;
read_vcapc_1=ADC[3]&0xffff0000;
read_vcapc_1=read_vcapc_1>>16;
read_vcapa=read_vcapa_1;
read_vcapb=read_vcapb_1;
read_vcapc=read_vcapc_1;

RESET_BIT(0x1780000,XCNTL0);
ica=0.002441*(float)(read_ica-offset_ica);
icb=0.002441*(float)(read_icb-offset_icb);
icc=-ica-icb;

vsab=0.0006278*(float)(read_vsab-offset_vsab);
vsbc=0.0006278*(float)(read_vsbc-offset_vsbc);
vsca=-vsab-vsbc;
va=vsab-vsca;
vb=vsbc-vsab;
vc=vsca-vsbc;

vcapa=0.293*(float)(read_vcapa-offset_vcapa);
vcapb=0.293*(float)(read_vcapb-offset_vcapb);
vcapc=0.293*(float)(read_vcapc-offset_vcapc);

        if (vcapa>450||vcapb>450||vcapc>450)
        {check_bit=0;}
        else
        {check_bit=1;}

delta_vcapa=160-vcapa;
delta_vcapb=160-vcapb;
delta_vcapc=160-vcapc;
sum_a=sum_a+ki_samp*delta_vcapa;
sum_b=sum_b+ki_samp*delta_vcapb;
sum_c=sum_c+ki_samp*delta_vcapc;

ida=kp*delta_vcapa+sum_a;
idb=kp*delta_vcapb+sum_b;
idc=kp*delta_vcapc+sum_c;

ica_ref=va*ida;
icb_ref=vb*idb;
icc_ref=vc*idc;

if (count_loop>0 & count_loop<1000)
{ah[init]=ica;
ah1[init]=icb;
ah2[init]=vsab;
ah3[init]=vsbc;
ah4[init]=vcapa;
ah5[init]=vcapb;
ah6[init]=vcapc;
++init;}

va_ref=61*(ica-ica_ref)+155.56*va;
vb_ref=61*(icb-icb_ref)+155.56*vb;
```

```
vc_ref=61*(icc-icc_ref)+155.56*vc;

vd=0.5*(2*va_ref-vb_ref-vc_ref);
vq=0.866*(vb_ref-vc_ref);
value=sqrtf(vd*vd+vq*vq);

theta=asinf(vq/value);
if (vd<0&vq<0)
{theta=3.14159-theta;}
if (vd<0&vq>0)
{theta=3.14159-theta;}
if (vd>0&vq<0)
{theta=theta+2*3.14159;}
                SET_BIT(0x1780000,XCNTL0);

                ss00=(int)(0.955*theta);
                s=ss00+1;
                theta1=theta-(1.0472)*ss00;

                sine_1=sinf(theta1+1.0472);
                sine_2=cosf(theta1+0.5236);
                sine_3=cosf(0.5236-theta1);
                sine_4=sinf(theta1);
                sine_5=sinf(1.0472-theta1);

/*================================================================*/
                /* check over modulation*/
                        max_input_voltage=(277.12/sine_1)-0.5;
                        if (value>max_input_voltage)
                        {value=max_input_voltage;}

                /*ma=vm/(E*(m-1)*0.866);*/
                ma=0.0036085*value;
                ma_3level=2*ma;

                a=(int)(ma_3level*sine_2)+1;
                b=(int)(ma_3level*sine_3)+1;
                h=(int)(ma_3level*sine_4)+1;

                reg=-a+b*b-b+1+h;

                /*ma_samp=ma_3level*samp;                */
                ma_samp=ma_3level*256;

                        if (reg==1)
                        {t1=ma_samp*sine_5;
                         t2=ma_samp*sine_4;}
                         else if (reg==2)
                        {t1=ma_samp*sine_5-256;
                        t2=ma_samp*sine_4;}
                        else if (reg==3)
                        {t1=256-ma_samp*sine_5;
                        t2=ma_samp*sine_1-256;}
                        else
                        {t1=ma_samp*sine_5;
                        t2=ma_samp*sine_4-256;}

                        t0=0.5*(256-t1-t2);

                time0=(int)(t0);            /*(int)(256*t0/samp);*/
                time1=(int)(t1);            /*(int)(256*t1/samp);*/
```

```
                time2=(int)(t2);            /*(int)(256*t2/samp);*/


        if (s==2||s==4||s==6)
        {
        y=time1;
        time1=time2;
        time2=y;
        }

        time00=time0;
        time11=time0+time1;
        time22=time0+time1+time2;
        if (s==1)
        {
                if (reg==1)
                {sa_0=5587968;}
                else if (reg==2)
                {sa_0=9848848;}
                else if (reg==3)
                {sa_0=9848080;}
                else
                {sa_0=10914068;}
        }
        /*=====================================*/
        else if (s==2)
        {
                if (reg==1)
                {sa_0=5587200;}
                else if (reg==2)
                {sa_0=10913300;}
                else if (reg==3)
                {sa_0=10851860;}
                else
                {sa_0=6652420;}
        }
        /*=====================================*/
        else if (s==3)
        {
                if (reg==1)
                {sa_0=5525760;}
                else if (reg==2)
                {sa_0=6590980;}
                else if (reg==3)
                {sa_0=6590788;}
                else
                {sa_0=6857285;}
        }
        /*=====================================*/
        else if (s==4)
        {
                if (reg==1)
                {sa_0=5525568;}
                else if (reg==2)
                {sa_0=6857093;}
                else if (reg==3)
                {sa_0=6906245;}
                else
                {sa_0=5841025;}
        }
        /*=====================================*/
```

```
else if (s==5)
{
        if (reg==1)
        {sa_0=5574720;}
        else if (reg==2)
        {sa_0=5841025;}
        else if (reg==3)
        {sa_0=5841985;}
        else
        {sa_0=10101905;}
}
/*=================================*/
else
{
        if (reg==1)
        {sa_0=5575680;}
        else if (reg==2)
        {sa_0=10102865;}
        else if (reg==3)
        {sa_0=10115153;}
        else
        {sa_0=9836560;}
}
                        LOAD_FIELD(&total_1,time00,0,8);
                        LOAD_FIELD(&total_1,time11,8,8);
                        LOAD_FIELD(&total_1,time22,16,8);
                        LOAD_FIELD(&total_1,check_bit,27,1);
                        LOAD_FIELD(&total_2,sa_0,0,24);
                        ++count_loop;
                        }
        }
        interrupt void ahmed(void)
                {
                        WRITE1_DAUGHTER=total_1;
                        WRITE2_DAUGHTER=total_2;
                        ++count_intr;
                }
```

E.2 Using PS-SVM

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "emif.h"
#include "dma.h"
#include "math.h"
#include "intr.h"
#include "FPGA_CONTROL_3level.h"
#include "AED_new.h"
#include "mathf.h"

unsigned short int offset_ica,offset_icb,read_ica,read_icb;
unsigned short int offset_vsab,offset_vsbc,read_vsab,read_vsbc;
unsigned short int offset_vcapa,offset_vcapb,offset_vcapc,read_vcapa,read_vcapb,read_vcapc;
unsigned short int y,s,ss00,time00,time11,time22,time0,time1,time2;
unsigned short int check_bit=1;
unsigned int total,ADC[8];
unsigned int read_ica_1,read_icb_1,ica_offset,icb_offset;
unsigned int read_vsab_1,read_vsbc_1,vsab_offset,vsbc_offset;
```

```
unsigned int read_vcapa_1,read_vcapb_1,read_vcapc_1,vcapa_offset,vcapb_offset,vcapc_offset;
int trial,count_loop=0,count_intr=0;
float ma,t1,t2,t0,theta=0,theta1,samp=0.00004096;
float max_input_voltage;
float vd,vq,va_ref,vb_ref,vc_ref,value;
float ica,icb,icc,ica_ref,icb_ref,icc_ref;
float vsab,vsbc,vsca,vcapa,vcapb,vcapc,ida,idb,idc;
float delta_vcapa,delta_vcapb,delta_vcapc;
float sum_a=0,sum_b=0,sum_c=0,kp=0.08,ki=8/*0.1*/,ki_samp=0.00032768/*0.000004096*/;
float va,vb,vc;
unsigned int init=0;

interrupt void ahmed();

void main()
{
                board_init();
                RESET_BIT(DSP_CNTL_ADDR,XCNTL0);
                SET_BIT(DSP_CNTL_ADDR,XCNTL0);
        emif_init(0x00003078,
                  0x00000040,
                  0x40FD0220,
                  0x00000030,
                  0x00000030,
                  0x07229000,
                  0x00000619);

       WRITE1_DAUGHTER=0X01C29030;

                  ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
                  ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
                  ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
                  ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
                  ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
                  ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
                  ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
                  ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/

       RESET_BIT(DSP_CNTL_ADDR,XCNTL0);
       ica_offset=ADC[0]&0x0000ffff;
       icb_offset=ADC[0]&0xffff0000;
       icb_offset=icb_offset>>16;
       offset_ica=ica_offset;
       offset_icb=icb_offset;

       vsab_offset=ADC[1]&0x0000ffff;
       vsbc_offset=ADC[1]&0xffff0000;
       vsbc_offset=vsbc_offset>>16;
       offset_vsab=vsab_offset;
       offset_vsbc=vsbc_offset;

       vcapa_offset=ADC[2]&0x0000ffff;
       vcapb_offset=ADC[2]&0xffff0000;
       vcapb_offset=vcapb_offset>>16;
       vcapc_offset=ADC[3]&0xffff0000;
       vcapc_offset=vcapc_offset>>16;
       offset_vcapa=vcapa_offset;
       offset_vcapb=vcapb_offset;
       offset_vcapc=vcapc_offset;

       printf("enter the trial\n\n");
       scanf("%d",&trial);
```

```
                    SET_BIT(DSP_CNTL_ADDR,XCNTL0);
                    intr_map(CPU_INT7,ISN_EXT_INT7);
                    INTR_ENABLE(CPU_INT_NMI);
                    INTR_ENABLE(CPU_INT7);
                    SET_BIT(DSP_CNTL_ADDR,XCNTL1);
                    intr_hook(ahmed,CPU_INT7);
/*==========================================================================*/
/*==========================================================================*/
        while (1)
        {
                while(GET_BIT(DSP_STAT_ADDR,XSTAT0)==0)
{ ;}

                ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
                ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
                ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
                ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
                ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
                ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
                ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
                ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/

                read_ica_1=ADC[0]&0x0000ffff;
                read_icb_1=ADC[0]&0xffff0000;
                read_icb_1=read_icb_1>>16;
                read_ica=read_ica_1;
                read_icb=read_icb_1;

                read_vsab_1=ADC[1]&0x0000ffff;
                read_vsbc_1=ADC[1]&0xffff0000;
                read_vsbc_1=read_vsbc_1>>16;
                read_vsab=read_vsab_1;
                read_vsbc=read_vsbc_1;

                read_vcapa_1=ADC[2]&0x0000ffff;
                read_vcapb_1=ADC[2]&0xffff0000;
                read_vcapb_1=read_vcapb_1>>16;
                read_vcapc_1=ADC[3]&0xffff0000;
               read_vcapc_1=read_vcapc_1>>16;
                read_vcapa=read_vcapa_1;
                read_vcapb=read_vcapb_1;
                read_vcapc=read_vcapc_1;

                RESET_BIT(DSP_CNTL_ADDR,XCNTL0);

                        ica=0.002441*(float)(read_ica-offset_ica);
                        icb=0.002441*(float)(read_icb-offset_icb);
                        icc=-ica-icb;

                vsab=0.0006278*(float)(read_vsab-offset_vsab);
                vsbc=0.0006278*(float)(read_vsbc-offset_vsbc);
                vsca=-vsab-vsbc;
                va=vsab-vsca;
                vb=vsbc-vsab;
                vc=vsca-vsbc;

                vcapa=0.293*(float)(read_vcapa-offset_vcapa);
                vcapb=0.293*(float)(read_vcapb-offset_vcapb);
                vcapc=0.293*(float)(read_vcapc-offset_vcapc);
```

```
if (vcapa>450||vcapb>450||vcapc>450)
{check_bit=0;}
else
{check_bit=1;}

delta_vcapa=160-vcapa;
delta_vcapb=160-vcapb;
delta_vcapc=160-vcapc;

sum_a=sum_a+ki_samp*delta_vcapa;
sum_b=sum_b+ki_samp*delta_vcapb;
sum_c=sum_c+ki_samp*delta_vcapc;
ida=kp*delta_vcapa+sum_a;
idb=kp*delta_vcapb+sum_b;
idc=kp*delta_vcapc+sum_c;

ica_ref=va*ida;
icb_ref=vb*idb;
icc_ref=vc*idc;

va_ref=61*(ica-ica_ref)+155.56*va;
vb_ref=61*(icb-icb_ref)+155.56*vb;
vc_ref=61*(icc-icc_ref)+155.56*vc;

vd=0.5*(2*va_ref-vb_ref-vc_ref);
vq=0.866*(vb_ref-vc_ref);

value=sqrtf(vd*vd+vq*vq);
theta=asinf(vq/value);
if (vd<0&vq<0)
{theta=3.14159-theta;}
if (vd<0&vq>0)
{theta=3.14159-theta;}
if (vd>0&vq<0)
{theta=theta+2*3.14159;}

    SET_BIT(DSP_CNTL_ADDR,XCNTL0);
/*=============================================================*/

ss00=(int)(0.955*theta);
s=ss00+1;
theta1=theta-(1.0472)*ss00;

/* check over modulation*/
max_input_voltage=(277.12/*346.4*//sinf(theta1+1.0472))-0.274;
if (value>max_input_voltage)
{value=max_input_voltage;}

ma=0.0036085*value;

/*calculation of the time distribution between the states*/
t1=ma*samp*sinf(1.0472-theta1);
t2=ma*samp*sinf(theta1);
t0=0.5*(samp-t1-t2);

/* convert t00,t11,t22 to the number of counts required in fpga*/
time0=(int)(6250000*t0);
time1=(int)(6250000*t1);  /* time1=(int)(256*t11/samp);*/
time2=(int)(6250000*t2);  /* time2=(int)(256*t22/samp);*/

if (s==2||s==4||s==6)
{
```

```
y=time1;
time1=time2;
time2=y;
}

if (time0<2)
{time0=2;
time1=time1-2;
time2=time2-2;
}
if (time1<2)
{time1=2;
time2=time2-2;
time0=time0;
}
if (time2<2)
{
time2=2;
time1=time1-2;
time0=time0;
}

time00=time0;
time11=time0+time1;
time22=time0+time1+time2;

LOAD_FIELD(&total,time00,0,8);
LOAD_FIELD(&total,time11,8,8);
LOAD_FIELD(&total,time22,16,8);
LOAD_FIELD(&total,s,24,3);
LOAD_FIELD(&total,check_bit,27,1);
                ++count_loop;
        }
}

        interrupt void ahmed(void)
                {
                        WRITE1_DAUGHTER=total;
                        ++count_intr;
                }
```

Appendix F

C code for the five-level APF

F.1 Using PS-SVM

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "emif.h"
#include "dma.h"
#include "math.h"
#include "intr.h"
#include "FPGA_CONTROL_3level.h"
#include "AED_new.h"
#include "mathf.h"

unsigned short int offset_ica,offset_icb,read_ica,read_icb;
unsigned short int offset_vsab,offset_vsbc,read_vsab,read_vsbc;
unsigned short int offset_vcapa,offset_vcapb,offset_vcapc,read_vcapa,read_vcapb,read_vcapc;
unsigned short int offset_vcapa2,offset_vcapb2,offset_vcapc2,read_vcapa2,read_vcapb2,read_vcapc2;
unsigned short int y,s,ss00,time00,time11,time22,time0,time1,time2;
unsigned short int check_bit=1,change=0;
unsigned int total,ADC[8];
unsigned int read_ica_1,read_icb_1,ica_offset,icb_offset;
unsigned int read_vsab_1,read_vsbc_1,vsab_offset,vsbc_offset;
unsigned int read_vcapa_1,read_vcapb_1,read_vcapc_1,vcapa_offset,vcapb_offset,vcapc_offset;
unsigned int read_vcapa_2,read_vcapb_2,read_vcapc_2,vcapa2_offset,vcapb2_offset,vcapc2_offset;
int trial,count_loop=0,count_intr=0;
float ma,t1,t2,t0,theta=0,theta1,samp=0.00004096;
float max_input_voltage;
float vd,vq,va_ref,vb_ref,vc_ref,value;
float ica,icb,icc,ica_ref,icb_ref,icc_ref;
float vsab,vsbc,vsca,vcapa,vcapb,vcapc,ida,idb,idc;
float vcapa2,vcapb2,vcapc2;
float delta_vcapa,delta_vcapb,delta_vcapc;
float sum_a=0,sum_b=0,sum_c=0,kp=0.08,ki=/*8*/0.1,ki_samp=/*0.00032768*/0.000004096;
float va,vb,vc;
unsigned int init=0;
int aa=0,bb=0,dd1=0,dd2=0,dd3=0,dd4=0,dd5=0,dd6=0,dd7=0,nn=1;

interrupt void ahmed();

void main()
{
                board_init();
                RESET_BIT(DSP_CNTL_ADDR,XCNTL0);
SET_BIT(DSP_CNTL_ADDR,XCNTL0);
emif_init(0x00003078,
                0x00000040,
                0x40FD0220,
                0x00000030,
                0x00000030,
                0x07229000,
                0x00000619);

  WRITE1_DAUGHTER=0X01C29030;

  ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
  ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
```

```
ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/

RESET_BIT(DSP_CNTL_ADDR,XCNTL0);
ica_offset=ADC[0]&0x0000ffff;
icb_offset=ADC[0]&0xffff0000;
icb_offset=icb_offset>>16;
offset_ica=ica_offset;
offset_icb=icb_offset;

vsab_offset=ADC[1]&0x0000ffff;
vsbc_offset=ADC[1]&0xffff0000;
vsbc_offset=vsbc_offset>>16;
offset_vsab=vsab_offset;
offset_vsbc=vsbc_offset;

vcapa_offset=ADC[2]&0x0000ffff;
vcapb_offset=ADC[2]&0xffff0000;
vcapb_offset=vcapb_offset>>16;
vcapc_offset=ADC[3]&0xffff0000;
vcapc_offset=vcapc_offset>>16;
offset_vcapa=vcapa_offset;
offset_vcapb=vcapb_offset;
offset_vcapc=vcapc_offset;

vcapa2_offset=ADC[4]&0x0000ffff;
vcapb2_offset=ADC[4]&0xffff0000;
vcapb2_offset=vcapb2_offset>>16;
vcapc2_offset=ADC[5]&0x0000ffff;
offset_vcapa2=vcapa2_offset;
offset_vcapb2=vcapb2_offset;
offset_vcapc2=vcapc2_offset;

 printf("enter the trial\n\n");
scanf("%d",&trial);

SET_BIT(DSP_CNTL_ADDR,XCNTL0);
intr_map(CPU_INT7,ISN_EXT_INT7);
INTR_ENABLE(CPU_INT_NMI);
INTR_ENABLE(CPU_INT7);
SET_BIT(DSP_CNTL_ADDR,XCNTL1);
intr_hook(ahmed,CPU_INT7);
/*=============================================================================*/
/*=============================================================================*/
while (1)
{
        while(GET_BIT(DSP_STAT_ADDR,XSTAT0)==0)
            { ;}

          ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
          ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
          ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
          ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
          ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
          ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
          ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
          ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/
```

```
read_ica_1=ADC[0]&0x0000ffff;
read_icb_1=ADC[0]&0xffff0000;
read_icb_1=read_icb_1>>16;
read_ica=read_ica_1;
read_icb=read_icb_1;

read_vsab_1=ADC[1]&0x0000ffff;
read_vsbc_1=ADC[1]&0xffff0000;
read_vsbc_1=read_vsbc_1>>16;
read_vsab=read_vsab_1;
read_vsbc=read_vsbc_1;

read_vcapa_1=ADC[2]&0x0000ffff;
read_vcapb_1=ADC[2]&0xffff0000;
read_vcapb_1=read_vcapb_1>>16;
read_vcapc_1=ADC[3]&0xffff0000;
read_vcapc_1=read_vcapc_1>>16;
read_vcapa=read_vcapa_1;
read_vcapb=read_vcapb_1;
read_vcapc=read_vcapc_1;

read_vcapa_2=ADC[4]&0x0000ffff;
read_vcapb_2=ADC[4]&0xffff0000;
read_vcapb_2=read_vcapb_2>>16;
read_vcapc_2=ADC[5]&0x0000ffff;
read_vcapa2=read_vcapa_2;
read_vcapb2=read_vcapb_2;
read_vcapc2=read_vcapc_2;

        RESET_BIT(DSP_CNTL_ADDR,XCNTL0);

ica=0.002441*(float)(read_ica-offset_ica);
icb=0.002441*(float)(read_icb-offset_icb);
icc=-ica-icb;

vsab=0.0006278*(float)(read_vsab-offset_vsab);
vsbc=0.0006278*(float)(read_vsbc-offset_vsbc);
vsca=-vsab-vsbc;
va=vsab-vsca;
vb=vsbc-vsab;
vc=vsca-vsbc;

vcapa=0.293*(float)(read_vcapa-offset_vcapa);
 vcapb=0.293*(float)(read_vcapb-offset_vcapb);
vcapc=0.293*(float)(read_vcapc-offset_vcapc);
vcapa2=0.293*(float)(read_vcapa2-offset_vcapa2);
vcapb2=0.293*(float)(read_vcapb2-offset_vcapb2);
vcapc2=0.293*(float)(read_vcapc2-offset_vcapc2);

if (vcapa>350||vcapb>350||vcapc>350)
{check_bit=0;}
else
{check_bit=1;}

if (check_bit==1)
{
        if (vcapa2>350||vcapb2>350||vcapc2>350)
        {check_bit=0;}
        else
        {check_bit=1;}

        if (check_bit==1)
```

```
{
        if (vcapa<5||vcapb<5||vcapc<5)
        {check_bit=0;}
        else
        {check_bit=1;}

        if (check_bit==1)
        {
                if (vcapa2<5||vcapb2<5||vcapc2<5)
                {check_bit=0;}
                else
                {check_bit=1;}
        }
                }
        }

/* multiplexing action for both sets in each cycle*/
                dd7=dd6;
                dd6=dd5;
                dd5=dd4;
                dd4=dd3;
                dd3=dd2;
                dd2=dd1;
                bb=aa;
                if (va>0)
                {aa=3;
                dd1=0;
                dd2=0;
                dd3=0;
                dd4=0;
                dd5=0;
                dd6=0;
                }
                else
                {aa=1;
                ++dd1;}

                if (aa-bb==2)
                {if (dd7>60)
                        {++nn;}
                }

                if (nn%2==0)
                {change=0;}
                else
                {change=1;}
/*================================================*/
                delta_vcapa=100-vcapa;
                delta_vcapb=100-vcapb;
                delta_vcapc=100-vcapc;
                sum_a=sum_a+ki_samp*delta_vcapa;
                sum_b=sum_b+ki_samp*delta_vcapb;
                sum_c=sum_c+ki_samp*delta_vcapc;
                ida=kp*delta_vcapa+sum_a;
                idb=kp*delta_vcapb+sum_b;
                idc=kp*delta_vcapc+sum_c;

                ica_ref=va*ida;
                icb_ref=vb*idb;
                icc_ref=vc*idc;

                va_ref=61*(ica-ica_ref)+155.56*va;
```

```
vb_ref=61*(icb-icb_ref)+155.56*vb;
vc_ref=61*(icc-icc_ref)+155.56*vc;
vd=0.5*(2*va_ref-vb_ref-vc_ref);
vq=0.866*(vb_ref-vc_ref);

value=sqrtf(vd*vd+vq*vq);
theta=asinf(vq/value);
if (vd<0&vq<0)
{theta=3.14159-theta;}
if (vd<0&vq>0)
{theta=3.14159-theta;}
if (vd>0&vq<0)
{theta=theta+2*3.14159;}
        SET_BIT(DSP_CNTL_ADDR,XCNTL0);
/*=============================================================*/

ss00=(int)(0.955*theta);
s=ss00+1;
theta1=theta-(1.0472)*ss00;

/* check over modulation*/
max_input_voltage=(346.4/sinf(theta1+1.0472))-0.274;
if (value>max_input_voltage)
{value=max_input_voltage;}
ma=0.002886836*value;

/*calculation of the time distribution between the states*/
t1=ma*samp*sinf(1.0472-theta1);
t2=ma*samp*sinf(theta1);
t0=0.5*(samp-t1-t2);

/* convert t00,t11,t22 to the number of counts required in fpga*/
time0=(int)(6250000*t0);
time1=(int)(6250000*t1);
time2=(int)(6250000*t2);

if (s==2||s==4||s==6)
{
y=time1;
time1=time2;
time2=y;
}

if (time0<3)
{time0=3;
time1=time1-3;
time2=time2-3;
}
if (time1<3)
{time1=3;
time2=time2-3;
time0=time0;
}
if (time2<3)
{
time2=3;
time1=time1-3;
time0=time0;
}

time00=time0;
```

```
                        time11=time0+time1;
                        time22=time0+time1+time2;

                        LOAD_FIELD(&total,time00,0,8);
                        LOAD_FIELD(&total,time11,8,8);
                        LOAD_FIELD(&total,time22,16,8);
                        LOAD_FIELD(&total,s,24,3);
                        LOAD_FIELD(&total,check_bit,27,1);
                        LOAD_FIELD(&total,change,29,1);
                        ++count_loop;
                }
}
interrupt void ahmed(void)
        {
                WRITE1_DAUGHTER=total;
                ++count_intr;
        }
```

F.2 Using H-SVM

```
#include <stdlib.h>
#include <stdio.h>
#include "regs.h"
#include "math.h"
#include "intr.h"
#include "FPGA_3level.h"
#include "mathf.h"

unsigned short int offset_ica,offset_icb,read_ica,read_icb;
unsigned short int offset_vsab,offset_vsbc,read_vsab,read_vsbc;
unsigned short int offset_vcapa,offset_vcapb,offset_vcapc,read_vcapa,read_vcapb,read_vcapc;
unsigned short int offset_vcapa2,offset_vcapb2,offset_vcapc2,read_vcapa2,read_vcapb2,read_vcapc2;
unsigned short int y,s,ss00,time00,time11,time22,time0,time1,time2;
unsigned short int check_bit=1,change=0;
unsigned int total_1,total_2,ADC[8];
unsigned int read_ica_1,read_icb_1,ica_offset,icb_offset;
unsigned int read_vsab_1,read_vsbc_1,vsab_offset,vsbc_offset;
unsigned int read_vcapa_1,read_vcapb_1,read_vcapc_1,vcapa_offset,vcapb_offset,vcapc_offset;
unsigned int read_vcapa_2,read_vcapb_2,read_vcapc_2,vcapa2_offset,vcapb2_offset,vcapc2_offset;
int trial,count_loop=0,count_intr=0;
float vd,vq,va_ref,vb_ref,vc_ref,value;
float ica,icb,icc,ica_ref,icb_ref,icc_ref;
float ida,idb,idc;
int
vcapa,vcapb,vcapc,vcapa2,vcapb2,vcapc2,delta_vcapa,delta_vcapb,delta_vcapc,vsab,vsbc,vsca,va,vb,vc;
float
sum_a=0,sum_b=0,sum_c=0,kp=0.000014715632/*0.293*0.08*0.0006278*/,ki=/*8*/0.1,ki_samp=/*0.0
0032768*/0.00000000753440358/*0.293*0.000004096*0.0006278*/;
float gain;
unsigned int init=0;
int aa=0,bb=0,dd1=0,dd2=0,dd3=0,dd4=0,dd5=0,dd6=0,dd7=0,nn=1;
float ma,m,t1,t2,t0,theta=0,theta1,samp=0.00004096;
float ma_3level,max_input_voltage,sine_1,sine_2,sine_3,sine_4,sine_5;
float v_input_new,input_voltage,ma_samp,abc;
unsigned int sa_0;
unsigned int reg,a,b,h;
```

Appendix F: C code for the five-level APF

```
interrupt void ahmed();

void main()
{
            board_init();
            RESET_BIT(0x1780000,XCNTL0);
            SET_BIT(0x1780000,XCNTL0);
           emif_init(0x00003078,
                     0x00000040,
                     0x40FD0220,
                      0x00000030,
                      0x00000030,
                      0x07229000,
                      0x00000619);
           WRITE1_DAUGHTER=0X01C29030;
           WRITE2_DAUGHTER=0X00000000;/* 1C29030;*/

              ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
              ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
              ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
              ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
              ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
              ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
              ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
              ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/

              RESET_BIT(0x1780000,XCNTL0);
              ica_offset=ADC[0]&0x0000ffff;
              offset_ica=ica_offset;

                        printf("enter the trial\n\n");
                        scanf("%d",&trial);

                        SET_BIT(0x1780000,XCNTL0);
                        intr_map(CPU_INT7,ISN_EXT_INT7);
                        INTR_ENABLE(CPU_INT_NMI);
                        INTR_ENABLE(CPU_INT7);
                        SET_BIT(0x1780000,XCNTL1);
                        intr_hook(ahmed,CPU_INT7);
/*=============================================================================*/
/*=============================================================================*/
              while (1)
              {
              while(GET_BIT(DSP_STAT_ADDR,XSTAT0)==0)
                   { ;}

                        ADC[0]= READ_DAUGHTER;  /*u5ap,u6ap*/
                        ADC[1]= READ_DAUGHTER;  /*u7ap,u8ap*/
                        ADC[2]= READ_DAUGHTER;  /*u5am,u6am*/
                        ADC[3]= READ_DAUGHTER;  /*u7am,u8am*/
                        ADC[4]= READ_DAUGHTER;  /*u5bp,u6bp*/
                        ADC[5]= READ_DAUGHTER;  /*u7bp,u8bp*/
                        ADC[6]= READ_DAUGHTER;  /*u5bm,u6bm*/
                        ADC[7]= READ_DAUGHTER;  /*u7bm,u8bp*/

                        read_ica_1=ADC[0]&0x0000ffff;
                        read_icb_1=ADC[0]&0xffff0000;
                        read_icb_1=read_icb_1>>16;
                        read_ica=read_ica_1;
                        read_icb=read_icb_1;
```

```
read_vsab_1=ADC[1]&0x0000ffff;
read_vsbc_1=ADC[1]&0xffff0000;
read_vsbc_1=read_vsbc_1>>16;
read_vsab=read_vsab_1;
read_vsbc=read_vsbc_1;

read_vcapa_1=ADC[2]&0x0000ffff;
read_vcapb_1=ADC[2]&0xffff0000;
read_vcapb_1=read_vcapb_1>>16;
read_vcapc_1=ADC[3]&0xffff0000;
read_vcapc_1=read_vcapc_1>>16;
read_vcapa=read_vcapa_1;
read_vcapb=read_vcapb_1;
read_vcapc=read_vcapc_1;

read_vcapa_2=ADC[4]&0x0000ffff;
read_vcapb_2=ADC[4]&0xffff0000;
read_vcapb_2=read_vcapb_2>>16;
read_vcapc_2=ADC[5]&0x0000ffff;
read_vcapa2=read_vcapa_2;
read_vcapb2=read_vcapb_2;
read_vcapc2=read_vcapc_2;

RESET_BIT(0x1780000,XCNTL0);

        ica=0.002441*(float)(read_ica-offset_ica);
        icb=0.002441*(float)(read_icb-offset_ica/*b*/);
        icc=-ica-icb;

        vsab=(read_vsab-offset_ica/*vsab*/);
        vsbc=(read_vsbc-offset_ica/*vsbc*/);
        vsca=-vsab-vsbc;
        va=vsab-vsca;
        vb=vsbc-vsab;
        vc=vsca-vsbc;
        abc=vsab*0.0006278;

        vcapa=(read_vcapa-offset_ica/*vcapa*/);
        vcapb=(read_vcapb-offset_ica/*vcapb*/);
        vcapc=(read_vcapc-offset_ica/*vcapc*/);
        vcapa2=(read_vcapa2-offset_ica/*vcapa2*/);
        vcapb2=(read_vcapb2-offset_ica/*vcapb2*/);
        vcapc2=(read_vcapc2-offset_ica/*vcapc2*/);

        if (vcapa>1195||vcapb>1195||vcapc>1195)
        {check_bit=0;}
        else
        {check_bit=1;}

        if (check_bit==1)
        {
                if (vcapa2>1195||vcapb2>1195||vcapc2>1195)
                {check_bit=0;}
                else
                {check_bit=1;}
                }

        /* multiplexing action for both sets in each cycle*/
        dd4=dd3;
        dd3=dd2;
        dd2=dd1;
```

```
bb=aa;
if (va>0)
{aa=3;
dd1=0;
dd2=0;
dd3=0;
}
else
{aa=1;
++dd1;}

if (aa-bb==2)
{if (dd4>60)
        {++nn;}
}

if (nn%2==0)
{change=0;}
else
{change=1;}

/*==================================================*/
delta_vcapa=342-vcapa;
delta_vcapb=342-vcapb;
delta_vcapc=342-vcapc;

sum_a=sum_a+ki_samp*delta_vcapa;
sum_b=sum_b+ki_samp*delta_vcapb;
sum_c=sum_c+ki_samp*delta_vcapc;

ida=kp*delta_vcapa+sum_a;
idb=kp*delta_vcapb+sum_b;
idc=kp*delta_vcapc+sum_c;
ica_ref=va*ida;
icb_ref=vb*idb;
icc_ref=vc*idc;

va_ref=61*(ica-ica_ref)+0.097661*va;
vb_ref=61*(icb-icb_ref)+0.097661*vb;
vc_ref=61*(icc-icc_ref)+0.097661*vc;
vd=0.5*(2*va_ref-vb_ref-vc_ref);
vq=0.866*(vb_ref-vc_ref);

value=sqrtf(vd*vd+vq*vq);
theta=asinf(vq/value);
if (vd<0&vq<0)
{theta=3.14159-theta;}
if (vd<0&vq>0)
{theta=3.14159-theta;}
if (vd>0&vq<0)
{theta=theta+2*3.14159;}

    SET_BIT(0x1780000,XCNTL0);
/*==================================================*/

ss00=(int)(0.955*theta);
s=ss00+1;
theta1=theta-(1.0472)*ss00;
sine_1=sinf(theta1+1.0472);
sine_2=cosf(theta1+0.5236);
sine_3=cosf(0.5236-theta1);
sine_4=sinf(theta1);
```

```
                sine_5=sinf(1.0472-theta1);

        /* check over modulation*/
                max_input_voltage=(346.4/sine_1)-0.278;
                if (value>max_input_voltage)
                {value=max_input_voltage;}

                ma=0.002886836*value;
                ma_3level=2*ma;

                a=(int)(ma_3level*sine_2)+1;
                b=(int)(ma_3level*sine_3)+1;
                h=(int)(ma_3level*sine_4)+1;
                reg=-a+b*b-b+1+h;

                ma_samp=ma_3level*256;
                if (reg==1)
                {t1=ma_samp*sine_5;
                 t2=ma_samp*sine_4;}
                 else if (reg==2)
                 {t1=ma_samp*sine_5-256;
                 t2=ma_samp*sine_4;}
                 else if (reg==3)
                 {t1=256-ma_samp*sine_5;
                 t2=ma_samp*sine_1-256;}
                 else
                 {t1=ma_samp*sine_5;
                 t2=ma_samp*sine_4-256;}

                 t0=0.5*(256-t1-t2);
                        time0=(int)(t0);          /*(int)(256*t0/samp);*/
                        time1=(int)(t1);          /*(int)(256*t1/samp);*/
                        time2=(int)(t2);          /*(int)(256*t2/samp);*/

                if (s==2||s==4||s==6)
                {
                y=time1;
                time1=time2;
                time2=y;
                }

                time00=time0;
                time11=time0+time1;
                time22=time0+time1+time2;


if (s==1)
{
        if (reg==1)
        {sa_0=5587968;}
        else if (reg==2)
        {sa_0=9848848;}
        else if (reg==3)
        {sa_0=9848080;}
        else
        {sa_0=10914068;}
}
/*=================================*/
else if (s==2)
{
        if (reg==1)
```

```
            {sa_0=5587200;}
            else if (reg==2)
            {sa_0=10913300;}
            else if (reg==3)
            {sa_0=10851860;}
            else
            {sa_0=6652420;}
}
/*================================*/
else if (s==3)
{
            if (reg==1)
            {sa_0=5525760;}
            else if (reg==2)
            {sa_0=6590980;}
            else if (reg==3)
            {sa_0=6590788;}
            else
            {sa_0=6857285;}
}
/*================================*/
else if (s==4)
{
            if (reg==1)
            {sa_0=5525568;}
            else if (reg==2)
            {sa_0=6857093;}
            else if (reg==3)
            {sa_0=6906245;}
            else
            {sa_0=5841025;}
}
/*================================*/
else if (s==5)
{
            if (reg==1)
            {sa_0=5574720;}
            else if (reg==2)
            {sa_0=5841025;}
            else if (reg==3)
            {sa_0=5841985;}
            else
            {sa_0=10101905;}
}
/*================================*/
else
{
            if (reg==1)
            {sa_0=5575680;}
            else if (reg==2)
            {sa_0=10102865;}
            else if (reg==3)
            {sa_0=10115153;}
            else
            {sa_0=9836560;}
}

                        LOAD_FIELD(&total_1,time00,0,8);
                        LOAD_FIELD(&total_1,time11,8,8);
                        LOAD_FIELD(&total_1,time22,16,8);
                        LOAD_FIELD(&total_1,check_bit,27,1);
                        LOAD_FIELD(&total_1,change,29,1);
```

```
                    LOAD_FIELD(&total_2,sa_0,0,24);
                    ++count_loop;
                    }

}
interrupt void ahmed(void)
        {
                    WRITE1_DAUGHTER=total_1;
                    WRITE2_DAUGHTER=total_2;
                    ++count_intr;
        }
```

Appendix G

Practical results using R-L and R-C loads

The practical results for the thee-level and five-level APF have been performed using a three-phase diode bridge feeding series R-L and parallel R-C loads. The parameters of the series R-L and parallel R-C loads are (R = 62 Ohm, L = 100 mH and R = 235 Ohm, C = 2.2 mF).

G.1 Three-level APF using normal-SVM

i. Using R-L load

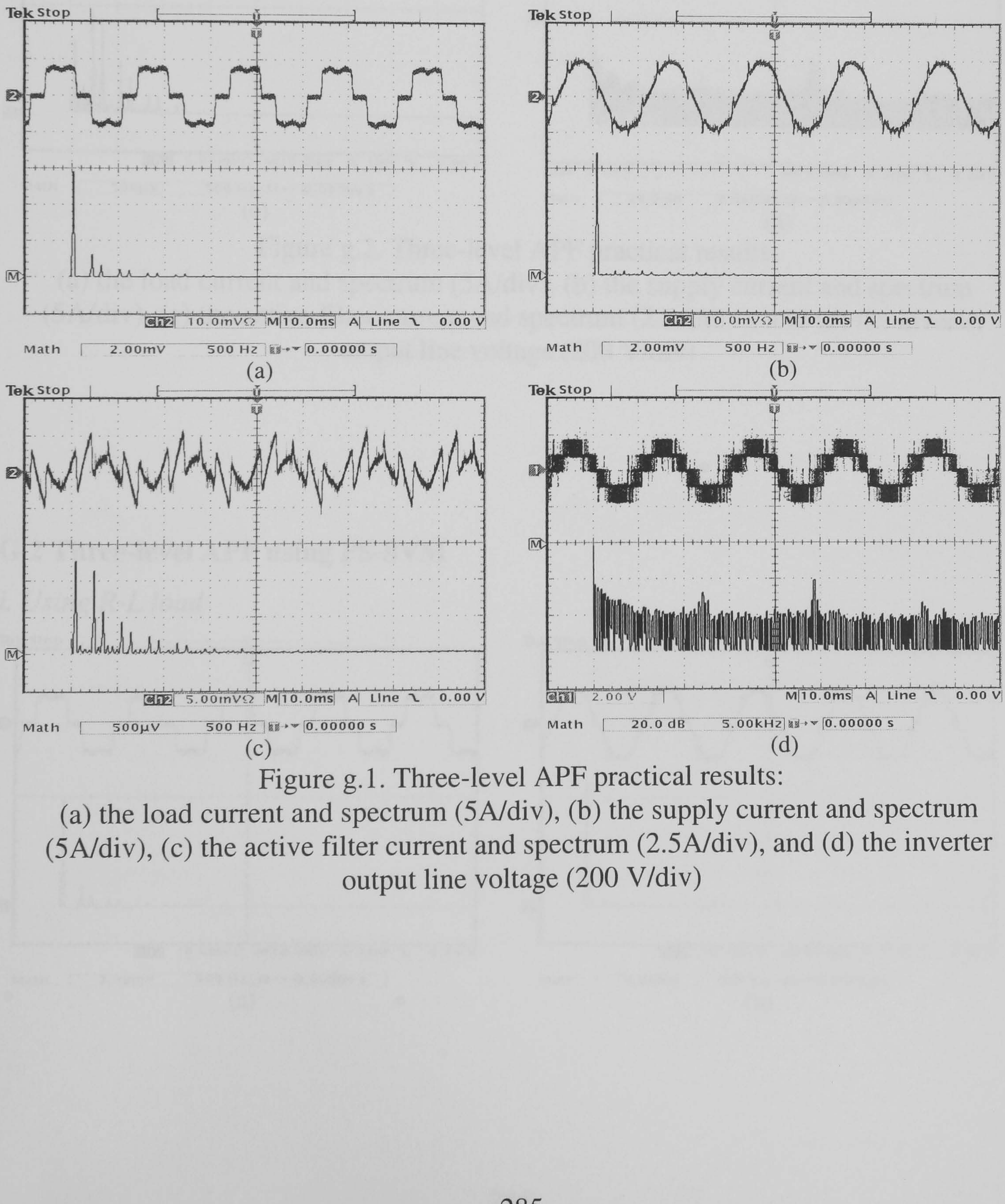


Figure g.1. Three-level APF practical results:
(a) the load current and spectrum (5A/div), (b) the supply current and spectrum (5A/div), (c) the active filter current and spectrum (2.5A/div), and (d) the inverter output line voltage (200 V/div)

ii. Using R-C load

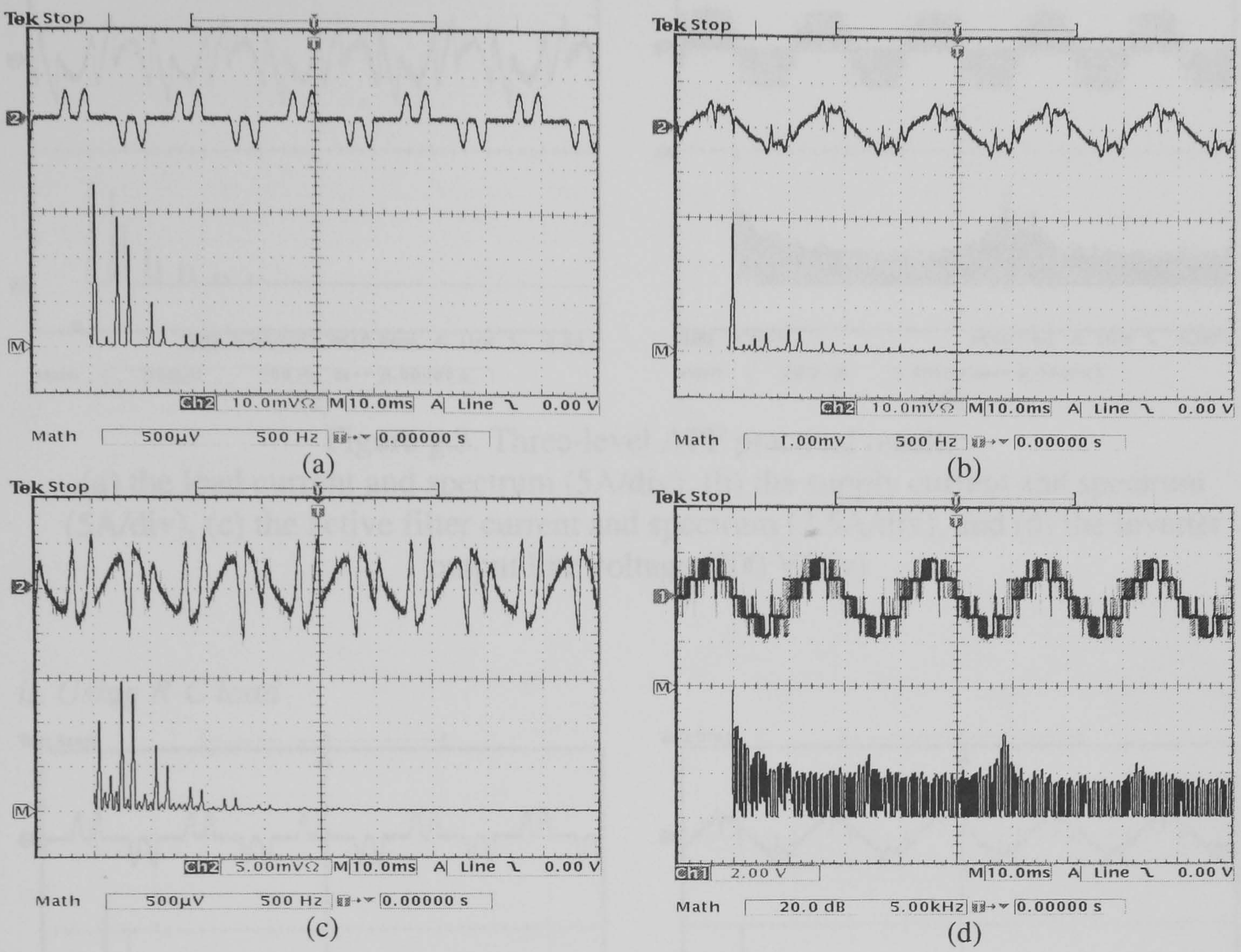
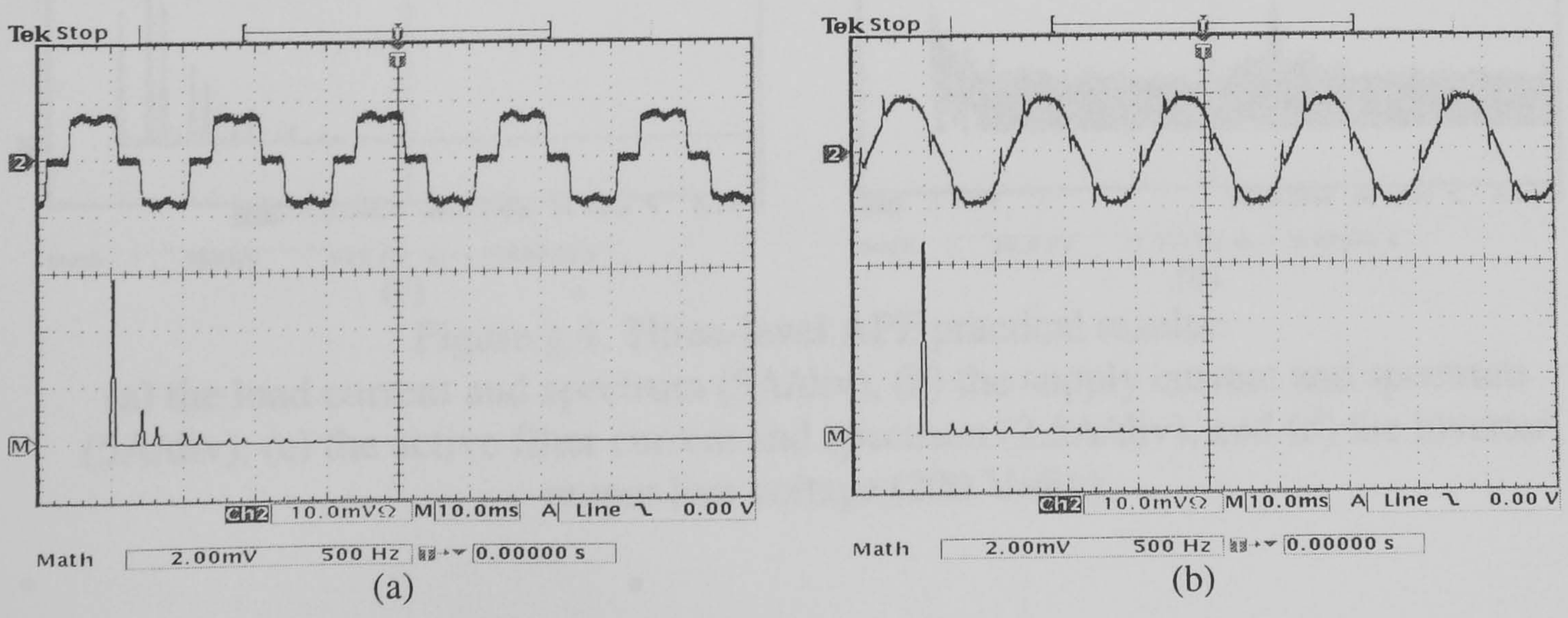


Figure g.2. Three-level APF practical results:
(a) the load current and spectrum (5A/div), (b) the supply current and spectrum (5A/div), (c) the active filter current and spectrum (2.5A/div), and (d) the inverter output line voltage (200 V/div)

G.2 Three-level APF using PS-SVM

i. Using R-L load



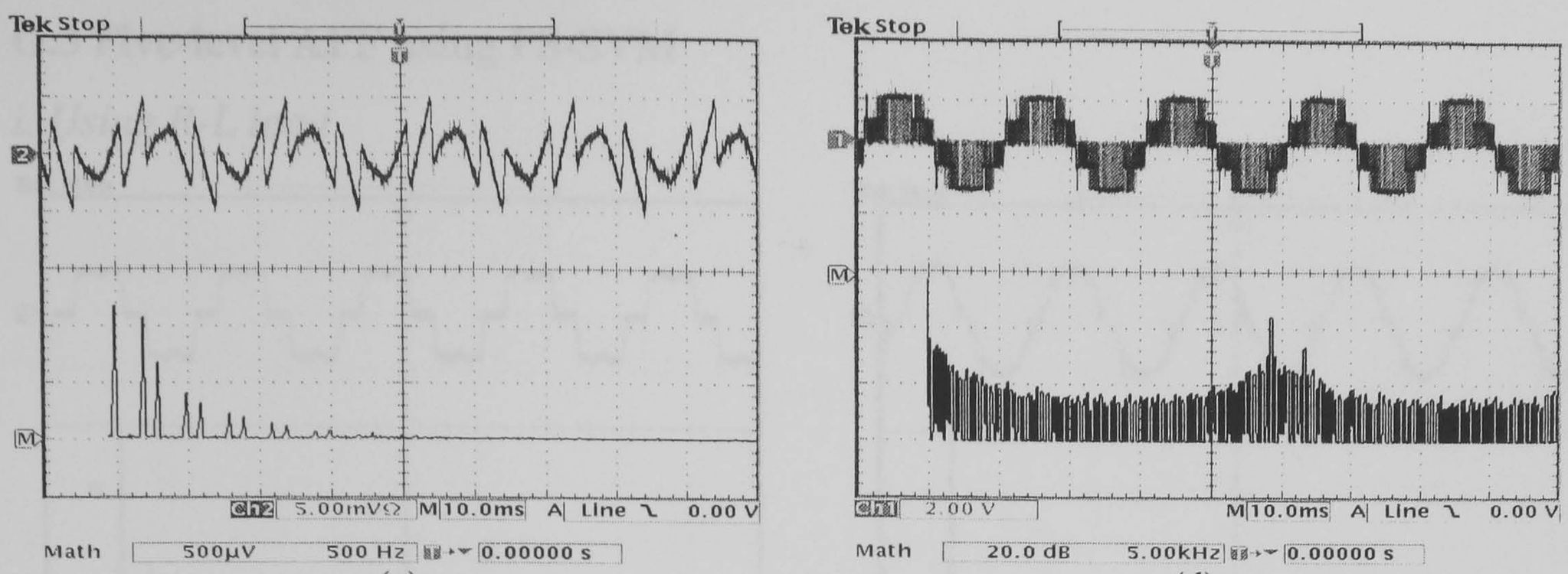


Figure g.3. Three-level APF practical results:
(a) the load current and spectrum (5A/div), (b) the supply current and spectrum (5A/div), (c) the active filter current and spectrum (2.5A/div), and (d) the inverter output line voltage (200 V/div)

ii. Using R-C load

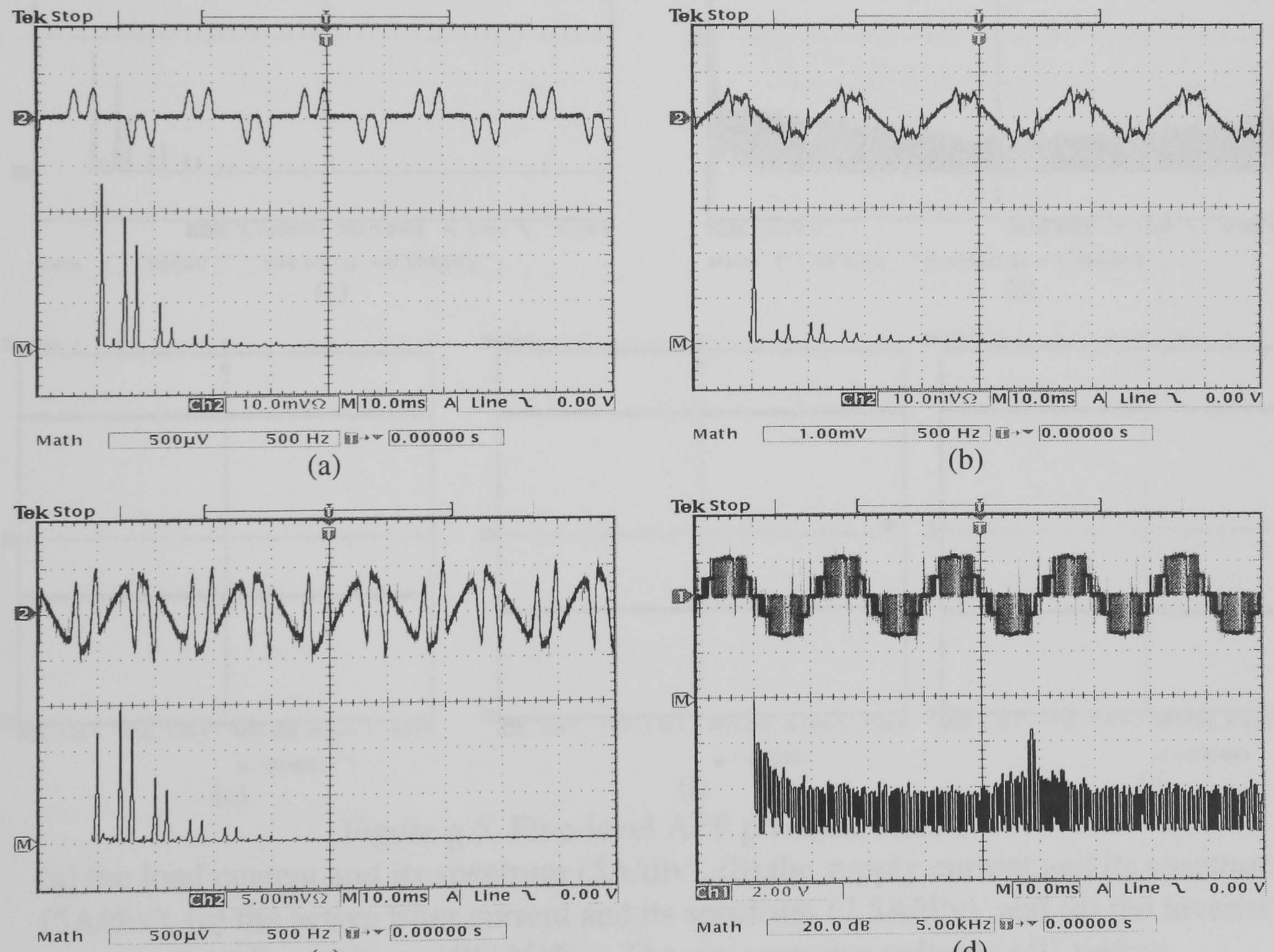


Figure g.4. Three-level APF practical results:
(a) the load current and spectrum (5A/div), (b) the supply current and spectrum (5A/div), (c) the active filter current and spectrum (2.5A/div), and (d) the inverter output line voltage (200 V/div)

G.3 Five-level APF using PS-SVM

i. Using R-L load

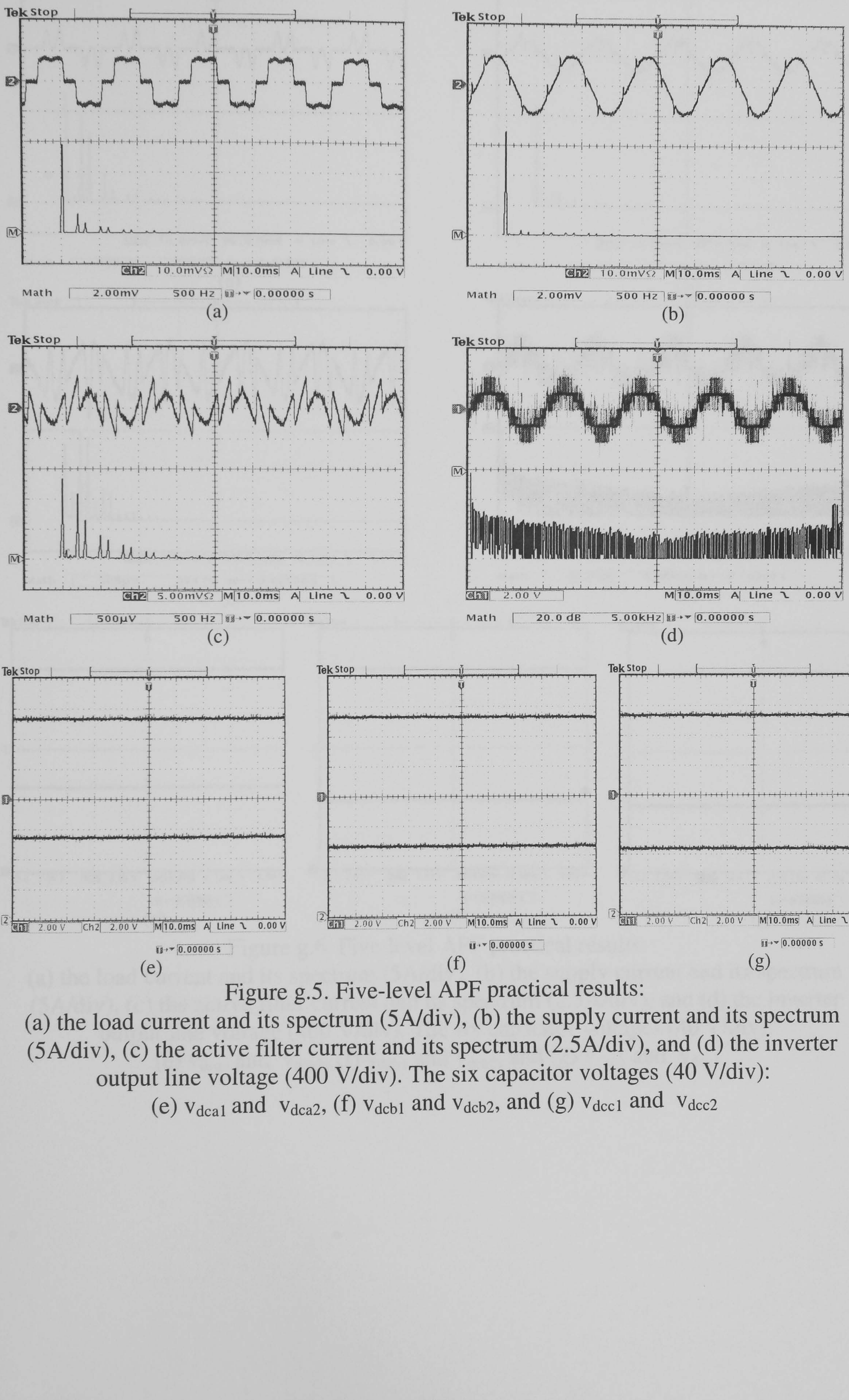
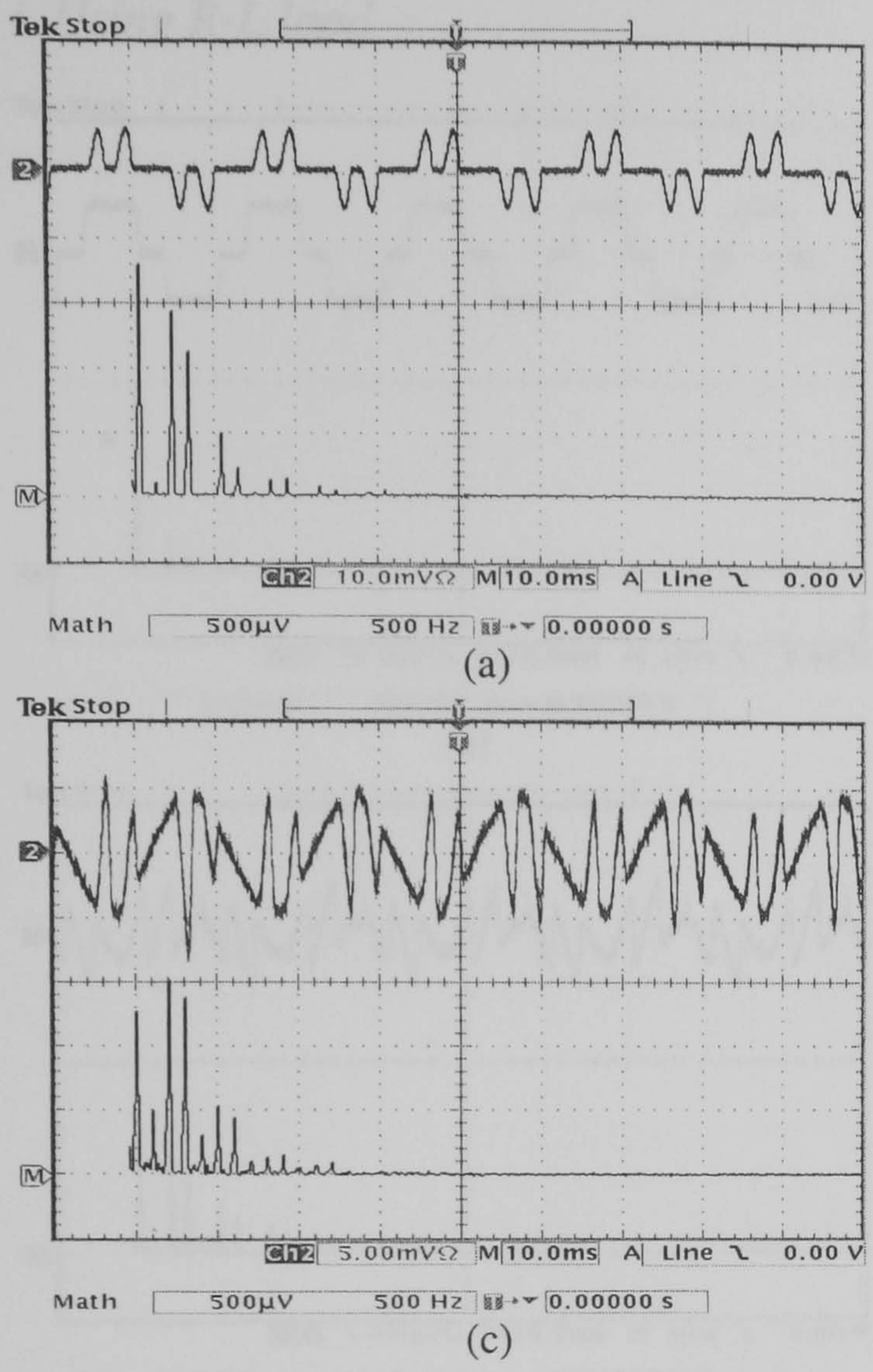


Figure g.5. Five-level APF practical results:
(a) the load current and its spectrum (5A/div), (b) the supply current and its spectrum (5A/div), (c) the active filter current and its spectrum (2.5A/div), and (d) the inverter output line voltage (400 V/div). The six capacitor voltages (40 V/div):
(e) v_{dca1} and v_{dca2}, (f) v_{dcb1} and v_{dcb2}, and (g) v_{dcc1} and v_{dcc2}

ii. Using R-C load



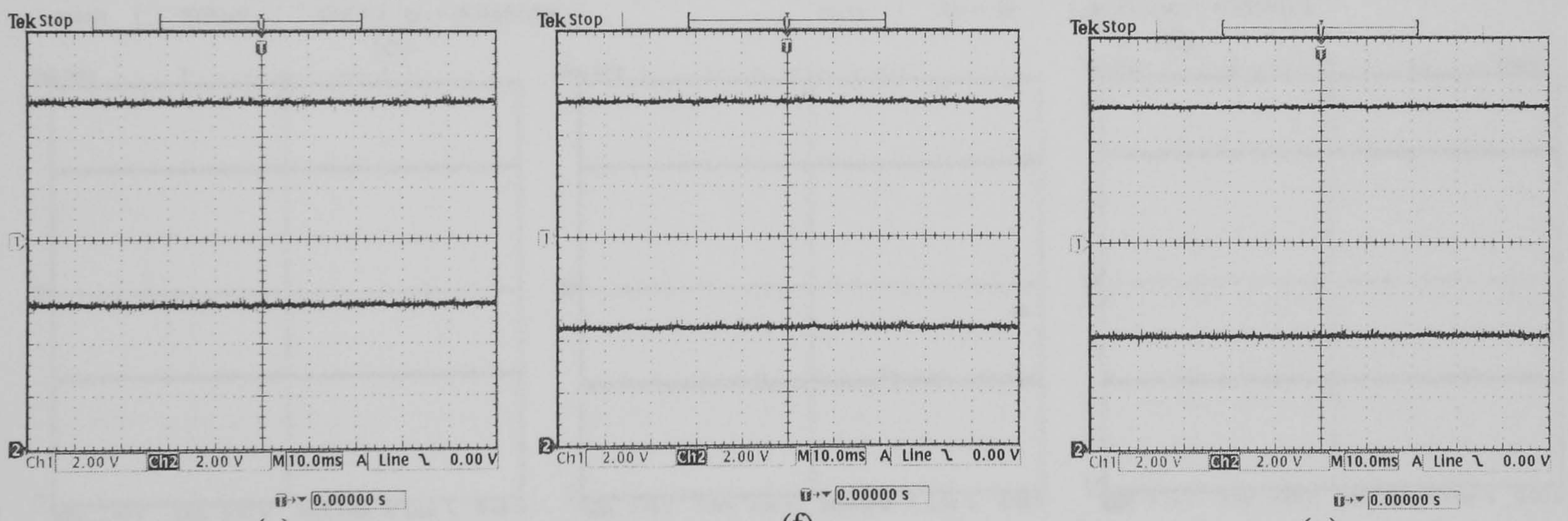


Figure g.6. Five-level APF practical results:
(a) the load current and its spectrum (5A/div), (b) the supply current and its spectrum (5A/div), (c) the active filter current and its spectrum (2.5A/div), and (d) the inverter output line voltage (400 V/div). The six capacitor voltages (40 V/div):
(e) v_{dca1} and v_{dca2}, (f) v_{dcb1} and v_{dcb2}, and (g) v_{dcc1} and v_{dcc2}

G.4 Five-level APF using H-SVM

i. Using R-L load

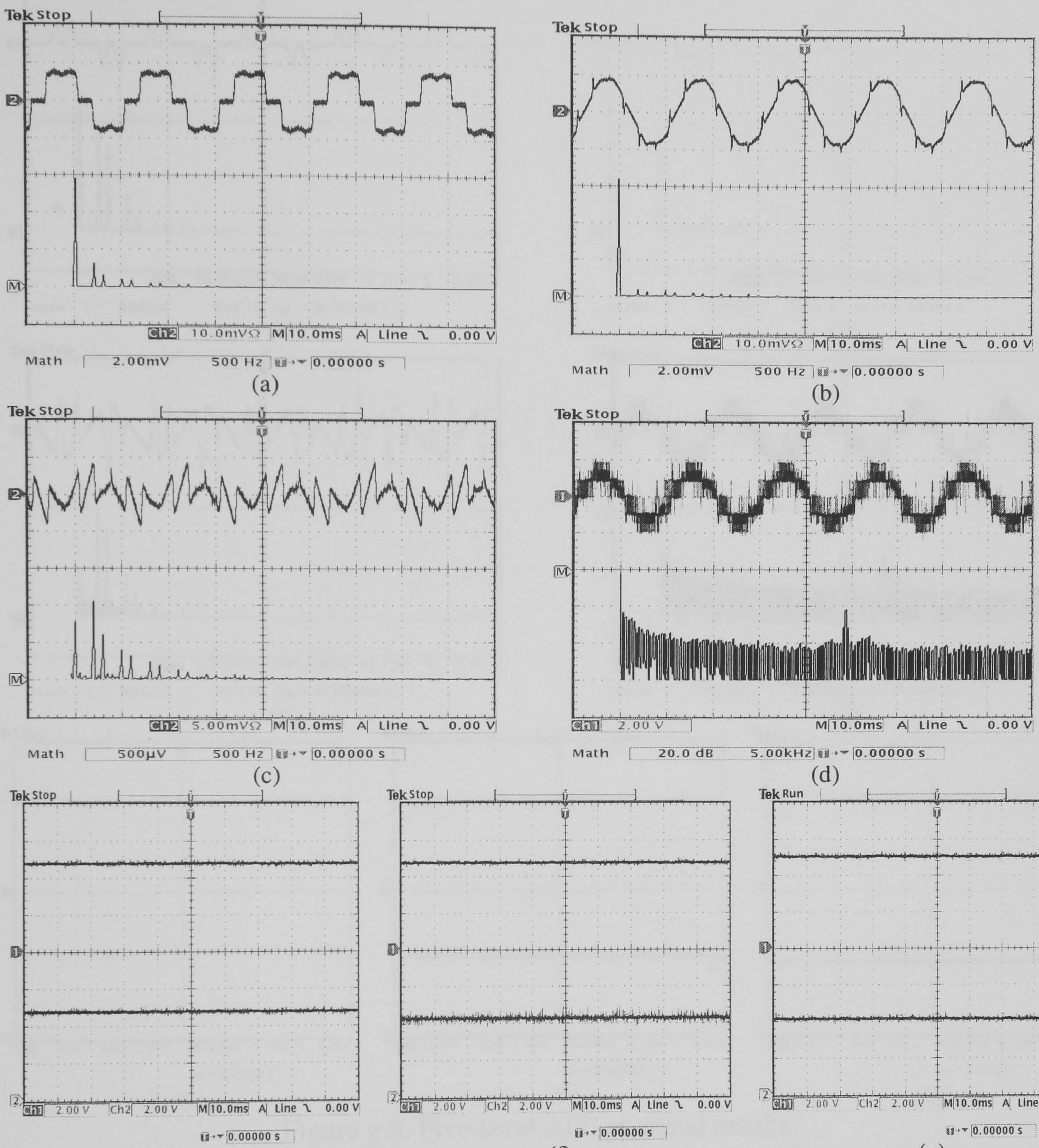


Figure g.7. Five-level APF practical results:
(a) the load current and its spectrum (5A/div), (b) the supply current and its spectrum (5A/div), (c) the active filter current and its spectrum (2.5A/div), and (d) the inverter output line voltage (400 V/div). The six capacitor voltages (40 V/div):
(e) v_{dca1} and v_{dca2}, (f) v_{dcb1} and v_{dcb2}, and (g) v_{dcc1} and v_{dcc2}

ii. Using R-C load

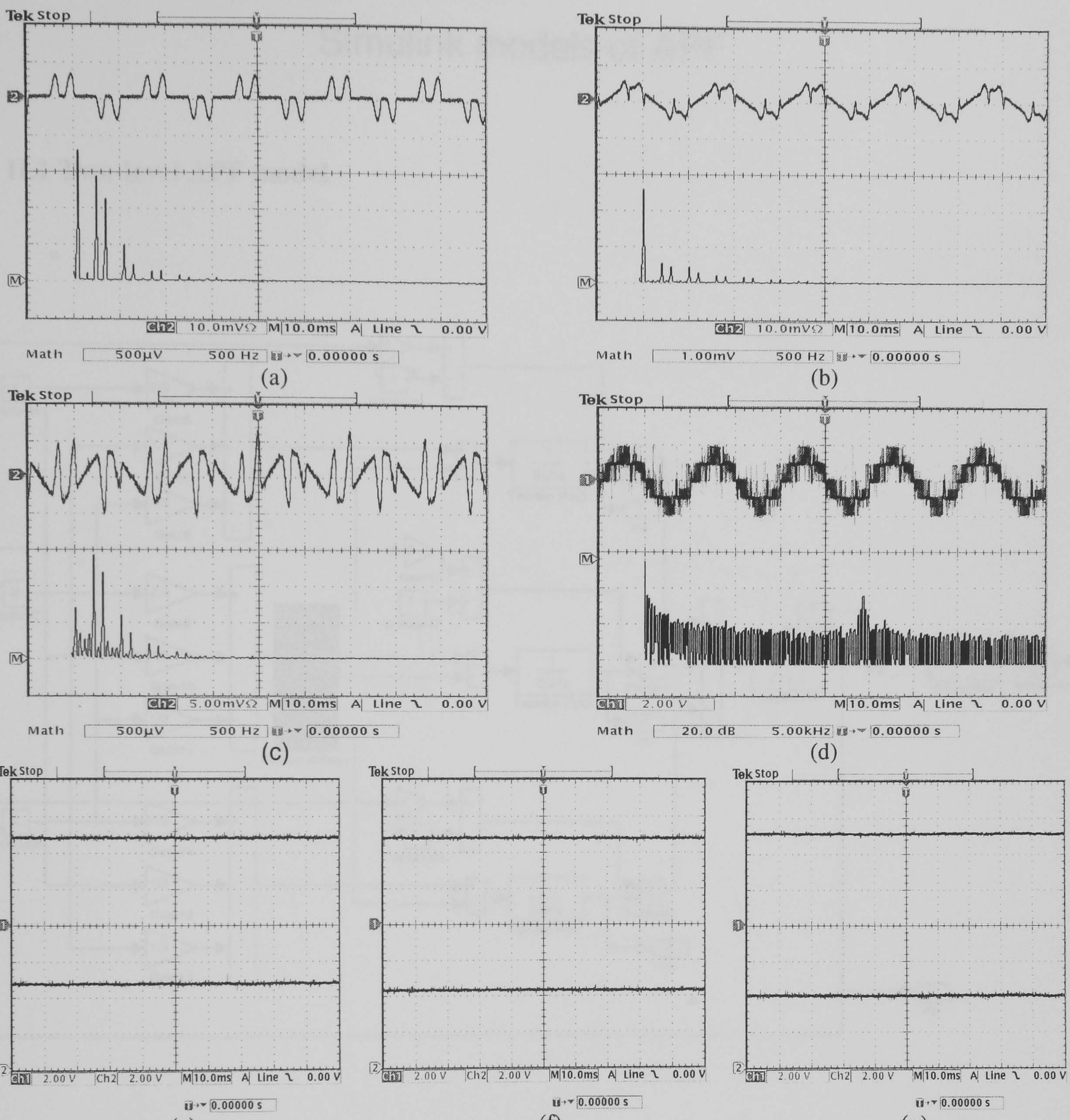
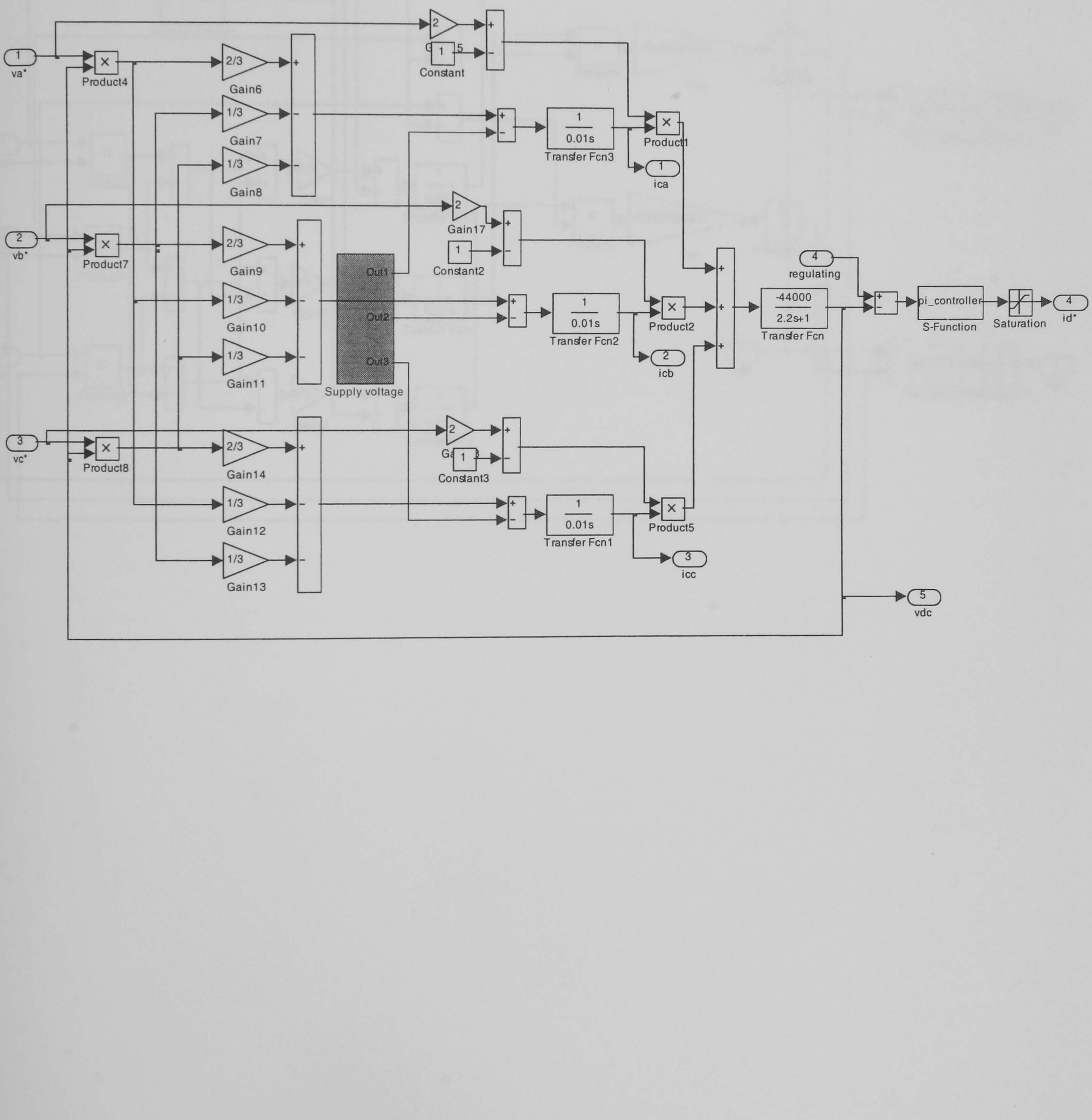


Figure g.8. Five-level APF practical results:
(a) the load current and its spectrum (5A/div), (b) the supply current and its spectrum (5A/div), (c) the active filter current and its spectrum (2.5A/div), and (d) the inverter output line voltage (400 V/div). The six capacitor voltages (40 V/div):
(e) v_{dca1} and v_{dca2}, (f) v_{dcb1} and v_{dcb2}, and (g) v_{dcc1} and v_{dcc2}

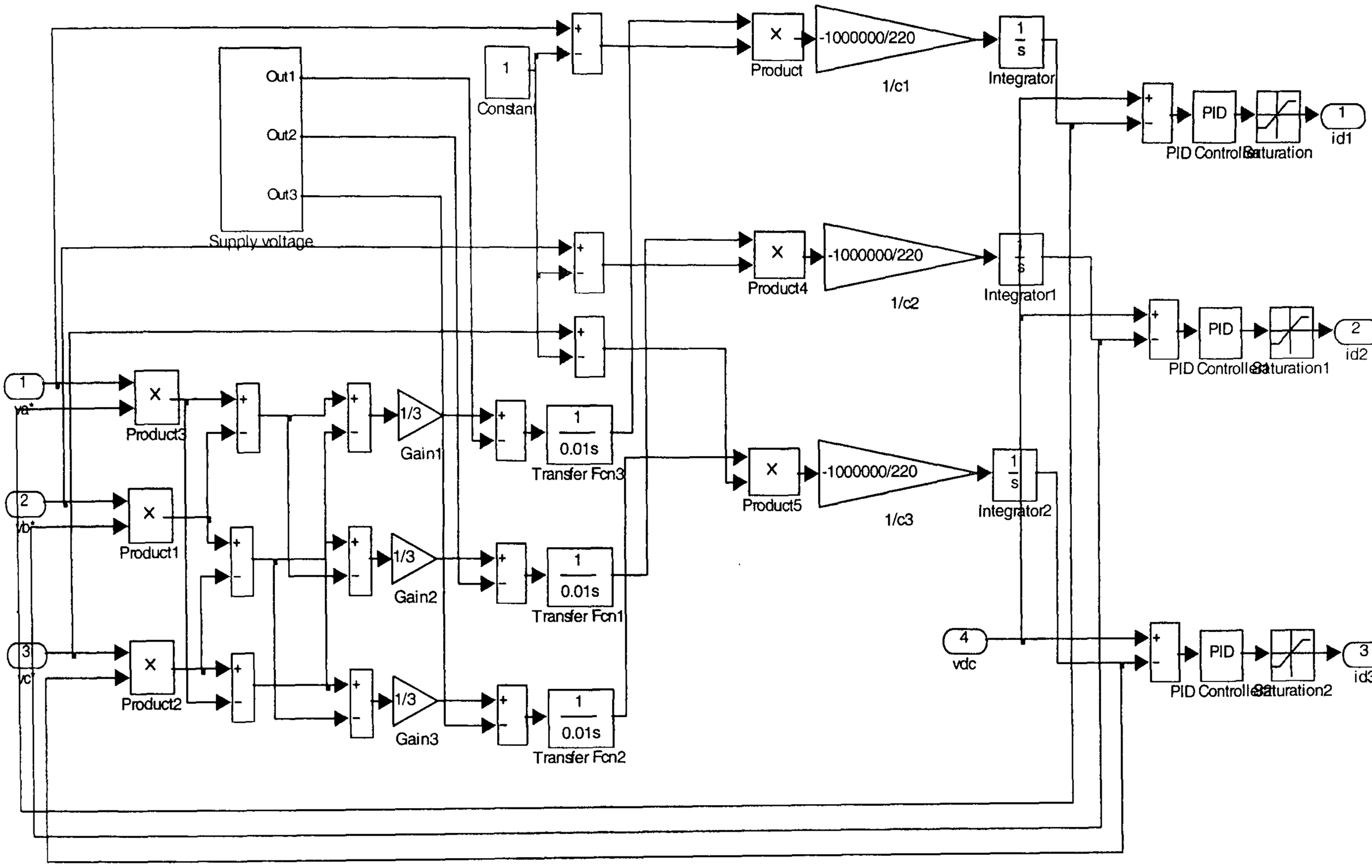
Appendix H

Simulink models of APF

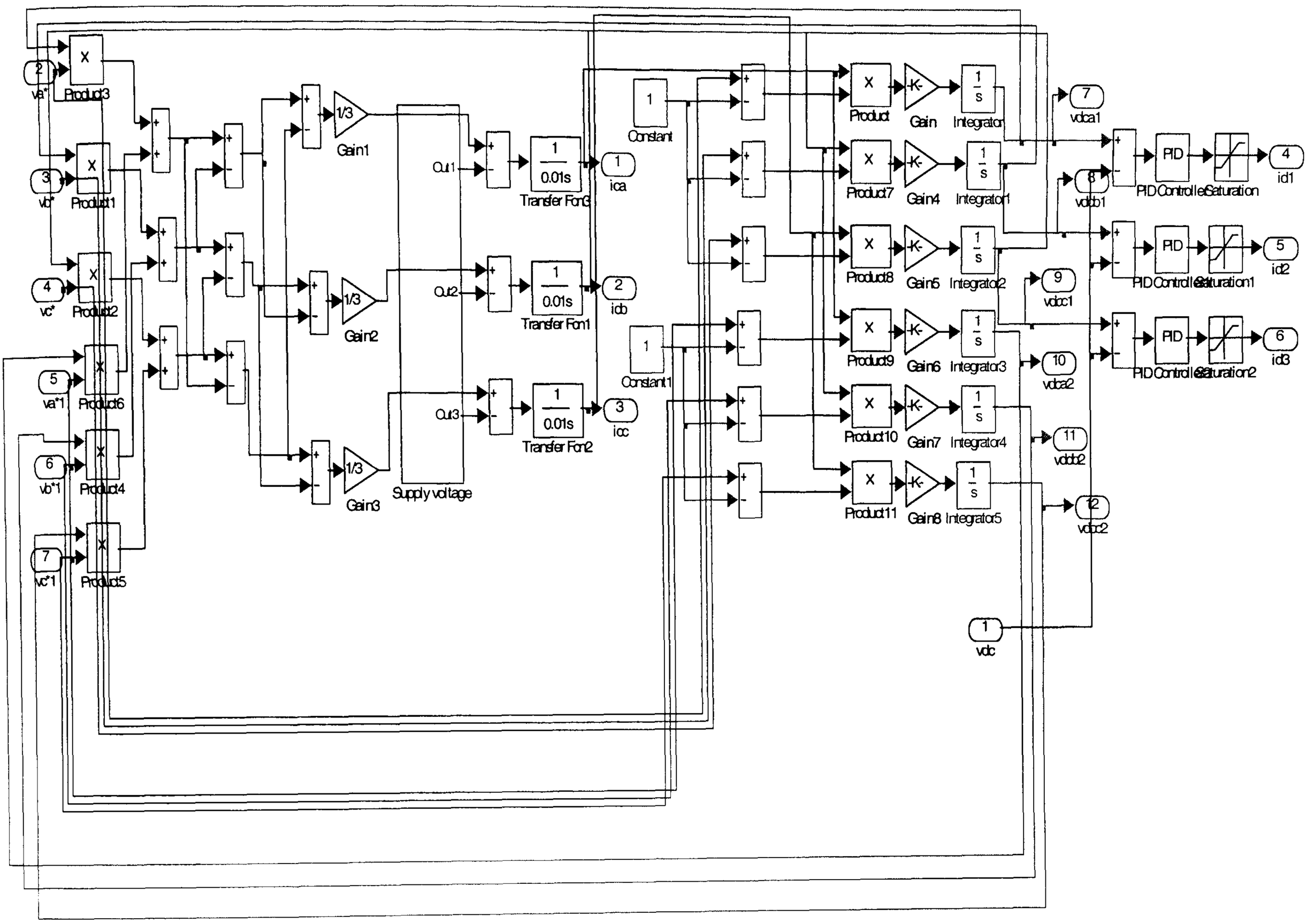
H.1 Two-level APF model



H.2 Three-level APF model



H.3 Five-level APF model



Appendix I

Numerical analysis example of state selection proof

In this appendix, a numerical analysis example of the state selection proof is given. In the five-level SVM, the states can be derived from the states matrix presented in chapter five as follows:

$$zero\_states\_vector = [000 \quad 111 \quad 222 \quad 333 \quad 444]$$
$$= [X(1,1,1) \quad X(1,1,2) \quad X(1,1,3) \quad X(1,1,4) \quad X(1,1,5)]$$

$$hexagon\_1\_matrix = \begin{bmatrix} 100 & 211 & 322 & 433 \\ 110 & 221 & 332 & 443 \\ 010 & 121 & 232 & 343 \\ 011 & 122 & 233 & 344 \\ 001 & 112 & 223 & 334 \\ 101 & 212 & 323 & 434 \end{bmatrix} = \begin{bmatrix} X(2,1,1) & X(2,1,2) & X(2,1,3) & X(2,1,4) \\ X(2,2,1) & X(2,2,2) & X(2,2,3) & X(2,2,4) \\ X(2,3,1) & X(2,3,2) & X(2,3,3) & X(2,3,4) \\ X(2,4,1) & X(2,4,2) & X(2,4,3) & X(2,4,4) \\ X(2,5,1) & X(2,5,2) & X(2,5,3) & X(2,5,4) \\ X(2,6,1) & X(2,6,2) & X(2,6,3) & X(2,6,4) \end{bmatrix}$$

$$hexagon\_2\_matrix = \begin{bmatrix} 200 & 311 & 422 \\ 210 & 321 & 432 \\ 220 & 331 & 442 \\ 120 & 231 & 342 \\ 020 & 131 & 242 \\ 021 & 132 & 243 \\ 022 & 133 & 244 \\ 012 & 123 & 234 \\ 002 & 113 & 224 \\ 102 & 213 & 324 \\ 202 & 313 & 424 \\ 201 & 312 & 423 \end{bmatrix} = \begin{bmatrix} X(3,1,1) & X(3,1,2) & X(3,1,3) \\ X(3,2,1) & X(3,2,2) & X(3,2,3) \\ X(3,3,1) & X(3,3,2) & X(3,3,3) \\ X(3,4,1) & X(3,4,2) & X(3,4,3) \\ X(3,5,1) & X(3,5,2) & X(3,5,3) \\ X(3,6,1) & X(3,6,2) & X(3,6,3) \\ X(3,7,1) & X(3,7,2) & X(3,7,2) \\ X(3,8,1) & X(3,8,2) & X(3,8,3) \\ X(3,9,1) & X(3,9,2) & X(3,9,3) \\ X(3,10,1) & X(3,10,2) & X(3,10,3) \\ X(3,11,1) & X(3,11,2) & X(3,11,3) \\ X(3,12,1) & X(3,12,2) & X(3,12,3) \end{bmatrix}$$

$$hexagon\_3\_matrix = \begin{bmatrix} 300 & 411 \\ 310 & 421 \\ 320 & 431 \\ 330 & 441 \\ 230 & 341 \\ 130 & 241 \\ 030 & 141 \\ 031 & 142 \\ 032 & 143 \\ 033 & 144 \\ 023 & 134 \\ 013 & 124 \\ 003 & 114 \\ 103 & 214 \\ 203 & 314 \\ 303 & 414 \\ 302 & 413 \\ 301 & 412 \end{bmatrix} = \begin{bmatrix} X(4,1,1) & X(4,1,2) \\ X(4,2,1) & X(4,2,2) \\ X(4,3,1) & X(4,3,2) \\ X(4,4,1) & X(4,4,2) \\ X(4,5,1) & X(4,5,2) \\ X(4,6,1) & X(4,6,2) \\ X(4,7,1) & X(4,7,2) \\ X(4,8,1) & X(4,8,2) \\ X(4,9,1) & X(4,9,2) \\ X(4,10,1) & X(4,10,2) \\ X(4,11,1) & X(4,11,2) \\ X(4,12,1) & X(4,12,2) \\ X(4,13,1) & X(4,13,2) \\ X(4,14,1) & X(4,14,2) \\ X(4,15,1) & X(4,15,2) \\ X(4,16,1) & X(4,16,2) \\ X(4,17,1) & X(4,17,2) \\ X(4,18,1) & X(4,18,2) \end{bmatrix}$$

$$hexagon\_3\_matrix = \begin{bmatrix} 400 \\ 410 \\ 420 \\ 430 \\ 440 \\ 340 \\ 240 \\ 140 \\ 040 \\ 041 \\ 042 \\ 043 \\ 044 \\ 034 \\ 024 \\ 014 \\ 004 \\ 104 \\ 204 \\ 304 \\ 404 \\ 403 \\ 402 \\ 401 \end{bmatrix} = \begin{bmatrix} X(5,1,1) \\ X(5,2,1) \\ X(5,3,1) \\ X(5,4,1) \\ X(5,5,1) \\ X(5,6,1) \\ X(5,7,1) \\ X(5,8,1) \\ X(5,9,1) \\ X(5,10,1) \\ X(5,11,1) \\ X(5,12,1) \\ X(5,13,1) \\ X(5,14,1) \\ X(5,15,1) \\ X(5,16,1) \\ X(5,17,1) \\ X(5,18,1) \\ X(5,19,1) \\ X(5,20,1) \\ X(5,21,1) \\ X(5,22,1) \\ X(5,23,1) \\ X(5,24,1) \end{bmatrix}$$

Using the previous states, the state sequences rotation for the five-level SVM can be defined as:

i. Region 1

$$\begin{aligned}
sector_1 &= [X(1,1,1) \rightarrow \quad X(2,1,1) \rightarrow \quad X(2,2,1) \rightarrow \quad X(1,1,2)] \\
&= [X(1,1,2) \rightarrow \quad X(2,1,2) \rightarrow \quad X(2,2,2) \rightarrow \quad X(1,1,3)] \\
&= [X(1,1,3) \rightarrow \quad X(2,1,3) \rightarrow \quad X(2,2,3) \rightarrow \quad X(1,1,4)] \\
&= [X(1,1,4) \rightarrow \quad X(2,1,4) \rightarrow \quad X(2,2,4) \rightarrow \quad X(1,1,5)]
\end{aligned}$$

$$\begin{aligned}
sector_2 &= [X(1,1,1) \rightarrow \quad X(2,3,1) \rightarrow \quad X(2,2,1) \rightarrow \quad X(1,1,2)] \\
&= [X(1,1,2) \rightarrow \quad X(2,3,2) \rightarrow \quad X(2,2,2) \rightarrow \quad X(1,1,3)] \\
&= [X(1,1,3) \rightarrow \quad X(2,3,3) \rightarrow \quad X(2,2,3) \rightarrow \quad X(1,1,4)] \\
&= [X(1,1,4) \rightarrow \quad X(2,3,4) \rightarrow \quad X(2,2,4) \rightarrow \quad X(1,1,5)]
\end{aligned}$$

$$\begin{aligned}
sector_3 &= [X(1,1,1) \rightarrow \quad X(2,3,1) \rightarrow \quad X(2,4,1) \rightarrow \quad X(1,1,2)] \\
&= [X(1,1,2) \rightarrow \quad X(2,3,2) \rightarrow \quad X(2,4,2) \rightarrow \quad X(1,1,3)] \\
&= [X(1,1,3) \rightarrow \quad X(2,3,3) \rightarrow \quad X(2,4,3) \rightarrow \quad X(1,1,4)] \\
&= [X(1,1,4) \rightarrow \quad X(2,3,4) \rightarrow \quad X(2,4,4) \rightarrow \quad X(1,1,5)]
\end{aligned}$$

$$\begin{aligned}
sector_4 &= [X(1,1,1) \rightarrow \quad X(2,5,1) \rightarrow \quad X(2,4,1) \rightarrow \quad X(1,1,2)] \\
&= [X(1,1,2) \rightarrow \quad X(2,5,2) \rightarrow \quad X(2,4,2) \rightarrow \quad X(1,1,3)] \\
&= [X(1,1,3) \rightarrow \quad X(2,5,3) \rightarrow \quad X(2,4,3) \rightarrow \quad X(1,1,4)] \\
&= [X(1,1,4) \rightarrow \quad X(2,5,4) \rightarrow \quad X(2,4,4) \rightarrow \quad X(1,1,5)]
\end{aligned}$$

$$\begin{aligned}
sector_5 &= [X(1,1,1) \rightarrow \quad X(2,5,1) \rightarrow \quad X(2,6,1) \rightarrow \quad X(1,1,2)] \\
&= [X(1,1,2) \rightarrow \quad X(2,5,2) \rightarrow \quad X(2,6,2) \rightarrow \quad X(1,1,3)] \\
&= [X(1,1,3) \rightarrow \quad X(2,5,3) \rightarrow \quad X(2,6,3) \rightarrow \quad X(1,1,4)] \\
&= [X(1,1,4) \rightarrow \quad X(2,5,4) \rightarrow \quad X(2,6,4) \rightarrow \quad X(1,1,5)]
\end{aligned}$$

$$\begin{aligned}
sector_6 &= [X(1,1,1) \rightarrow \quad X(2,1,1) \rightarrow \quad X(2,6,1) \rightarrow \quad X(1,1,2)] \\
&= [X(1,1,2) \rightarrow \quad X(2,1,2) \rightarrow \quad X(2,6,2) \rightarrow \quad X(1,1,3)] \\
&= [X(1,1,3) \rightarrow \quad X(2,1,3) \rightarrow \quad X(2,6,3) \rightarrow \quad X(1,1,4)] \\
&= [X(1,1,4) \rightarrow \quad X(2,1,4) \rightarrow \quad X(2,6,4) \rightarrow \quad X(1,1,5)]
\end{aligned}$$

ii. Region 2

$$\begin{aligned}
sector_1 &= [X(2,1,1) \rightarrow \quad X(3,1,1) \rightarrow \quad X(3,2,1) \rightarrow \quad X(2,1,2)] \\
&= [X(2,1,2) \rightarrow \quad X(3,1,2) \rightarrow \quad X(3,2,2) \rightarrow \quad X(2,1,3)] \\
&= [X(2,1,3) \rightarrow \quad X(3,1,3) \rightarrow \quad X(3,2,3) \rightarrow \quad X(2,1,4)]
\end{aligned}$$

$$\begin{aligned}
sector_2 &= [X(2,2,1) \rightarrow \quad X(3,4,1) \rightarrow \quad X(3,3,1) \rightarrow \quad X(2,2,2)] \\
&= [X(2,2,2) \rightarrow \quad X(3,4,2) \rightarrow \quad X(3,3,2) \rightarrow \quad X(2,2,3)] \\
&= [X(2,2,3) \rightarrow \quad X(3,4,3) \rightarrow \quad X(3,3,3) \rightarrow \quad X(2,2,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_3 &= [X(2,3,1) \rightarrow \quad X(3,5,1) \rightarrow \quad X(3,6,1) \rightarrow \quad X(2,3,2)] \\
&= [X(2,3,2) \rightarrow \quad X(3,5,2) \rightarrow \quad X(3,6,2) \rightarrow \quad X(2,3,3)] \\
&= [X(2,3,3) \rightarrow \quad X(3,5,3) \rightarrow \quad X(3,6,3) \rightarrow \quad X(2,3,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_4 &= [X(2,4,1) \rightarrow \quad X(3,8,1) \rightarrow \quad X(3,7,1) \rightarrow \quad X(2,4,2)] \\
&= [X(2,4,2) \rightarrow \quad X(3,8,2) \rightarrow \quad X(3,7,2) \rightarrow \quad X(2,4,3)] \\
&= [X(2,4,3) \rightarrow \quad X(3,8,3) \rightarrow \quad X(3,7,3) \rightarrow \quad X(2,4,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_5 &= [X(2,5,1) \rightarrow \quad X(3,9,1) \rightarrow \quad X(3,10,1) \rightarrow \quad X(2,5,2)] \\
&= [X(2,5,2) \rightarrow \quad X(3,9,2) \rightarrow \quad X(3,10,2) \rightarrow \quad X(2,5,3)] \\
&= [X(2,5,3) \rightarrow \quad X(3,9,3) \rightarrow \quad X(3,10,3) \rightarrow \quad X(2,5,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_6 &= [X(2,6,1) \rightarrow \quad X(3,12,1) \rightarrow \quad X(3,11,1) \rightarrow \quad X(2,6,2)] \\
&= [X(2,6,2) \rightarrow \quad X(3,12,2) \rightarrow \quad X(3,11,2) \rightarrow \quad X(2,6,3)] \\
&= [X(2,6,3) \rightarrow \quad X(3,12,3) \rightarrow \quad X(3,11,3) \rightarrow \quad X(2,6,4)]
\end{aligned}$$

iii. Region 3

$$\begin{aligned}
\text{sec}tor_1 &= [X(2,1,1) \rightarrow \quad X(2,2,1) \rightarrow \quad X(3,2,1) \rightarrow \quad X(2,1,2)] \\
&= [X(2,1,2) \rightarrow \quad X(2,2,2) \rightarrow \quad X(3,2,2) \rightarrow \quad X(2,1,3)] \\
&= [X(2,1,3) \rightarrow \quad X(2,2,3) \rightarrow \quad X(3,2,3) \rightarrow \quad X(2,1,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_2 &= [X(2,2,1) \rightarrow \quad X(3,4,1) \rightarrow \quad X(2,3,2) \rightarrow \quad X(2,2,2)] \\
&= [X(2,2,2) \rightarrow \quad X(3,4,2) \rightarrow \quad X(2,3,3) \rightarrow \quad X(2,2,3)] \\
&= [X(2,2,3) \rightarrow \quad X(3,4,3) \rightarrow \quad X(2,3,4) \rightarrow \quad X(2,2,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_3 &= [X(2,3,1) \rightarrow \quad X(2,4,1) \rightarrow \quad X(3,6,2) \rightarrow \quad X(2,3,2)] \\
&= [X(2,3,2) \rightarrow \quad X(2,4,2) \rightarrow \quad X(3,6,3) \rightarrow \quad X(2,3,3)] \\
&= [X(2,3,3) \rightarrow \quad X(2,4,3) \rightarrow \quad X(3,6,4) \rightarrow \quad X(2,3,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_4 &= [X(2,4,1) \rightarrow \quad X(3,8,1) \rightarrow \quad X(2,5,2) \rightarrow \quad X(2,4,2)] \\
&= [X(2,4,2) \rightarrow \quad X(3,8,2) \rightarrow \quad X(2,5,3) \rightarrow \quad X(2,4,3)] \\
&= [X(2,4,3) \rightarrow \quad X(3,8,3) \rightarrow \quad X(2,5,4) \rightarrow \quad X(2,4,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_5 &= [X(2,5,1) \rightarrow \quad X(2,6,1) \rightarrow \quad X(3,10,2) \rightarrow \quad X(2,5,2)] \\
&= [X(2,5,2) \rightarrow \quad X(2,6,2) \rightarrow \quad X(3,10,3) \rightarrow \quad X(2,5,3)] \\
&= [X(2,5,3) \rightarrow \quad X(2,6,3) \rightarrow \quad X(3,10,4) \rightarrow \quad X(2,5,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_6 &= [X(2,6,1) \rightarrow \quad X(3,12,1) \rightarrow \quad X(2,1,2) \rightarrow \quad X(2,6,2)] \\
&= [X(2,6,2) \rightarrow \quad X(3,12,2) \rightarrow \quad X(2,1,3) \rightarrow \quad X(2,6,3)] \\
&= [X(2,6,3) \rightarrow \quad X(3,12,3) \rightarrow \quad X(2,1,4) \rightarrow \quad X(2,6,4)]
\end{aligned}$$

iv. Region 4

$$\begin{aligned}
\text{sec}tor_1 &= [X(2,2,1) \rightarrow \quad X(3,2,1) \rightarrow \quad X(3,3,1) \rightarrow \quad X(2,2,2)] \\
&= [X(2,2,2) \rightarrow \quad X(3,2,2) \rightarrow \quad X(3,3,2) \rightarrow \quad X(2,2,3)] \\
&= [X(2,2,3) \rightarrow \quad X(3,2,3) \rightarrow \quad X(3,3,3) \rightarrow \quad X(2,2,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_2 &= [X(2,3,1) \rightarrow \quad X(3,5,1) \rightarrow \quad X(3,4,1) \rightarrow \quad X(2,3,2)] \\
&= [X(2,3,2) \rightarrow \quad X(3,5,2) \rightarrow \quad X(3,4,2) \rightarrow \quad X(2,3,3)] \\
&= [X(2,3,3) \rightarrow \quad X(3,5,3) \rightarrow \quad X(3,4,3) \rightarrow \quad X(2,3,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_3 &= [X(2,4,1) \rightarrow \quad X(3,6,1) \rightarrow \quad X(3,7,1) \rightarrow \quad X(2,4,2)] \\
&= [X(2,4,2) \rightarrow \quad X(3,6,2) \rightarrow \quad X(3,7,2) \rightarrow \quad X(2,4,3)] \\
&= [X(2,4,3) \rightarrow \quad X(3,6,3) \rightarrow \quad X(3,7,3) \rightarrow \quad X(2,4,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_4 &= [X(2,5,1) \rightarrow \quad X(3,9,1) \rightarrow \quad X(3,8,1) \rightarrow \quad X(2,5,2)] \\
&= [X(2,5,2) \rightarrow \quad X(3,9,2) \rightarrow \quad X(3,8,2) \rightarrow \quad X(2,5,3)] \\
&= [X(2,5,3) \rightarrow \quad X(3,9,3) \rightarrow \quad X(3,8,3) \rightarrow \quad X(2,5,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_5 &= [X(2,6,1) \rightarrow \quad X(3,10,1) \rightarrow \quad X(3,11,1) \rightarrow \quad X(2,6,2)] \\
&= [X(2,6,2) \rightarrow \quad X(3,10,2) \rightarrow \quad X(3,11,2) \rightarrow \quad X(2,6,3)] \\
&= [X(2,6,3) \rightarrow \quad X(3,10,3) \rightarrow \quad X(3,11,3) \rightarrow \quad X(2,6,4)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_6 &= [X(2,1,1) \rightarrow \quad X(3,1,1) \rightarrow \quad X(3,12,1) \rightarrow \quad X(2,1,2)] \\
&= [X(2,1,2) \rightarrow \quad X(3,1,2) \rightarrow \quad X(3,12,2) \rightarrow \quad X(2,1,3)] \\
&= [X(2,1,3) \rightarrow \quad X(3,1,3) \rightarrow \quad X(3,12,3) \rightarrow \quad X(2,1,4)]
\end{aligned}$$

v. Region 5

$$\begin{aligned}
\text{sec}tor_1 &= [X(3,1,1) \rightarrow \quad X(4,1,1) \rightarrow \quad X(4,2,1) \rightarrow \quad X(3,1,2)] \\
&= [X(3,1,2) \rightarrow \quad X(4,1,2) \rightarrow \quad X(4,2,2) \rightarrow \quad X(3,1,3)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_2 &= [X(3,3,1) \rightarrow \quad X(4,5,1) \rightarrow \quad X(4,4,1) \rightarrow \quad X(3,3,2)] \\
&= [X(3,3,2) \rightarrow \quad X(4,5,2) \rightarrow \quad X(4,4,2) \rightarrow \quad X(3,3,3)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_3 &= [X(3,5,1) \rightarrow \quad X(4,7,1) \rightarrow \quad X(4,8,1) \rightarrow \quad X(3,5,2)] \\
&= [X(3,5,2) \rightarrow \quad X(4,7,2) \rightarrow \quad X(4,8,2) \rightarrow \quad X(3,5,3)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_4 &= [X(3,7,1) \rightarrow \quad X(4,11,1) \rightarrow \quad X(4,10,1) \rightarrow \quad X(3,7,2)] \\
&= [X(3,7,2) \rightarrow \quad X(4,11,2) \rightarrow \quad X(4,10,2) \rightarrow \quad X(3,7,3)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_5 &= [X(3,9,1) \rightarrow \quad X(4,13,1) \rightarrow \quad X(4,14,1) \rightarrow \quad X(3,9,2)] \\
&= [X(3,9,2) \rightarrow \quad X(4,13,2) \rightarrow \quad X(4,14,2) \rightarrow \quad X(3,9,3)]
\end{aligned}$$

$$\begin{aligned}
\text{sec}tor_6 &= [X(3,11,1) \rightarrow \quad X(4,17,1) \rightarrow \quad X(4,16,1) \rightarrow \quad X(3,11,2)] \\
&= [X(3,11,2) \rightarrow \quad X(4,17,2) \rightarrow \quad X(4,16,2) \rightarrow \quad X(3,11,3)]
\end{aligned}$$

vi. Region 6

$$\begin{aligned}
sector_1 &= [X(3,1,1) \rightarrow \quad X(3,2,1) \rightarrow \quad X(4,2,1) \rightarrow \quad X(3,1,2)] \\
&= [X(3,1,2) \rightarrow \quad X(3,2,2) \rightarrow \quad X(4,2,2) \rightarrow \quad X(3,1,3)] \\
sector_2 &= [X(3,3,1) \rightarrow \quad X(4,4,1) \rightarrow \quad X(3,4,2) \rightarrow \quad X(3,3,2)] \\
&= [X(3,3,2) \rightarrow \quad X(4,4,2) \rightarrow \quad X(3,4,3) \rightarrow \quad X(3,3,3)] \\
sector_3 &= [X(3,5,1) \rightarrow \quad X(3,6,1) \rightarrow \quad X(4,8,1) \rightarrow \quad X(3,5,2)] \\
&= [X(3,5,2) \rightarrow \quad X(3,6,2) \rightarrow \quad X(4,8,2) \rightarrow \quad X(3,5,3)] \\
sector_4 &= [X(3,7,1) \rightarrow \quad X(4,11,1) \rightarrow \quad X(3,8,2) \rightarrow \quad X(3,7,2)] \\
&= [X(3,7,2) \rightarrow \quad X(4,11,2) \rightarrow \quad X(3,8,3) \rightarrow \quad X(3,7,3)] \\
sector_5 &= [X(3,9,1) \rightarrow \quad X(3,10,1) \rightarrow \quad X(4,14,1) \rightarrow \quad X(3,9,2)] \\
&= [X(3,9,2) \rightarrow \quad X(3,10,2) \rightarrow \quad X(4,14,2) \rightarrow \quad X(3,9,3)] \\
sector_6 &= [X(3,11,1) \rightarrow \quad X(4,17,1) \rightarrow \quad X(3,12,2) \rightarrow \quad X(3,11,2)] \\
&= [X(3,11,2) \rightarrow \quad X(4,17,2) \rightarrow \quad X(3,12,3) \rightarrow \quad X(3,11,3)]
\end{aligned}$$

vii. Region 7

$$\begin{aligned}
sector_1 &= [X(3,2,1) \rightarrow \quad X(4,2,1) \rightarrow \quad X(4,3,1) \rightarrow \quad X(3,2,2)] \\
&= [X(3,2,2) \rightarrow \quad X(4,2,2) \rightarrow \quad X(4,3,2) \rightarrow \quad X(3,2,3)] \\
sector_2 &= [X(3,4,1) \rightarrow \quad X(4,6,1) \rightarrow \quad X(4,5,1) \rightarrow \quad X(3,4,2)] \\
&= [X(3,4,2) \rightarrow \quad X(4,6,2) \rightarrow \quad X(4,5,2) \rightarrow \quad X(3,4,3)] \\
sector_3 &= [X(3,6,1) \rightarrow \quad X(4,8,1) \rightarrow \quad X(4,9,1) \rightarrow \quad X(3,6,2)] \\
&= [X(3,6,2) \rightarrow \quad X(4,8,2) \rightarrow \quad X(4,9,2) \rightarrow \quad X(3,6,3)] \\
sector_4 &= [X(3,7,1) \rightarrow \quad X(4,12,1) \rightarrow \quad X(4,11,1) \rightarrow \quad X(3,8,2)] \\
&= [X(3,7,2) \rightarrow \quad X(4,12,2) \rightarrow \quad X(4,11,2) \rightarrow \quad X(3,8,3)] \\
sector_5 &= [X(3,10,1) \rightarrow \quad X(4,14,1) \rightarrow \quad X(4,15,1) \rightarrow \quad X(3,10,2)] \\
&= [X(3,10,2) \rightarrow \quad X(4,14,2) \rightarrow \quad X(4,15,2) \rightarrow \quad X(3,10,3)] \\
sector_6 &= [X(3,12,1) \rightarrow \quad X(4,18,1) \rightarrow \quad X(4,17,1) \rightarrow \quad X(3,12,2)] \\
&= [X(3,12,2) \rightarrow \quad X(4,18,2) \rightarrow \quad X(4,17,2) \rightarrow \quad X(3,12,3)]
\end{aligned}$$

viii. Region 8

$$\begin{aligned}
sector_1 &= [X(3,2,1) \rightarrow \quad X(3,3,1) \rightarrow \quad X(4,3,1) \rightarrow \quad X(3,2,2)] \\
&= [X(3,2,2) \rightarrow \quad X(3,3,2) \rightarrow \quad X(4,3,2) \rightarrow \quad X(3,2,3)] \\
sector_2 &= [X(3,4,1) \rightarrow \quad X(4,6,1) \rightarrow \quad X(3,5,2) \rightarrow \quad X(3,4,2)] \\
&= [X(3,4,2) \rightarrow \quad X(4,6,2) \rightarrow \quad X(3,5,3) \rightarrow \quad X(3,4,3)] \\
sector_3 &= [X(3,6,1) \rightarrow \quad X(3,7,1) \rightarrow \quad X(4,9,1) \rightarrow \quad X(3,6,2)] \\
&= [X(3,6,2) \rightarrow \quad X(3,7,2) \rightarrow \quad X(4,9,2) \rightarrow \quad X(3,6,3)]
\end{aligned}$$

$$\begin{aligned}
sector_4 &= [X(3,8,1) \rightarrow \quad X(4,12,1) \rightarrow \quad X(3,9,2) \rightarrow \quad X(3,8,2)] \\
&= [X(3,8,2) \rightarrow \quad X(4,12,2) \rightarrow \quad X(3,9,3) \rightarrow \quad X(3,8,3)] \\
sector_5 &= [X(3,10,1) \rightarrow \quad X(3,11,1) \rightarrow \quad X(4,15,1) \rightarrow \quad X(3,10,2)] \\
&= [X(3,10,2) \rightarrow \quad X(3,11,2) \rightarrow \quad X(4,15,2) \rightarrow \quad X(3,10,3)] \\
sector_6 &= [X(3,12,1) \rightarrow \quad X(4,18,1) \rightarrow \quad X(3,1,2) \rightarrow \quad X(3,12,2)] \\
&= [X(3,12,2) \rightarrow \quad X(4,18,2) \rightarrow \quad X(3,1,3) \rightarrow \quad X(3,12,3)]
\end{aligned}$$

ix. Region 9

$$\begin{aligned}
sector_1 &= [X(3,3,1) \rightarrow \quad X(4,3,1) \rightarrow \quad X(4,4,1) \rightarrow \quad X(3,3,2)] \\
&= [X(3,3,2) \rightarrow \quad X(4,3,2) \rightarrow \quad X(4,4,2) \rightarrow \quad X(3,3,3)] \\
sector_2 &= [X(3,5,1) \rightarrow \quad X(4,7,1) \rightarrow \quad X(4,6,2) \rightarrow \quad X(3,5,2)] \\
&= [X(3,5,2) \rightarrow \quad X(4,7,2) \rightarrow \quad X(4,6,3) \rightarrow \quad X(3,5,3)] \\
sector_3 &= [X(3,7,1) \rightarrow \quad X(4,9,1) \rightarrow \quad X(4,10,1) \rightarrow \quad X(3,7,2)] \\
&= [X(3,7,2) \rightarrow \quad X(4,9,2) \rightarrow \quad X(4,10,2) \rightarrow \quad X(3,7,3)] \\
sector_4 &= [X(3,9,1) \rightarrow \quad X(4,13,1) \rightarrow \quad X(4,12,2) \rightarrow \quad X(3,9,2)] \\
&= [X(3,9,2) \rightarrow \quad X(4,13,2) \rightarrow \quad X(4,12,3) \rightarrow \quad X(3,9,3)] \\
sector_5 &= [X(3,11,1) \rightarrow \quad X(4,15,1) \rightarrow \quad X(4,16,1) \rightarrow \quad X(3,11,2)] \\
&= [X(3,11,2) \rightarrow \quad X(4,15,2) \rightarrow \quad X(4,16,2) \rightarrow \quad X(3,11,3)] \\
sector_6 &= [X(3,1,1) \rightarrow \quad X(4,1,1) \rightarrow \quad X(4,18,2) \rightarrow \quad X(3,1,2)] \\
&= [X(3,1,2) \rightarrow \quad X(4,1,2) \rightarrow \quad X(4,18,3) \rightarrow \quad X(3,1,3)]
\end{aligned}$$

Summarizing the previous sequences in the table below and using numerical analysis, the general equations for state sequences in chapter five can be derived for the twelve variable (g1 to g12) of the states matrix.

Table i.1. Numerical representation for the state sequences in the five-level SVM

		X(g1,g2,g3)			*X(g4,g5,g6)*			*X(g7,g8,g9)*			*X(g10,g11,g12)*		
sector	*reg*	*g1*	*g2*	*g3*	*g4*	*g5*	*g6*	*g7*	*g8*	*g9*	*g10*	*g11*	*g12*
Hexagon 1													
1	*1*	*1*	*1*	Range from *1* to *m-1*	*2*	*1*	Range from *1* to *m-1*	*2*	*2*	Range from *1* to *m-1*	*1*	*2*	Range from *2* to *m*
2		*1*	*1*		*2*	*3*		*2*	*2*		*1*	*2*	
3		*1*	*1*		*2*	*3*		*2*	*4*		*1*	*2*	
4		*1*	*1*		*2*	*5*		*2*	*4*		*1*	*2*	
5		*1*	*1*		*2*	*5*		*2*	*6*		*1*	*2*	
6		*1*	*1*		*2*	*1*		*2*	*6*		*1*	*2*	
Hexagon 2													
1	*2*	*2*	*1*		*3*	*1*		*3*	*2*		*2*	*1*	
	3	*2*	*1*		*2*	*2*		*3*	*2*		*2*	*1*	
	4	*2*	*2*		*3*	*2*		*3*	*3*		*2*	*2*	

Appendix I: Numerical analysis example of state selection proof

				Range from 1 to *m*-2			Range from 2 to *m*-1			Range from 1 to *m*-2			Range from 2 to *m*-1		
2	2	2	2		3	4		3	3		2	2			
	3	2	2		3	4		2	3		2	2			
	4	2	3		3	5		3	4		2	3			
3	2	2	3		3	5		3	6		2	3			
	3	2	3		2	4		3	6		2	3			
	4	2	4		3	6		3	7		2	4			
4	2	2	4		3	8		3	7		2	4			
	3	2	4		3	8		2	5		2	5			
	4	2	5		3	9		3	8		2	5			
5	2	2	5		3	9		3	10		2	5			
	3	2	5		2	6		3	10		2	5			
	4	2	6		3	10		3	11		2	6			
6	2	2	6		3	12		3	11		2	6			
	3	2	6		3	12		2	1		2	6			
	4	2	1		3	1		3	12		2	2			
Hexagon 3															
1	5	3	1		4	1		4	2		3	1			
	6	3	1		3	2		4	2		3	1			
	7	3	2		4	2		4	3		3	2			
	8	3	2		3	3		4	3		3	2			
	9	3	3		4	3		4	4		3	3			
2	5	3	3		4	5		4	4		3	3			
	6	3	3		4	5		3	4		3	3			
	7	3	4		4	6		4	5		3	4			
	8	3	4		4	6		3	5		3	4			
	9	3	5		4	7		4	6		3	5			
3	5	3	5		4	7		4	8		3	5			
	6	3	5		3	6		4	8		3	5			
	7	3	6		4	8		4	9		3	6			
	8	3	6		3	7		4	9		3	6			
	9	3	7		4	9		4	10		3	7			
4	5	3	7		4	11		4	10		3	7			
	6	3	7		4	11		3	8		3	7			
	7	3	8		4	12		4	11		3	8			
	8	3	8		4	12		3	9		3	8			
	9	3	9		4	13		4	12		3	9			
5	5	3	9		4	13		4	14		3	9			
	6	3	9		3	10		4	14		3	9			
	7	3	10		4	14		4	15		3	10			
	8	3	10		3	11		4	15		3	10			
	9	3	11		4	15		4	16		3	11			
6	5	3	11		4	17		4	16		3	11			
	6	3	11		4	17		3	12		3	11			
	7	3	12		4	18		4	17		3	12			
	8	3	12		4	18		3	1		3	12			
	9	3	1		4	1		4	8		3	1			

Appendix J

List of Tables and Figures

List of figures

Chapter 6: New Multilevel SVM techniques

Chapter 9: Three-level Cascaded Shunt Active Power Filter

Chapter 10: The five-level Shunt Active Power Filter

List of tables

Appendix K

Summary of Relevant Published Work by the Author

1] A. M. Massoud, S. J. Finney, and B. W. Williams, 'High-power, high-voltage IGBT applications: series connection of IGBTs or multilevel converters?', International Journal of Electronics, 2003,

Abstract

In this paper a detailed quantitative comparison between two competing high voltage converter technologies is performed, namely series connection of semiconductor power devices versus multilevel converters. The comparison is based on converter losses (conduction and switching), total harmonic distortion, and distortion factor for the output phase and line voltages at different modulation frequency ratios. A new method is presented for conduction loss calculation of cascaded type multilevel converters, which use carrier-based pulse width modulation.

2] A. M. Massoud, S. J. Finney, and B. W. Williams, 'Control Techniques for Multilevel Voltage Source Inverters', IEEE, Conference PESC 2003

Abstract

In this paper different open loop PWM control techniques for multilevel voltage source inverters are investigated and compared. For sinusoidal PWM control, a comparison between different carrier techniques with different modulating signals is performed. This comparison includes total harmonic distortion and distortion factor of the phase and line voltages. A comparison between different modulating signals in sinusoidal PWM (pure sinusoidal, third harmonic injection, and dead band), space vector modulation, and sigma-delta modulation is performed. This comparison includes total harmonic distortion, distortion factor, fundamental, and harmonic r.m.s. of the line voltage.

3] A. M. Massoud, S. J. Finney, and B. W. Williams, 'Multilevel converters and series connection of IGBT evaluation for high power high voltage applications', IEE, PEMD 2004 Conference.

Abstract

In this paper a detailed quantitative comparison between two competing high voltage converter technologies is performed, namely series connection of semiconductor power devices versus multilevel converters. The comparison is based on converter losses (conduction and switching), total harmonic distortion and distortion factor for the output phase and line voltages, and common mode voltage at different modulation frequency ratios.

4] A. M. Massoud, S. J. Finney, and B. W. Williams, 'Conduction loss calculation for multilevel inverter: a generalized approach for carrier based PWM technique', IEE, PEMD 2004 Conference.

Abstract

In this paper, a new method for conduction loss calculation of cascaded type multilevel inverter is proposed. This method can be applied to any carrier-based PWM technique and also can be used for conduction loss calculation of the simple two-level inverter.

5] A. M. Massoud, S. J. Finney, and B. W. Williams, 'Predictive Current Control of a Shunt Active Power Filter', IEEE, Conference PESC 2004

Abstract

In this paper, a predictive current control method for the shunt active power filter is proposed. The active filter output voltage is predicted using the supply current, not the active filter current. Harmonic current extraction is achieved using the capacitor voltage control technique. Space vector modulation (SVM) is used as a pulse width modulation technique. The method improves the current control tracking performance, minimizes the number of sensors, uses SVM to reduce the capacitor voltage consequently the switching loss, and reduces computational burden. The proposed method is validated by simulation and experimentally.

6] A. M. Massoud, S. J. Finney, and B. W. Williams, 'Seven-Level Shunt Active Power Filter', IEEE, Conference ICHQP 2004

Abstract

In this paper, the seven-level cascaded type inverter is used as a shunt active power filter to exploit multilevel inverter advantages. The capacitor voltage control technique used as a harmonic current extraction method for the two-level inverter is extended to the seven-level shunt active power filter. A predictive current controller based on the supply current (not the active filter current) is applied. Phase-shifted space vector modulation for the multilevel inverter is used as a PWM technique. The proposed seven-level shunt active power filter is validated by simulation.

7] A. M. Massoud, S. J. Finney, and B. W. Williams, 'Practical Issues of Three-Phase Three-Wire Active Power Filters Voltage Source Inverter-Based for Medium Voltage Range', IEEE, Conference ICHQP 2004

Abstract

As huge the development in power electronics, active power filters for harmonic mitigation become a broad point of research. Still, the research of active filter application for medium voltage range is going through. This paper presents several practical issues of active power filters generally and for medium voltage range specifically.

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9] A. M. Massoud, S. J. Finney, and B. W. Williams, 'High-bandwidth predictive current controlled, three-phase, five-level cascaded shunt active power filter, using phase-shifted space vector modulation', IEEE, Power Electronics Transactions 2004

Abstract

In this paper, the five-level cascaded inverter is used as a shunt active power filter, which exploits multilevel inverter advantages. The capacitor voltage control technique used previously as a harmonic current extraction method for the two-level inverter, is extended to the five-level shunt active power filter, with a technique proposed for balancing capacitor voltages. Predictive current control based on the supply current (not the active filter current) is applied. Phase-shifted space vector modulation is used for multilevel inverter PWM generation. The proposed five-level shunt active power filter is validated by simulation and practically.

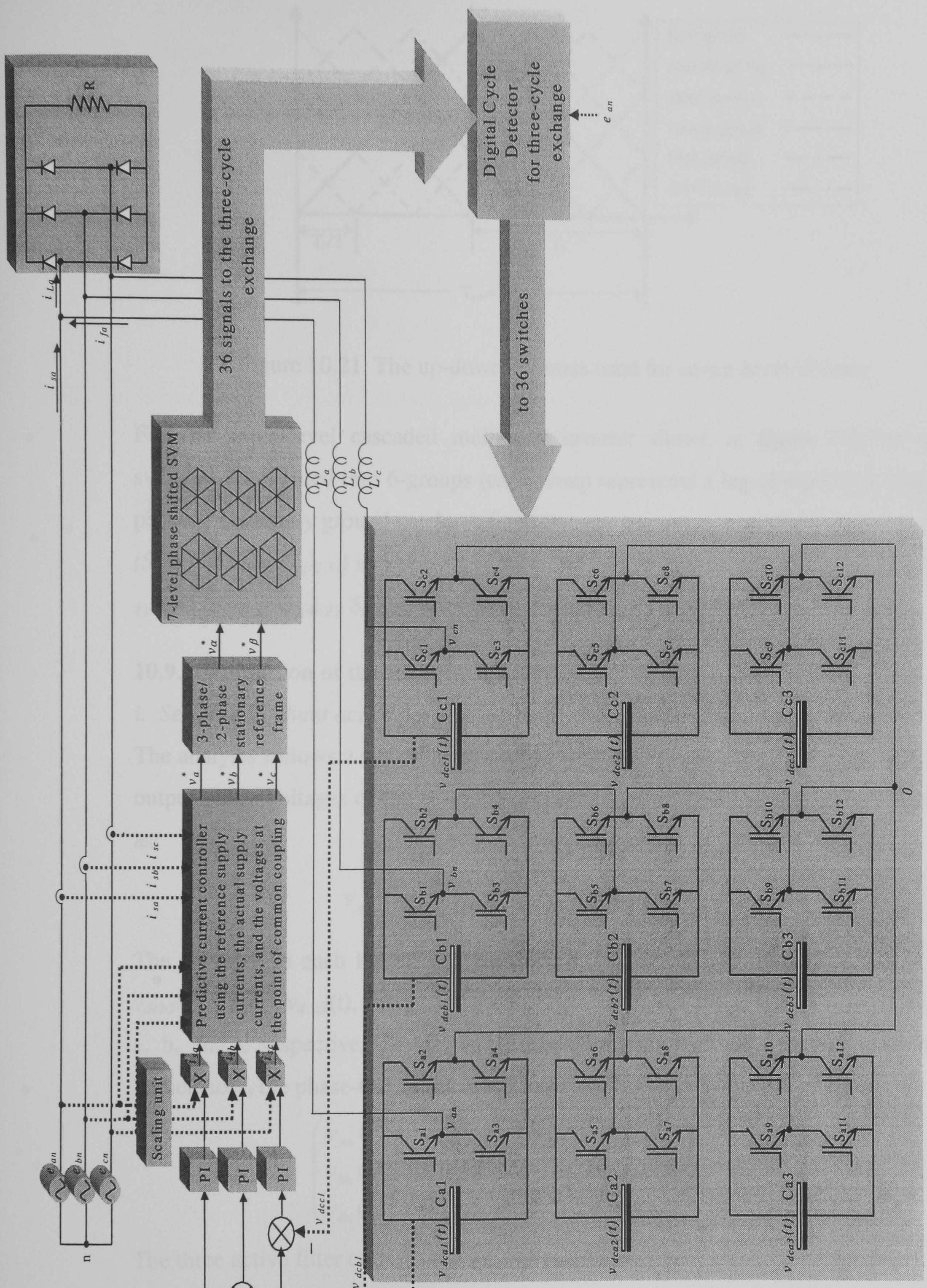


Figure 10.20. The seven-level shunt active power filter block diagram

10.4 Simulation of the five-level APF using PS-SVM

10.4.1 Five-level shunt active power filter state-space model

The five-level inverter used as a shunt active power filter is shown in figure (10.1), from which the three inverter output phase voltages are expressed as:

$$v_{x0}(t) = \sum_{i=1}^{2} v_{dcxi}(t).\left[s_{x(4i-3)} - s_{x(4i-2)}\right] \quad \textit{where } x = a, b \textit{ or } c \tag{10.1}$$

where x denotes phases a, b, and c. The switching state is '1' for the on-state and '0' for the off-state. The switches in each leg are complementary. v_{dca1}(t), v_{dca2}(t), v_{dcb1}(t), v_{dcb2}(t), v_{dcc1}(t), and v_{dcc2}(t) are the instantaneous capacitor voltages of both cells in each phase. Assuming balanced supply voltages and equal interfacing inductances, the phase-to-neutral voltages are:

$$\begin{pmatrix} v_{an}(t) \\ v_{bn}(t) \\ v_{cn}(t) \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}\begin{pmatrix} v_{a0}(t) \\ v_{b0}(t) \\ v_{c0}(t) \end{pmatrix} \tag{10.2}$$

The three active filter currents can be expressed as:

$$L\frac{di_{fx}(t)}{dt} = v_{xn}(t) - e_x(t) \qquad \textit{where } x = \textit{ a, b or c} \tag{10.3}$$

Equation (10.3) shows three independent currents. In simulation, the three currents must be checked to sum to zero. Equation (10.3) cannot be used for either unbalanced supply voltages or unequal interfacing inductances. In equation (10.3), the resistances of the interfacing inductors are neglected. The six capacitors currents (as shown in figure (10.1)) can be expressed in terms of the filter currents i_{fa}, i_{fb}, and i_{fc} as:

$$i_{dcxi}(t) = \left[s_{a(4i-3)} - s_{a(4i-2)}\right] i_{fx}(t) \qquad \text{for } i = 1,\ 2 \tag{10.4}$$

The six capacitor voltages are:

$$i_{dcxi}(t) = -C_{xi}.\frac{dv_{dcxi}(t)}{dt} \tag{10.5}$$

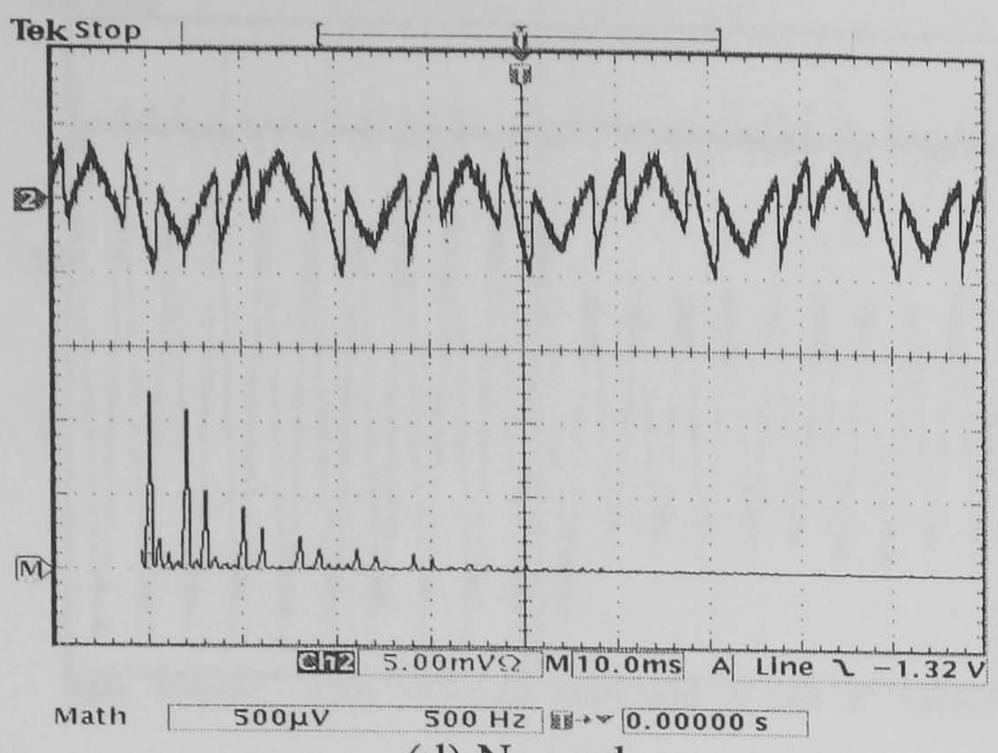
Substituting equation (10.4) into equation (10.5) yields

$$-C_{xi}.\frac{dv_{dcxi}(t)}{dt} = \left[s_{x(4i-3)} - s_{x(4i-2)}\right] i_{fx}(t) \tag{10.6}$$

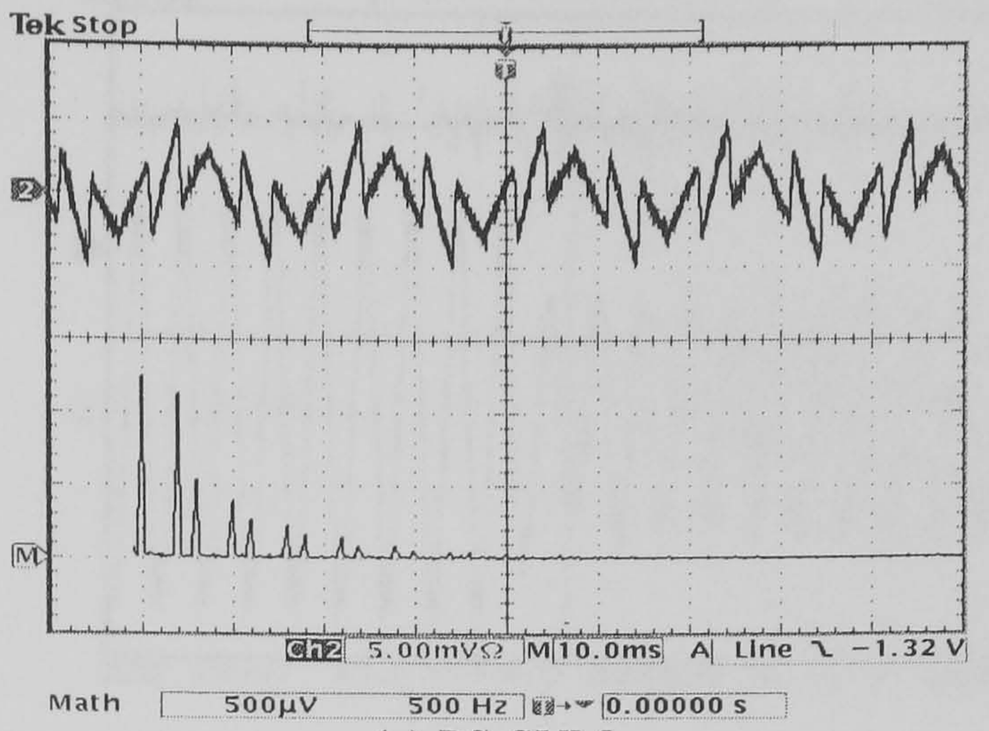
Equations (10.3) and (10.6) represent the state-space model in the following form

$$\dot{X} = A.X + B.U \tag{10.7}$$

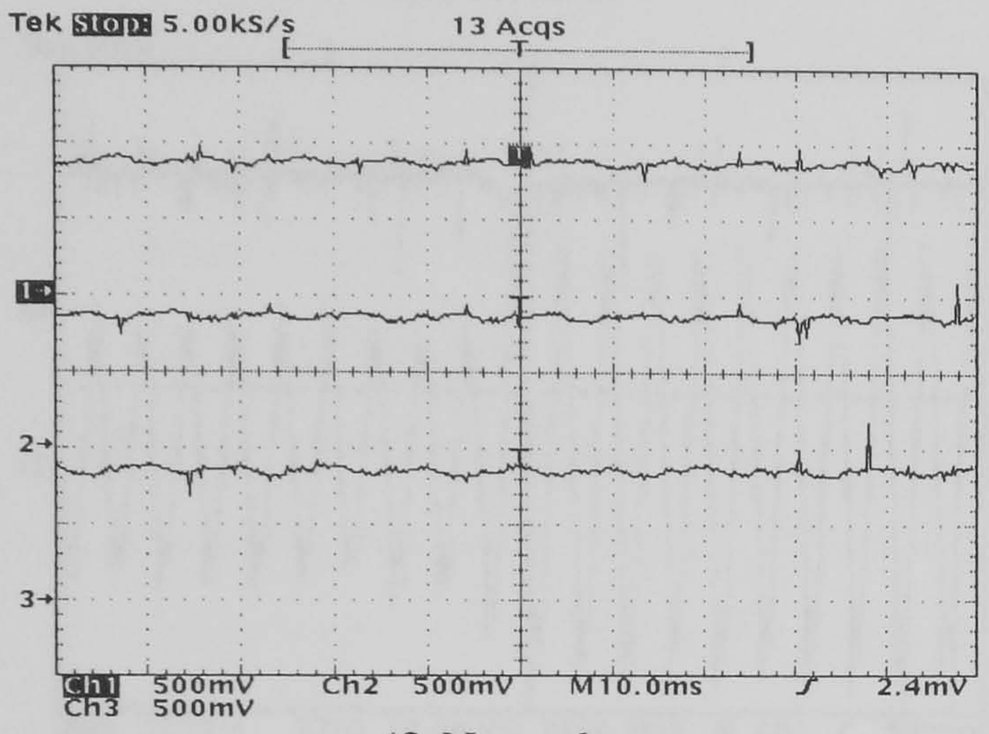
where A, X , B, and U are defined as follows



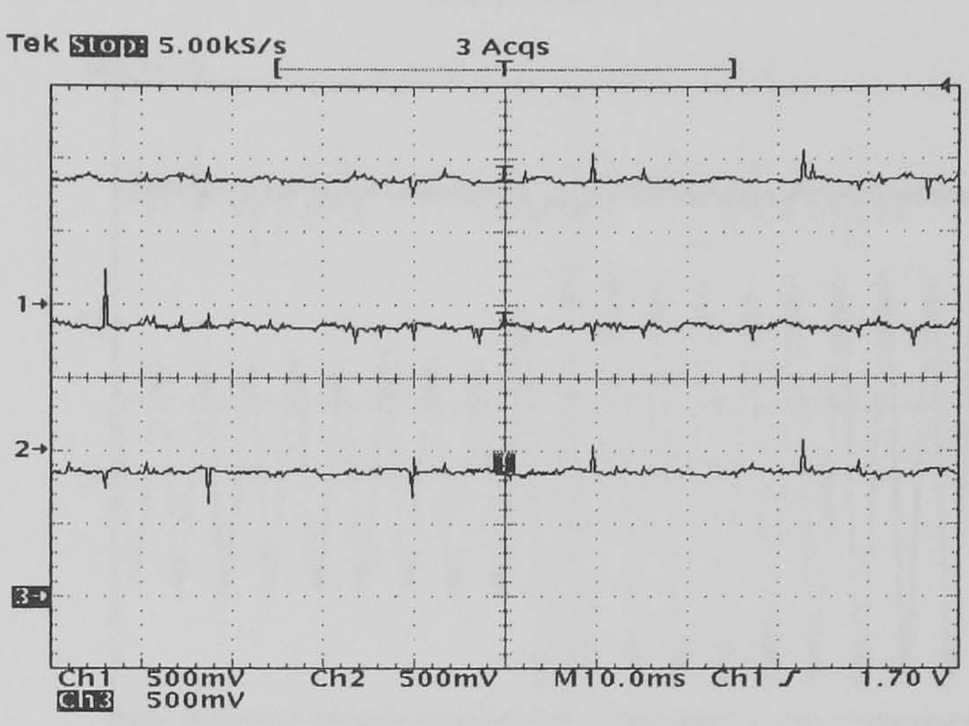
(d) Normal



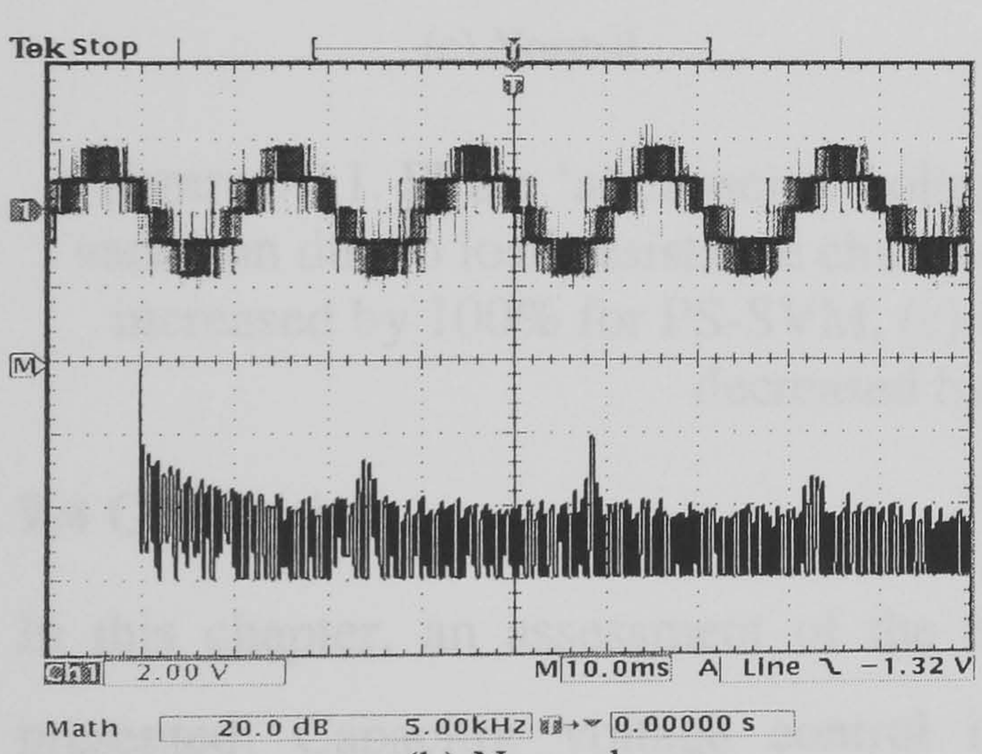
(e) PS-SVM



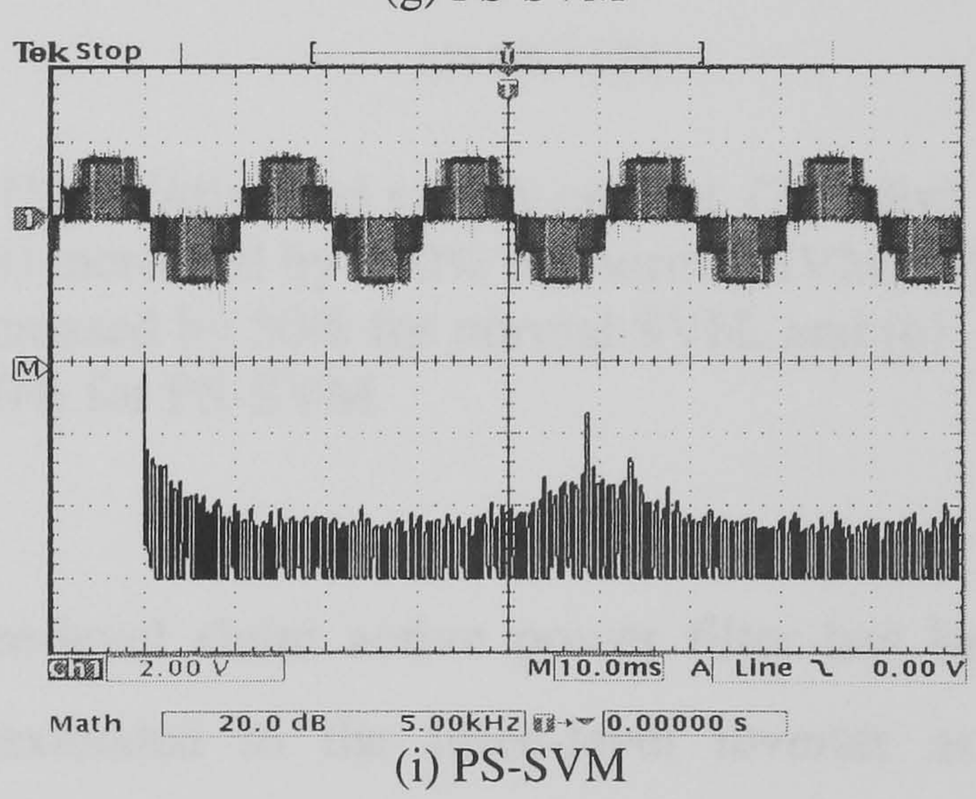
(f) Normal



(g) PS-SVM



(h) Normal



(i) PS-SVM

Figure 9.10. Practical results:
(a) the load current and spectrum (5A/div), (b) the supply current and spectrum for normal SVM (5A/div), (c) the supply current and spectrum for PS-SVM (5A/div), (d) the active filter current and spectrum for normal SVM (2.5A/div), (e) the active filter current and spectrum for PS-SVM (2.5A/div), (f) the capacitor voltages for normal SVM (100 V/div), (g) the capacitor voltages for PS-SVM (100 V/div), (h) the inverter output line voltage for normal SVM (400 V/div), and (i) the inverter output line voltage for PS-SVM (400 V/div)

Parts a and b of figure (9.11) show the capacitor voltage of phase 'a' for normal SVM and PS-SVM respectively, due to a load resistance increase of 100% and then a 50% decrease. Parts c and d show the corresponding supply current of phase 'a' for each modulation case. It is clear that the practical results agree with the simulation results.

are expected and large starting transients in the capacitor voltages and active filter currents may occur that in turn causes tripping of the protection devices. Decreasing k_I increases the restoration time. As a rule of thumb, k_I is chosen between 5 and 20 and $k_p = k_I/100$. In simulation and practice, k_I and k_p are 10 and 0.1 respectively.

For a 50% load current reduction, with the effects shown in figure (9.5), parts a to f of figure (9.8) show the three performance factors as a function of capacitance and integrator coefficient (k_I) for both normal three-level SVM and PS-SVM. It can be concluded that increasing both the integrator coefficient and the capacitance, decreases the maximum overshoot, while increasing the integrator term and decreasing the capacitance, decreases the restoration time. Voltage ripple is independent of integrator coefficient and decreases as capacitance increases.

9.3 Practical results

The two proposed algorithms are implemented using the DSP software (Code Composer see Appendix E). The DSP execution time is 38 μs for normal three-level SVM and is 36 μs for PS-SVM. An inverter dead time of 640 ns is provided using the Xilinx project. Capacitor over-voltage protection is provided using Xilinx such that when one of the three capacitors is over charged, all 12 inverter switches are commutated. Figure (9.9) shows the flow chart procedure for the practical system.

Figure (9.10a) shows the load current and its spectrum. Parts b and c of figure (9.10) show the supply current and its spectrum using normal SVM and PS-SVM respectively. Parts d and e show the active filter current and its spectrum for both modulation schemes. Parts f and g show the capacitor voltages in each modulation case while parts h and i show the line voltage and its spectrum for normal SVM and PS-SVM respectively. It is clear from the parts of figure (9.10) that the voltage harmonic spectrum in the case of PS-SVM appears at 24 kHz and its multiples, while it appears at 12 kHz for normal SVM, which agrees with the simulation results. See appendices G.1. and G.2 for R-L and R-C loads.

7.6 Active Power Filters

Active power filters are divided into AC and DC filters [7.16]. Active DC filters have been designed to compensate for current and/or voltage harmonics on the DC side of thyristor inverters for HVDC systems and on the DC link of a PWM rectifier/inverter for traction systems [7.17]-[7.21]. AC active filters, generally known as active filters (AFs), are also called active power line conditioners, instantaneous reactive power compensators, active power filters, and active power quality conditioners [7.22]. AFs are a mature technology for providing compensation for harmonics, reactive power, and/or neutral current in ac networks. AFs are also used to eliminate voltage harmonics, to regulate terminal voltage, to suppress voltage flicker, and to improve voltage balance in three-phase systems [7.22]. Active power filters, rather than passive filters, have better harmonic compensation characteristics for coping with impedance variation of the AC power line and the frequency variation of harmonic currents. A voltage source PWM inverter is usually used in active power filters (APF) and VAR compensators. A voltage source APF has a capacitor on the DC side with constant DC voltage whereas a current source APF has an inductor with constant DC current. Although the voltage source type is better with regards to losses and filter capacity to eliminate PWM carrier harmonics, the current source type is better with regards to dynamics of compensating current as well as reliability and protection [7.7]. Active filters have a few disadvantages [7.10]:

- The initial and running costs, losses, and complexity of an active filter are much higher than that of a passive filter.
- It is difficult to build an active filter with both a high power rating and a fast dynamic current response.

Depending on the topology, the APF can be classified as series, shunt, or unified power quality conditioner which uses a combination of both. Combinations of active series and passive shunt filtering are known as hybrid filters [7.22].

The maximum harmonic order to be suppressed has no theoretical limit, and is determined by the switching pattern of the active filter. Injecting PWM current enables the harmonic components of orders not greater than the pulse number per half cycle, to be removed completely [7.23]. If harmonic components change in magnitude and frequency, active filters can continue to function without changing any components.

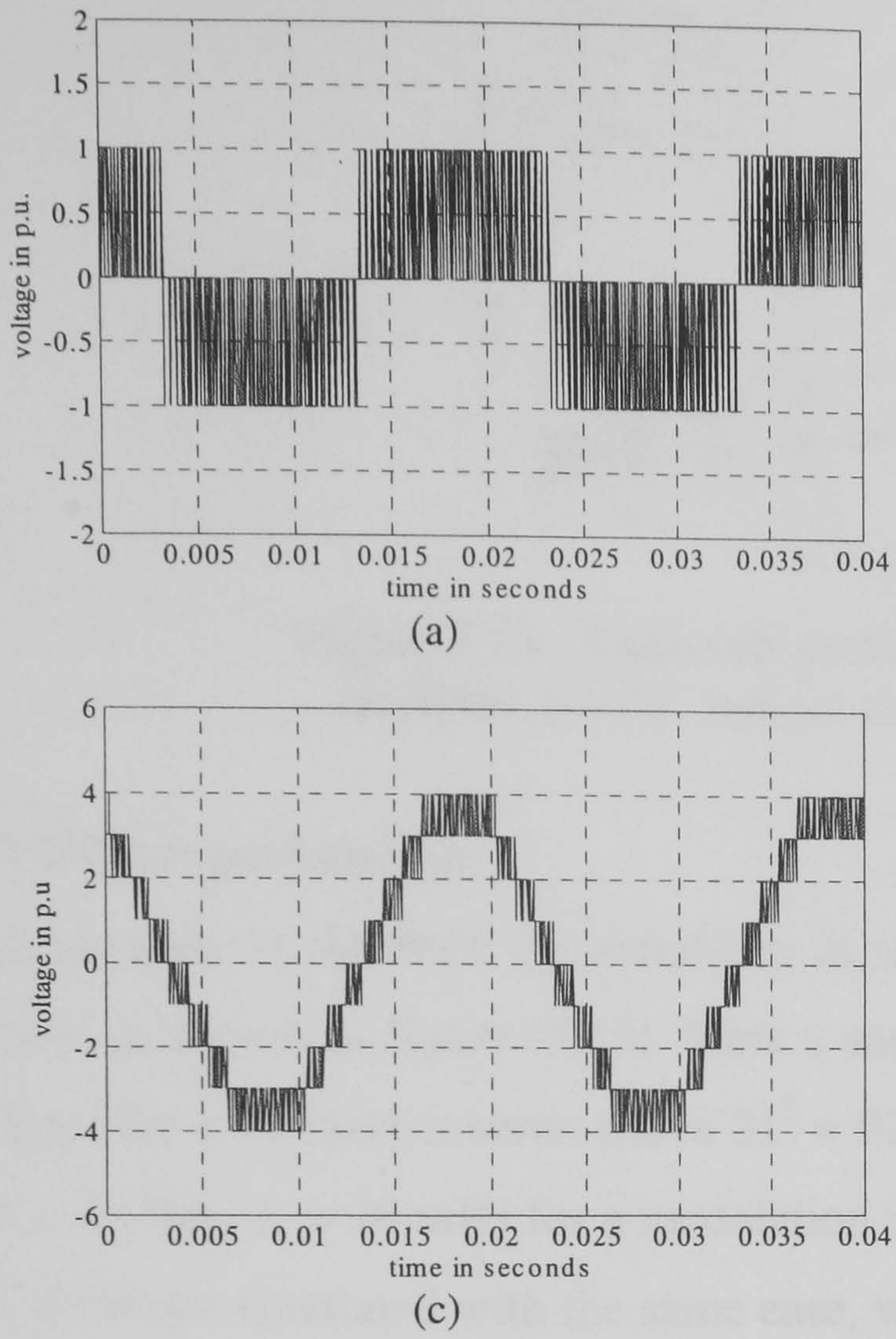
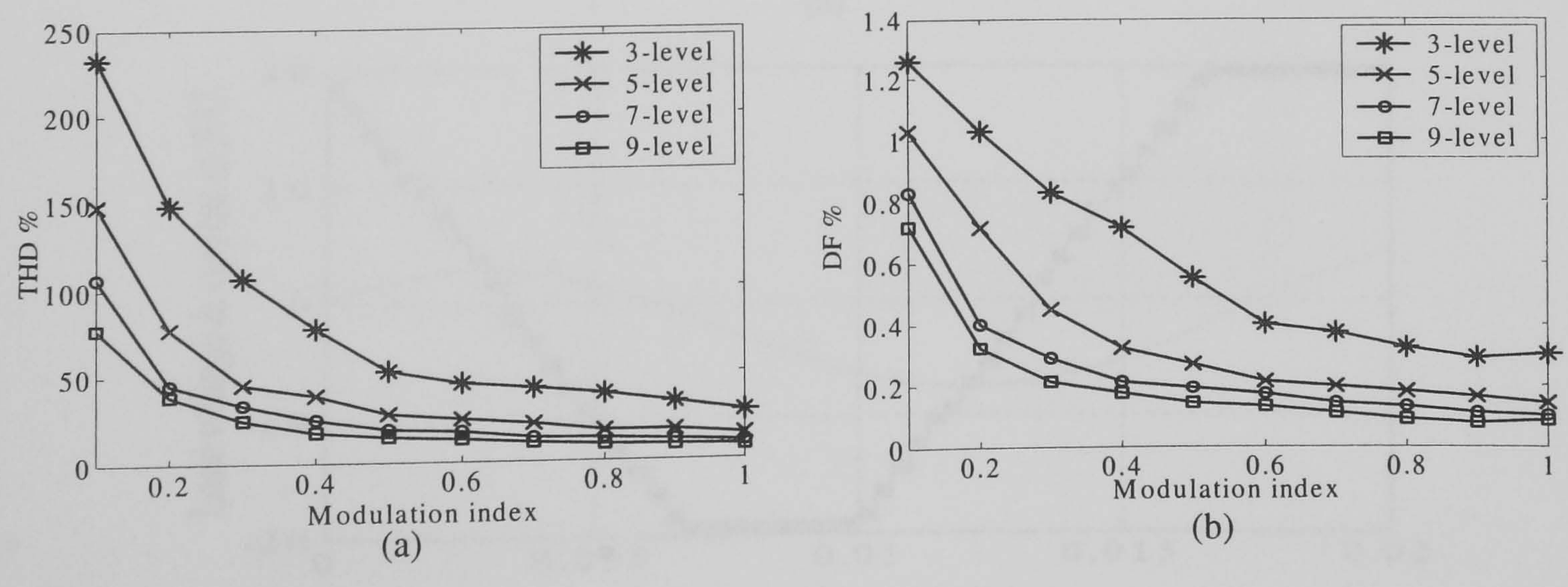


Figure 5.13. Line voltage for:
(a) 2-level, (b) 3-level, (c) 5-level, (d) 7-level, (e) 9-level, and (f) 11-level inverters



distribution between the states can be determined, using numerical analysis, as a function of the parameters a, b, and h.

$$\begin{pmatrix} T_s V_m \cos(\theta) \\ T_s V_m \sin(\theta) \\ T_s \end{pmatrix} = \begin{pmatrix} \left(\frac{2b-1-h}{2}\right)E & \left(\frac{3a-b-2+2h}{2}\right)E & \left(\frac{2b-h}{2}\right)E \\ (h-1)E\cos\left(\frac{\pi}{6}\right) & (b-a)E\cos\left(\frac{\pi}{6}\right) & hE\cos\left(\frac{\pi}{6}\right) \\ 1 & 1 & 1 \end{pmatrix} \begin{pmatrix} t_0 \\ t_1 \\ t_2 \end{pmatrix} \tag{5.18}$$

Solving these equations to find times t_0, t_1, and t_2 gives

$$\begin{pmatrix} t_0 \\ t_1 \\ t_2 \end{pmatrix} = \frac{1}{\Delta} \begin{pmatrix} (b-a-h)E\cos\left(\frac{\pi}{6}\right) & \left(\frac{3b-3a-3h+2}{2}\right)E & r_1E^2\cos\left(\frac{\pi}{6}\right) \\ E\cos\left(\frac{\pi}{6}\right) & -\frac{1}{2}E & (h-b)E^2\cos\left(\frac{\pi}{6}\right) \\ (a-b+h-1)E\cos\left(\frac{\pi}{6}\right) & \left(\frac{3a-3b+3h-1}{2}\right)E & r_2E^2\cos\left(\frac{\pi}{6}\right) \end{pmatrix} \begin{pmatrix} T_s V_m \cos(\theta) \\ T_s V_m \sin(\theta) \\ T_s \end{pmatrix} \tag{5.19}$$

where

$$\Delta = E^2\cos\left(\frac{\pi}{6}\right)(2a-2b+2h-1) \tag{5.20}$$

$$r_1 = ah+h^2-h+ab-b^2 \tag{5.21}$$

$$r_2 = b^2-ab-b+2a-ah+2h-1-h^2 \tag{5.22}$$

Let

$$q = a-b+h \tag{5.23}$$

Then substituting equation (5.23) into equations (5.19) to (5.22), reduces the time equations to:

$$\begin{pmatrix} t_0 \\ t_1 \\ t_2 \end{pmatrix} = \frac{1}{\Delta_1} \begin{pmatrix} -2m_a(m-1)q\cos\left(\frac{\pi}{6}\right) & m_a(m-1)(2-3q) & 2q(h+b)-2h \\ 2m_a(m-1)\cos\left(\frac{\pi}{6}\right) & -m_a(m-1) & 2(q-a) \\ 2m_a(m-1)(q-1)\cos\left(\frac{\pi}{6}\right) & m_a(m-1)(3q-1) & -2q(h+b-2)+2b-2 \end{pmatrix} \begin{pmatrix} T_s\cos(\theta) \\ T_s\sin(\theta) \\ T_s \end{pmatrix} \tag{5.24}$$

where

$$\Delta_1 = 2(2q-1) \tag{5.25}$$

To reduce DSP execution time, t_1 and t_2 are calculated from equation (5.24) while t_0 is calculated from

$$t_0 = T_S - t_1 - t_2 \tag{5.26}$$

three groups of 8 buffered digital signals can be switched to either input or output. Breadboard space is provided for constructing signal conditioning and interface circuits.

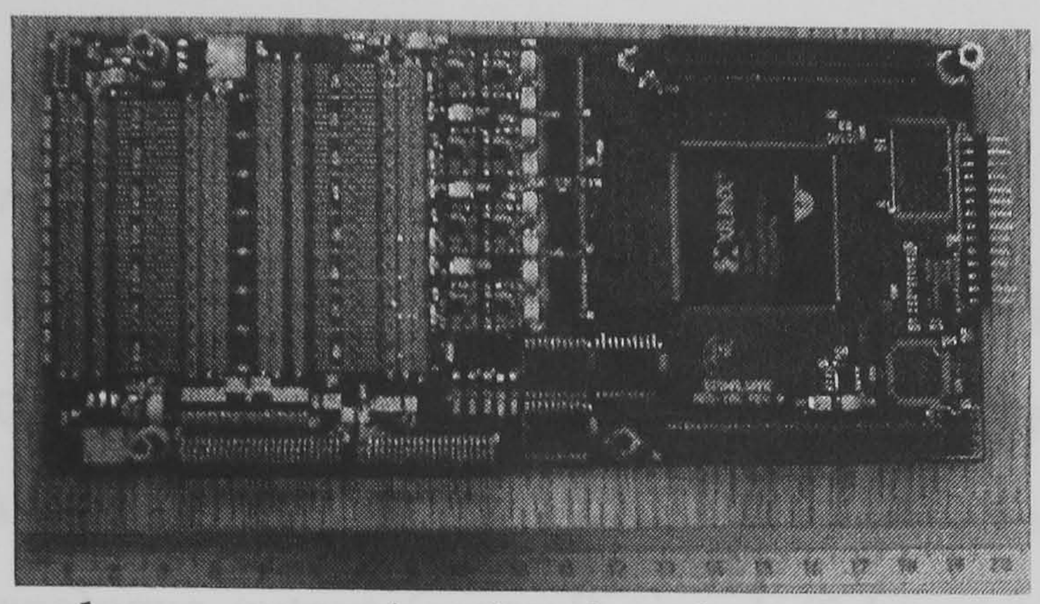


Figure 4.5. The analogue expansion daughter board (AED 106) used with the TMS320C6701

Each of the four A/D converters can sample up to 4 single-ended or 2 differential channels simultaneously, with 12-bit resolution and 1.25 MS/s on each channel. Single channels can be sampled up to 6 MS/s. The bias voltage of the A/D is 2.5 V.

The configuration also includes voltage reference, digital buffers, amplifiers, regulators, programmable logic interface, and 90 pins on I/O connectors for off-board connections. The AED-106 comes with a demonstration logic program and software for the DSP.

Preprocessing of the A/D samples and control of the converters with the Field Programmable Gate Array (FPGA) significantly reduces the load on the DSP, making more computation possible with a single C6701 DSP. The FPGA is a Xilinx Virtex™ XCV50-4 with 57,906 logic gates (2034 flip-flops, 57K RAM bits).

Digital I/O and External Synchronization:

- 24 - Buffered TTL Input/Outputs up to 100 MHz
- Switchable to input or output in groups of 8.

4.1.3 Anti-aliasing filters

The Nyquist theorem states that any signal can be reconstructed if it is sampled at greater than twice the frequency of the highest frequency component of that signal. All frequency components of a sampled signal greater than or equal to one half the sampling frequency will be folded back into the band between DC and half the sampling frequency. This means that all signals, including noise, need to be low pass filtered before they are sampled. This filter is called an anti-aliasing filter [4.10].

For designing an anti-aliasing filter, there are some parameters which define it [4.10], sampling frequency, highest frequency of interest, and desired signal to noise ratio. The